National Semiconductor

PRELIMINARY

# NS16C551 Universal Asynchronous Receiver/Transmitter with FIFOs, Parallel Interface and Decode Logic†

## General Description

The NS16C551 integrates a CMOS version of the NS16550AF UART with a bidirectional parallel interface and an on-chip address decoder into a single IC. The UART is compatible with all existing software written for the INS8250A, NS16450, INS82C50A, NS16C450 and NS16550AF. The parallel port is compatible with all existing software written for the IBM® PC®, XT®, AT®, PS/2® and Centronics parallel ports. Chip selection can be done through an on-chip decoder to reduce the external hardware required when intefacing the NS16C551 with an IBM AT or compatible I/O map. The improved AC timings ensure compatibility with state-of-the-art CPUs.

The UART can operate with on-chip transmitter and receiver FIFOs (FIFO mode) to relieve the CPU of excessive software overhead. In FIFO mode each channel is capable of buffering 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) of data in both the transmitter and receiver. All the FIFO control logic is on-chip to minimize system overhead and maximize system efficiency.

Signalling for DMA transfers is done through two pins per channel ($\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$). The $\overline{\text{RXRDY}}$ function is multiplexed on one pin with the $\overline{\text{OUT 2}}$ and BAUDOUT functions. The CPU can select these functions through a new UART register (Alternate Function Register).

The UART includes one programmable baud rate generator capable of dividing the clock input by divisors of 1 to ($2^{16} - 1$), and producing a 16 × clock for driving the internal logic of both the receiver and transmitter sections. The UART has complete MODEM-control capability, and a processor-interrupt system.

The parallel port has three registers, two of which provide status and control for the data register. The CPU can transfer data through this register in both directions by control of the $\overline{\text{POS}}$ Mode Pin, a bit in the Control register and the $\overline{\text{RD}}$ $\overline{\text{WR}}$ signals. All of the signals required by PC and Centronics printers to transfer data and monitor printer status are provided. On-Chip buffers meet or exceed drive current requirements of the PS/2 systems.

The on-chip decode logic can be used as an alternate to the chip select and channel select pins. When the NS16C551 is mapped to the same addresses as COM1, COM2, LPT1, LPT2 and LPT3 on the AT bus, the decode logic will sense these addresses and enable the appropriate serial or parallel port.

The NS16C551 is fabricated using National Semiconductor's advanced M²CMOS™.

## Features

- UART capable of interfacing with existing INS8250A, NS16450, INS82C50A, NS16C450 and NS16550AF software
- Capable of interfacing with all PC, PS/2 and Centronics parallel port software
- High current drivers that meet or exceed all Micro Channel and PS/2 parallel port drive current requirements
- Provides all control and status pins for a complete PC, AT, PS/2, Micro Channel, and Centronics parallel port interface
- Monitors all signals necessary to decode standard COM1, COM2, LPT1, LPT2 and LPT3 addresses on the PC AT bus
- Read and Write cycle times of 84 ns
- After reset, all UART registers are identical to the 16450 register set
- In the FIFO mode transmitter and receiver are each buffered with 16-byte FIFOs to reduce the number of interrupts presented to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator divide any input clock by 1 to ($2^{16} - 1$) and generate the 16 × clock
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 1.5M baud) with 16 × clock
- False start bit detection
- Line break generation and detection
- Loopback controls for communications link fault isolation
- Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls

†Note: This part is patented.