NCV7718B, NCV7718C

Hex Half-Bridge Driver

The NCV7718B/C is a Hex Half−Bridge Driver with protection features designed specifically for automotive and industrial motion control applications. The NCV7718B/C has independent controls and diagnostics. The device can be operated in forward, reverse, brake, and high impedance states. The drivers are controlled via a 16 bit SPI interface and are daisy chain compatible.

Features

- Low Quiescent Current Sleep Mode
- High−Side and Low−Side Drivers Connected in a Half−Bridge Configuration
- Integrated Freewheeling Protection (LS and HS)
- 0.55 A Peak Current
- $R_{DS(on)}$ = 1 Ω (typ)
- 5 MHz SPI Control
- Compliance with 5 V and 3. 3 V Systems
- Undervoltage and Overvoltage Lockout
- Discriminated Fault Reporting
- Overcurrent Protection
- Overtemperature Protection
- Under Load Detection (LS)
- Daisy Chain Compatible with Multiple of 8 bit Devices
- 16−Bit Frame Detection
- Available SSOP24 Package Options:
  - NCV7718B − Exposed Pad Package
  - NCV7718C − Standard Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial
- DC Motor Management for HVAC Application

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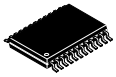
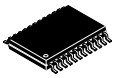
MARKING DIAGRAM



SSOP24 NB EP
DQ SUFFIX
CASE 940AK



SSOP−24
DP SUFFIX
CASE 565AL

A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 26 of this data sheet.

Shown below is a typical application for the NCV7718B/C configuration.

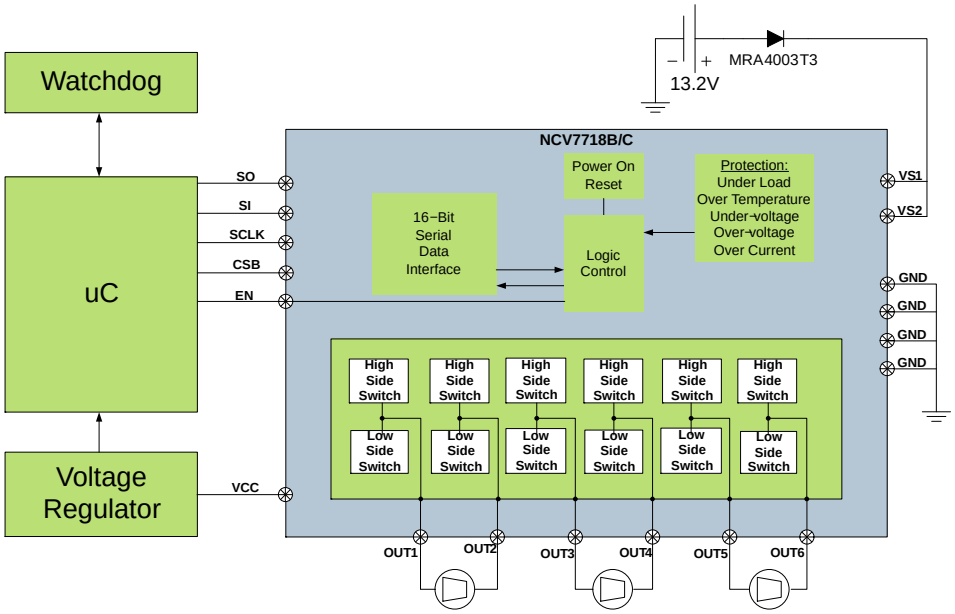


Figure 1. Typical Application

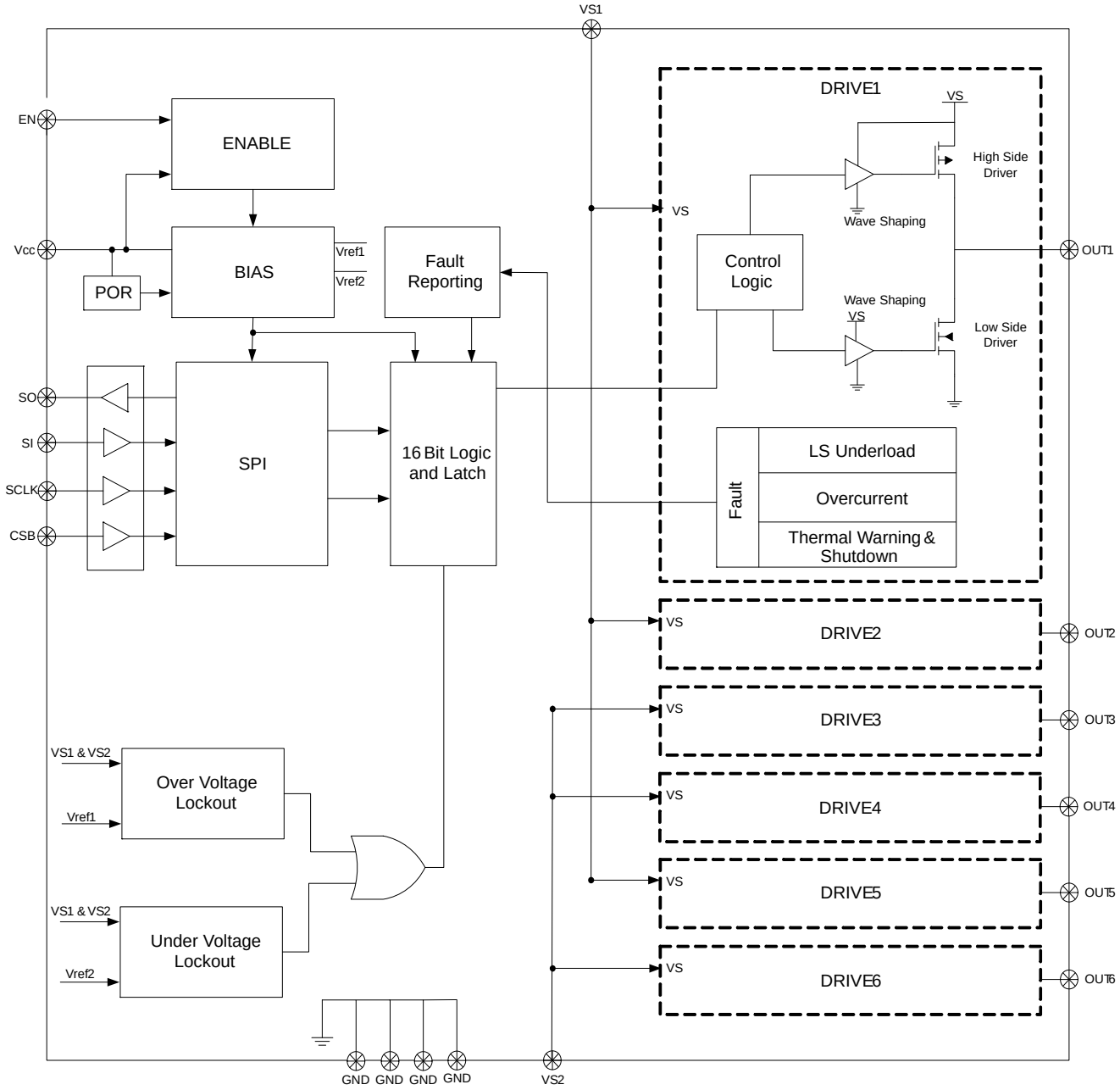


Figure 2. Block Diagram

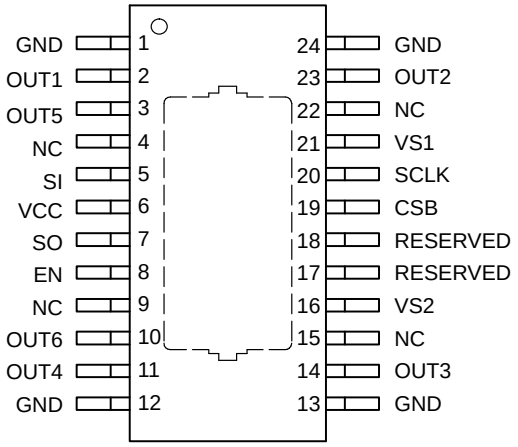


Figure 3. Pinout − SSOP24 NB and SSOP24 NB EP (Top View)

PACKAGE PIN DESCRIPTION: SSOP24 NB, SSOP24 NB EP

Pin #	Symbol	Description
1	GND	Ground. Shorted to pin 24 internally.
2	OUT1	Half Bridge Output 1
3	OUT5	Half Bridge Output 5
4	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
5	SI	Serial Input. 16 bit serial communications input. 3.3 V/5 V (TTL) Compatible. Internally pulled down.
6	VCC	Power supply input for Logic.
7	SO	Serial Output. 16 bit serial communications output. 3.3 V/5 V Complaint
8	EN	Enable. Input high wakes the IC up from a sleep mode. 3.3 V/5 V (TTL) Compatible. Internally pulled down.
9	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
10	OUT6	Half Bridge Output 6
11	OUT4	Half Bridge Output 4
12	GND	Ground. Shorted to pin 13 internally.
13	GND	Ground. Shorted to pin 12 internally.
14	OUT3	Half Bridge Output 3
15	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
16	VS2	Voltage Power Supply input for the Drivers 3, 4 and 6. This pin must be connected to VS1 externally.
17	Reserved	Factory use − connect to GND or leave unconnected − internally pulled down.
18	Reserved	Factory use − connect to GND or leave unconnected − internally pulled down.
19	CSB	Chip Select Bar. Active low serial port operation. 3.3V/5V (TTL) Compatible. Internally pulled up.
20	SCLK	Serial Clock. Clock input for use with SPI communication. 3.3 V/5 V (TTL) Compatible. Internally pulled down.
21	VS1	Voltage Power Supply input for the Drivers 1, 2 and 5, all the pre−drivers and the charge pump. This pin must be connected to VS2 externally.
22	NC	No Connection. This pin should be isolated from any traces or via on the PCB board.
23	OUT2	Half Bridge Output 2
24	GND	Ground. Shorted to pin 1 internally.
EPAD	Exposed Pad	Connect to GND or leave unconnected (SSOP24 NB EP package option).

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (VS1, VS2) (DC) (AC), t < 500ms, Ivsx > −2A	VsxdcMax VSXac	 −0.3 to 40 −1.0	V
Output Pin OUTx (DC) (AC), t< 500ms, IOUTx > −1.1A (AC), t< 500ms, IOUTx < 1A	VoutxDc VoutxAc	 −0.3 to 40 −1.0 1.0	V
Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, V_{CC})	VioMax	−0.3 to 5.5	V
Output Current (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6)	IoutxImax	−2.0 to 2.0	A
Electrostatic Discharge, Human Body Model, VSx, OUTx (AEC−Q100−002)	Vesd4k	≥ ±4.0	kV
Electrostatic Discharge, Human Body Model, all other pins (AEC−Q100−002)	Vesd2k	≥ ±2.0	kV
Electrostatic Discharge, Charged Device Model (AEC−Q100−011)	VesdCDM	Level C4B	−
Short Circuit Reliability Characterization	AECQ10x	Grade A	−
Operating Junction Temperature	Tj	−40 to 150	°C
Storage Temperature Range	Tstr	−55 to 150	°C
Moisture Sensitivity Level (MAX 260°C Processing) SSOP24 NB, SSOP24 NB EP	MSL	2	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL INFORMATION (Note 1)

Rating		Symbol	SSOP24 NB EP	SSOP24 NB	Unit
Package Thermal Resistance − Still−air					°C/W
Junction−to−Ambient	(Note 2)	$R_{\theta JA}$	56	−	
	(Note 3)	$R_{\theta JA}$	22	−	
	(Note 4)	$R_{\theta JA}$	−	95	
Junction−to−Board	(Note 2)	$R_{\psi JBOARD}$	28	−	
	(Note 3)	$R_{\psi JBOARD}$	12	−	
Junction−to−Lead	(Note 4)	$R_{\psi JL}$	−	62	

1. Thermal Information is based on having 3 high side and 3 low side drivers dissipating 80 mW each.
2. 2S0P 2−layer PCB based on JESD51−3, 1.2 mm thick FR4, with 2 oz. copper and 18 thermal vias to 600 mm^2 spreader on bottom layer.
3. 2S2P 4−layer PCB based on JESD51−7, 1.2 mm thick FR4, with 2 oz. copper and 18 thermal vias to 80x80 mm 1 oz. internal planes.
4. 2S0P 2−layer PCB based on JESD51−3, 1.2 mm thick FR4, with 2 oz. copper to 600 mm^2 spreader on top layer.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value		Unit
		Min	Max	
Digital Supply Input Voltage	VccOp	3.15	5.25	V
Battery Supply Input Voltage	VsxOp	5.5	28	V
DC Output Current	IxOp	−	0.55	A
Junction Temperature	TjOp	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Supply Current (VS1 + VS2) Sleep Mode	IqVsx85	VS1 = VS2 = 13.2 V, V_{CC} = 0 V −40°C to 85°C No Load	−	1.0	2.5	μA
Supply Current (VS1 + VS2) Active Mode	IvsOp	EN = V_{CC}, 5.5 V < VSx < 28 V No Load	−	2.5	5.0	mA
Supply Current (V_{CC}) Sleep Mode	IqV_{CC}	CSB = V_{CC}, EN = SI = SCLK = 0 V (−40°C to 85°C)	−	1.0	2.5	μA
Active Mode	$IV_{CC}Op$	EN = CSB = V_{CC}, SI = SCLK = 0 V No Load	−	1.5	3.0	mA
Total Sleep Mode Current I(VS1) + I(VS2) + I(VCC)	IqTot	Sleep Mode, −40°C to 85°C, No Load	−	2	5	μA
V_{CC} Power−On−Reset Threshold	V_{CC}por	V_{CC} increasing	−	2.55	2.9	V
VSx Undervoltage Detection Threshold	VsXuv	VSx decreasing	3.7	4.1	4.5	V
VSx Undervoltage Detection Hysteresis	VsXuHys		100	−	450	mV
VSx Overvoltage Detection Threshold	VsXov	VSx increasing	32	36	40	V
VSx Overvoltage Detection Hysteresis	VsXoHys		1	2.5	4	V
THERMAL RESPONSE						
Thermal Warning	Twr	Not ATE tested	120	140	170	°C
Thermal Warning Hysteresis	TwHy	Not ATE tested	−	20	−	°C
Thermal Shutdown	Tsd	Not ATE tested	150	175	200	°C
Thermal Shutdown Hysteresis	TsdHy	Not ATE tested	−	20	−	°C
OUTPUTS						
Output High $R_{DS(on)}$ (source)	RDSonHS	I_{out} = −500 mA, VSx = 13.2 V, V_{CC} = 3.15 V	−	1	2.25	Ω
Output Low $R_{DS(on)}$ (sink)	RDSonLS	I_{out} = 500 mA, VSx = 13.2 V, V_{CC} = 3.15 V	−	1	2.0	Ω
Output Path $R_{DS(HSx+LSx)}$	RDSonPath	I_{out} = |500| mA	−	−	4.0	Ω
Source Leakage Current	IsrcLkg13.2	V_{CC} = 5 V, OUT(1−6) = 0 V, −40°C to 85°C; V_{Sx} = 13.2 V	−1.0	−	−	μA
	IsrcLkg28	V_{Sx} = 28 V	−2.0	−	−	
Sink Leakage Current	IsnkLkg13.2	V_{CC} = 5 V; OUT(1−6) = V_{Sx} = 13.2 V	−	−	1.0	μA
	IsnkLkg28	OUT(1−6) = V_{Sx} = 28 V	−	−	2.0	
Overcurrent Shutdown Threshold (Source)	IsdSrc	V_{CC} = 5 V, VSx = 13.2 V	−2.0	−1.2	−0.8	A
Overcurrent Shutdown Threshold (Sink)	IsdSnk	V_{CC} = 5 V, VSx = 13.2 V	0.8	1.2	2.0	A
Over Current Delay Timer	TdOc		10	25	50	μs
Under Load Detection Threshold (Low Side)	IuldLS	V_{CC} = 5 V, VSx = 13.2 V	2.0	11	20	mA
Under Load Detection Delay Time	TdUld	V_{CC} = 5 V, VSx = 13.2 V	200	350	600	μs

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 5.5 V < VSx < 40 V, 3.15 V < V_{CC} < 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
BODY DIODE						
Power Transistor Body Diode Forward Voltage	VbdFwd	If = 500 mA	−	0.9	1.3	V
LOGIC INPUTS (EN, SI, SCLK, CSB)						
Input Threshold High Low	VthInH VthInL		 2.0 −	 − −	 − 0.6	V
Input Hysteresis (SI, SCLK, CSB)	VthInHys		50	150	300	mV
Enable Hysteresis	VthENHys		150	400	800	mV
Input Pull−down Resistance (EN, SI, SCLK)	Rpdx	EN = SI = SCLK = V_{CC}	50	125	200	kΩ
Input Pull−up Resistance (CSB)	RpuCSB	CSB = 0 V	50	125	250	kΩ
Input Capacitance	Cinx	Not ATE tested	−	−−	15	pF
LOGIC OUTPUT (SO)						
Output High	VsoH	I_{SOURCE} = −1 mA	V_{CC} − 0.6	−	−	V
Output Low	VsoL	I_{SINK} = 1.6 mA	−	−	0.4	V
Tri−state Leakage	ItriStLkg	CSB = 5 V	−5	−	5	μA
Tri−state Output Capacitance	ItriStCout	CSB = V_{CC}, 0 V < V_{CC} < 5.25 V Not ATE tested	−	−	15	pF

ELECTRICAL CHARACTERISTICS (−40°C < TJ < 150°C, 5.5 V < VSx < 40 V, 3.15 < Vcc < 5.25 V, EN= Vcc, unless otherwise specified)

Characteristic	Symbol	Conditions	Timing Chart	Min	Typ	Max	Unit
DRIVER OUTPUT TIMING SPECIFICATIONS							
High Side Turn On Time	ThsOn	VSx = 13.2 V, R_{load} = 39 Ω		−	7.5	13	μs
High Side Turn Off Time	ThsOff	VSx = 13.2 V, R_{load} = 39 Ω		−	3.0	6.0	μs
Low Side Turn On Time	TlsOn	VSx = 13.2 V, R_{load} = 39 Ω		−	6.5	13	μs
Low Side Turn Off Time	TlsOff	VSx = 13.2 V, R_{load} = 39 Ω		−	2.0	6.0	μs
High Side Rise Time	ThsTr	VSx =13.2 V, R_{load} = 39 Ω		−	4.0	8.0	μs
High Side Fall Time	ThsTf	VSx = 13.2 V, R_{load} = 39 Ω		−	2.0	4.0	μs
Low Side Rise Time	TlsTr	VSx = 13.2 V, R_{load} = 39 Ω		−	1.0	3.0	μs
Low Side Fall Time	TlsTf	VSx = 13.2 V, R_{load} = 39 Ω		−	1.0	3.0	μs
High Side Off to Low Side On Non−Overlap Time	ThsOffLsOn	VSx = 13.2 V, R_{load} = 39 Ω		1.5	−	−	μs
Low Side Off to High Side On Non−Overlap Time	TlsOffHsOn	VSx = 13.2 V, R_{load} = 39 Ω		1.5	−	−	μs
SERIAL PERIPHERAL INTERFACE							
SCLK Frequency	Fclk	V_{CC} = 5 V V_{CC} = 3.15 V		− −	− −	5.0 2.0	MHz
SCLK Clock Period	TpClk	V_{CC} = 5 V V_{CC} = 3.15 V		200 500	− −	− −	ns
SCLK High Time	TclkH		1	85	−	−	ns
SCLK Low Time	TclkL		2	85	−	−	ns
SCLK Setup Time	TclkSup		3 4	85 85	− −	− −	ns
SI Setup Time	TsiSup		11	50	−	−	ns
SI Hold Time	TsiH		12	50	−	−	ns
CSB Setup Time	TcsbSup		5 6	100 100	− −	− −	ns
CSB High Time (Note 5)	TcsbH		7	5.0	−	−	μs
SO enable after CSB falling edge	TenSo	V_{CC} = 5 V	8	−	−	200	ns
SO disable after CSB rising edge	TdisSo	V_{CC} = 5 V	9	−	−	200	ns
SO Rise Time	TsoR	C_{load} = 40 pF Not ATE tested	−	−	10	25	ns
SO Fall Time	TsoF	C_{load} = 40 pF Not ATE tested	−	−	10	25	ns
SO Valid Time	TsoV	C_{load} = 40 pF SCLK ↑ to SO 50%, Not ATE tested	10	−	20	50	ns
EN Low Valid Time (Note 6)	TenL	V_{CC} = 5 V EN going low 50% to OUTx turing off 50%		10	−	−	μs
EN High to SPI Valid	TenHspiV			−	−	100	μs
SRR Delay Between Two Consecutive Frame (Note 7)	Tsrr			150	−	−	μs

5. This is the minimum time the user must wait between SPI commands.
6. This is the minimum time the user must wait before bringing EN up.
7. This is the minimum time the user must wait to send a SRR command between consecutive frames. If Tsrr time is not met the SRR request is ignored.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTIC TIMING DIAGRAMS

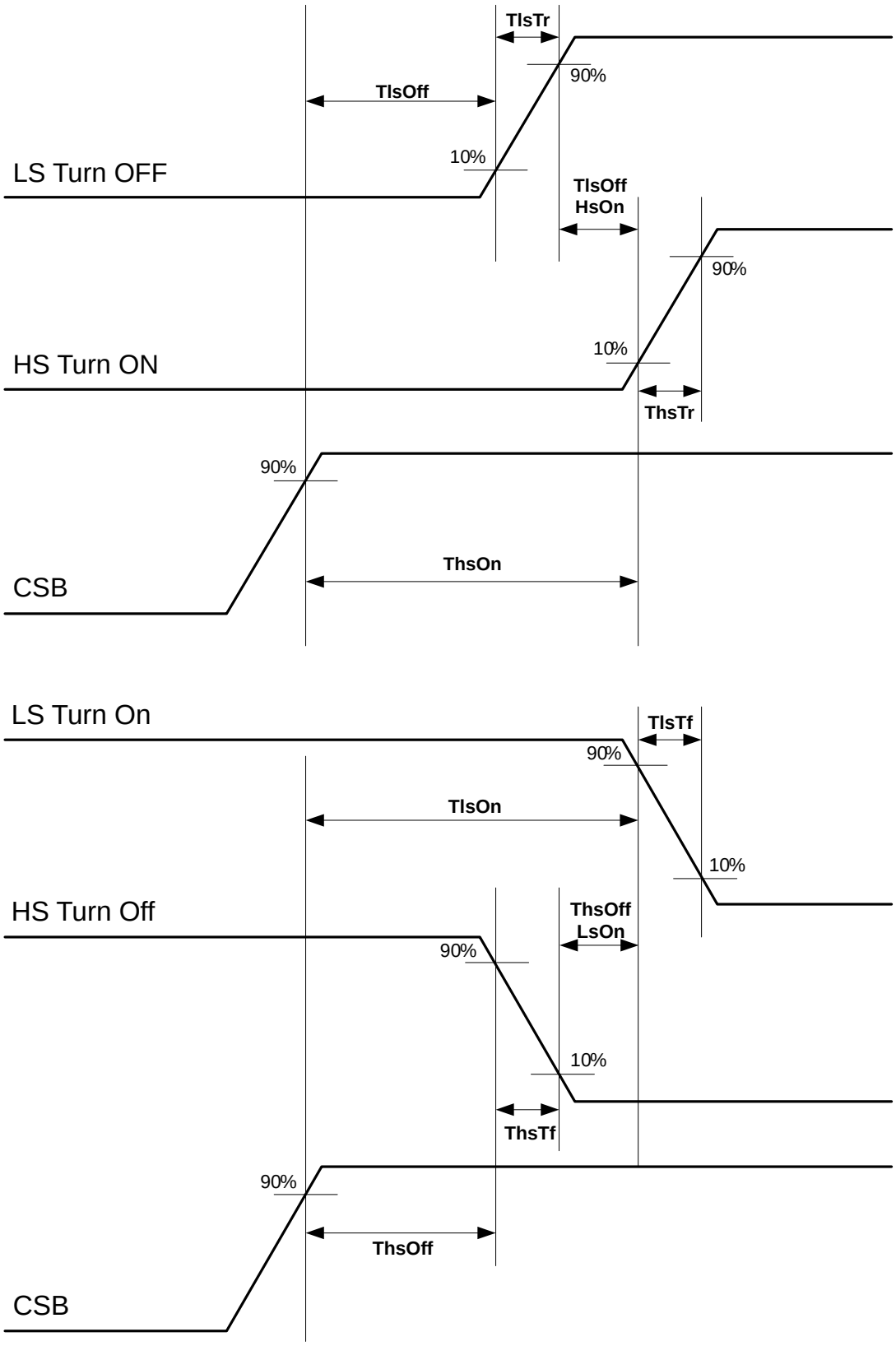


Figure 4. Detailed Driver Timing

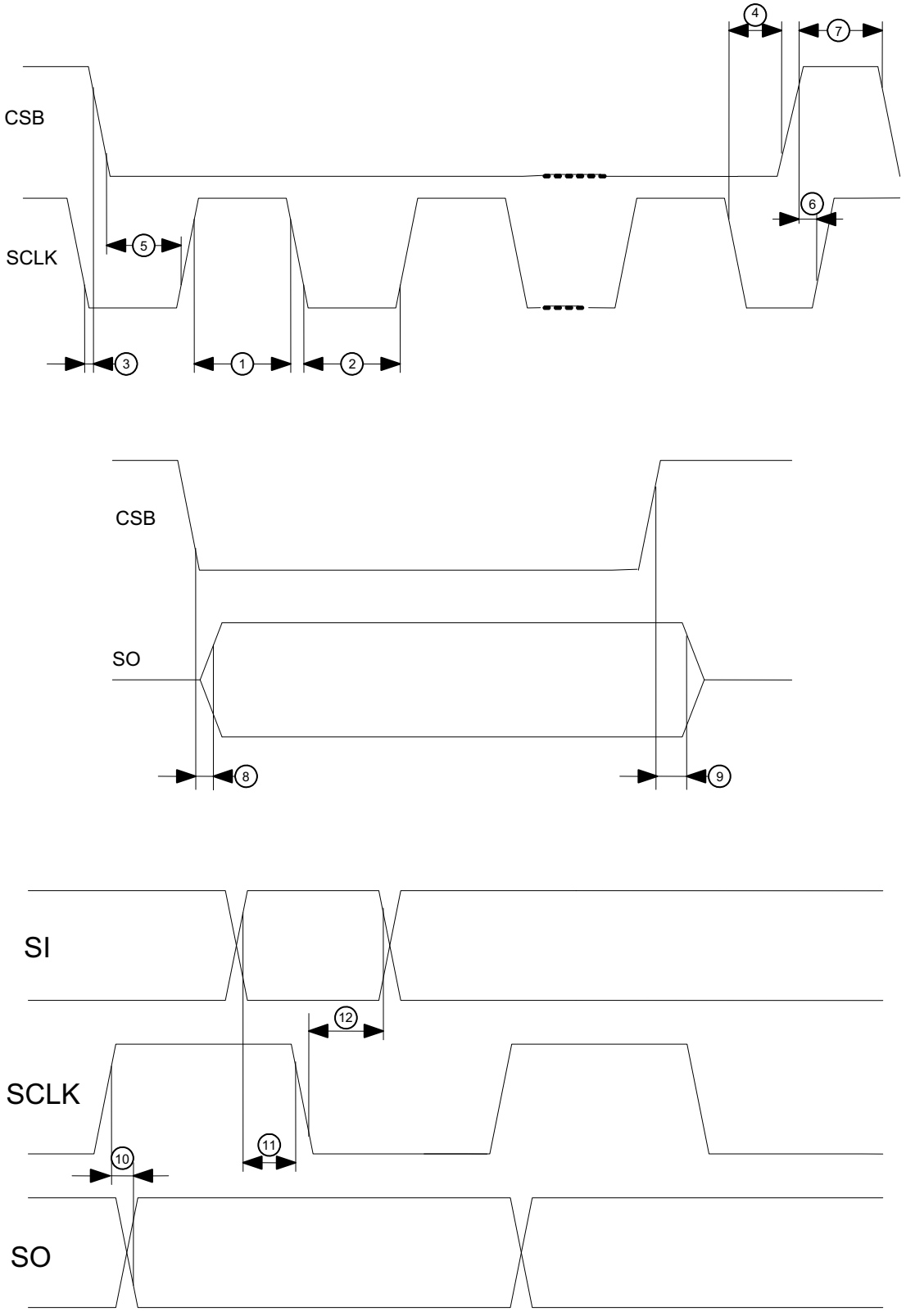


Figure 5. Detailed SPI Timing

TYPICAL PERFORMANCE GRAPHS

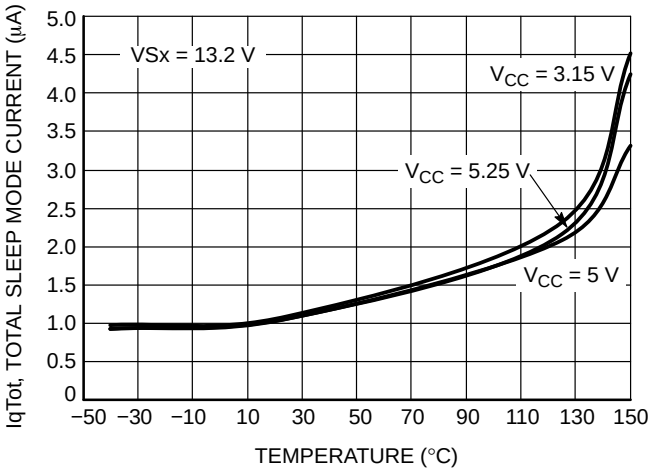


Figure 6. IqTot vs. Temperature

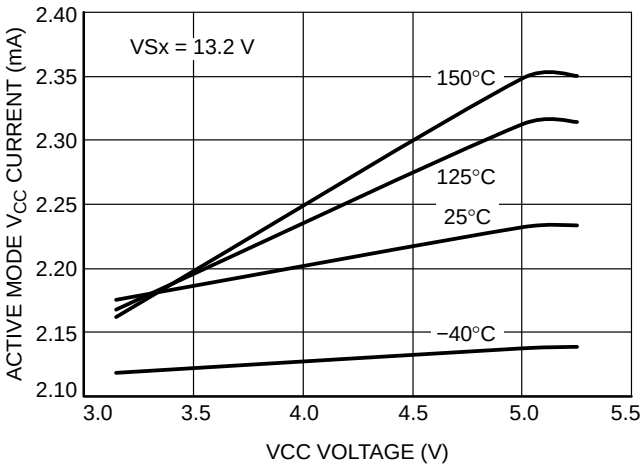


Figure 7. I(V_{CC}) Active Mode vs. V(V_{CC})

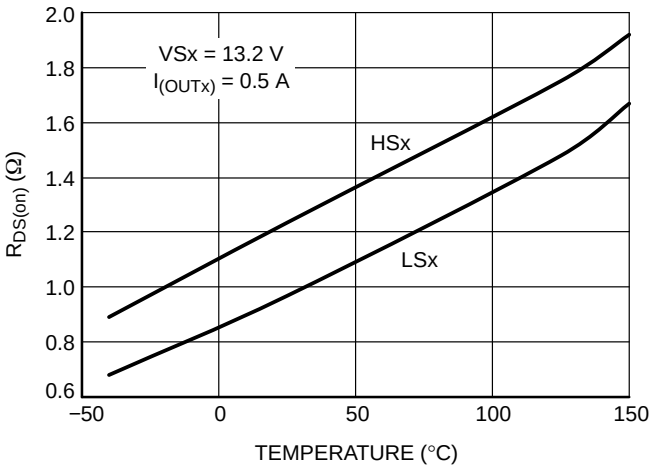


Figure 8. $R_{DS(on)}$ vs. Temperature

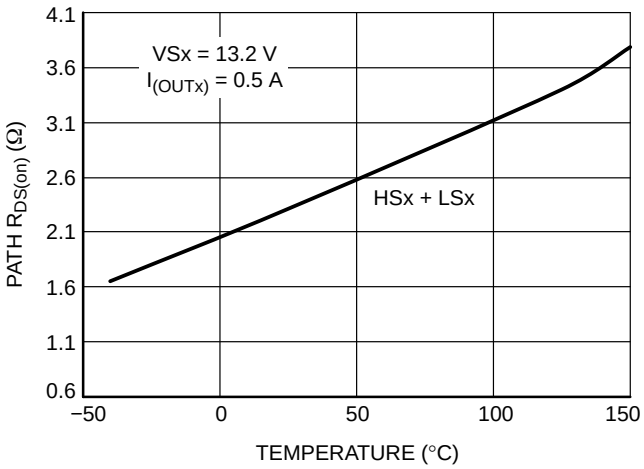


Figure 9. $R_{DS(on)}$ vs. Temperature

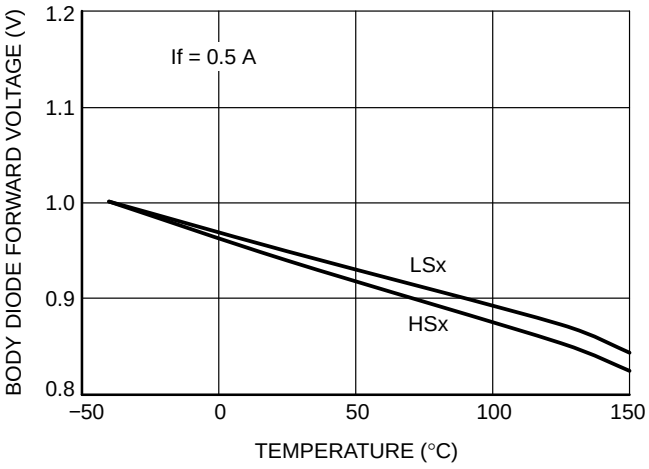


Figure 10. Body Diode vs. Temperature

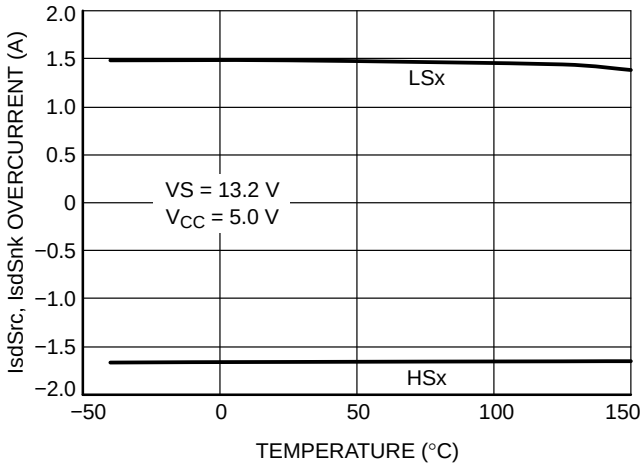


Figure 11. Overcurrent vs. Temperature

TYPICAL PERFORMANCE GRAPHS

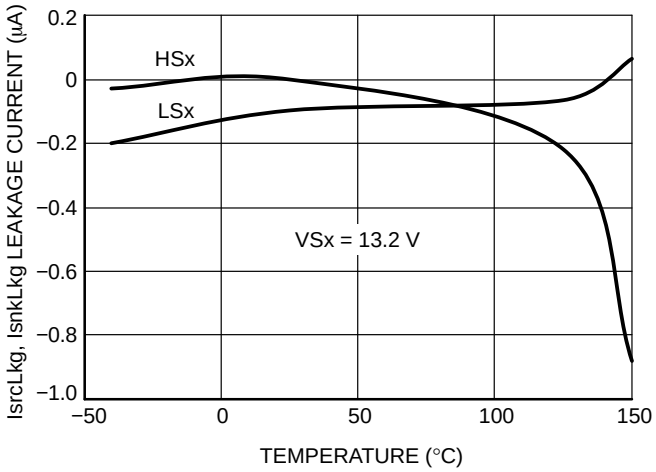


Figure 12. Source−Sink Leakage vs. Temperature

OPERATING DESCRIPTION

General Overview

The NCV7718B/C is comprised of twelve DMOS power drivers (six PMOS High Side Driver and six NMOS Low Side Driver) configured as six half bridges that enables three independent Full Bridge operations. Each output drive is characterized for a max 550 mA DC load and has a typical 2 A surge capability (at VSx =13.2 V). Strict adherence to integrated circuit die temperature is necessary. Maximum die temperature is 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting is handled via the SPI (Serial Peripheral Interface) port.

An Enable function (EN) provides a low quiescent sleep current mode when the device is not being utilized. No data is stored when the device is in sleep mode. An internal pull down resistor is provided on the EN input to ensure the device is off if the input signal is lost. De−asserting the EN signal clears all the registers and resets the driver. When the EN signal is asserted the IC will proceed with the V_{CC} POR cycle and brings the drivers into normal operation.

SPI Communication

16−bit full duplex SPI communication has been implemented for the communication of this IC for device configurations, driver controls and reading the diagnostic data. In addition to the 16−bit diagnostic data, a pseudo bit (PRE_15) can also be retrieved from the SO register. The part is required to be enabled (EN active high) for SPI communication. The inputs for the SPI are TTL logic compatible and are specified by the VthInH and VthInL thresholds. The active low CSB input has a pull up resistor and the remaining SPI inputs have pull−down resistors to bias them to a known state when SPI is not active.

Reference the SPI communication frame format diagram in Figure 13 for the 16 bit SPI implementation. Tables 1 and 2 define the programming bits and diagnostic bits shown in Figure 13.

SPI COMMUNICATION FRAME FORMAT

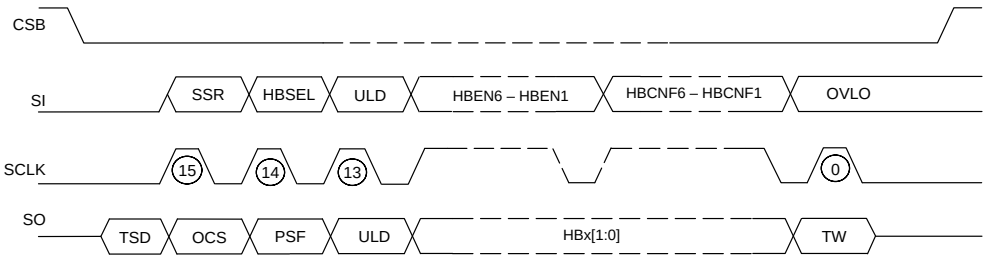


Figure 13. SPI Communication Frame Format

Communication is implemented as follows and is also illustrated in Figure 16:

1. SI and SCLK are set to low before the CSB cycle.
2. CSB goes low to allow serial data transfer.
3. SI data starting with the Most Significant bit (MSB) is shifted in first.
4. SI data is recognized on every falling edge of the clock.
5. Simultaneously, SO data from the previous frame starting with the MSB bit is shifted out on every rising edge of the clock.
6. The input data is compared to a 16 bit counter for the initial 16 bits shifted into SI for frame detection error scheme.
7. The sequential input bits are compared to a *n* x 8 (*n* can take on the value of any integer) bit counter for daisy chain operations and are monitored by the frame detection error scheme.
8. CSB goes high and the most recent 16 bits clocked into SI are transferred to the data register given that there is no frame detection error. Otherwise the entire frame is ignored.
9. SO is tri−state when CSB is high.

Table 1. SPI INPUT DATA FRAME

Input Data			
Bit Number	**Bit Name**	**Bit Description**	**Bit Status**
15	SRR	Status Reset Register When Asserted All Latched Faults are Cleared (TSD, OCS & ULD)	0 = No Reset
			1 = Reset
14	HBSEL (Note 8)	Half Bridge Selection	Reserved
13	ULDSC	Under Load Detection Shutdown Control Global Enable; Per Half Bridge Operation	0 = Disable
			1 = Enable
12	HBEN6	Half Bridge 6 Enable	0 = High Z
			1 = Enabled
11	HBEN5	Half Bridge 5 Enable	0 = High Z
			1 = Enabled
10	HBEN4	Half Bridge 4 Enable	0 = High Z
			1 = Enabled
9	HBEN3	Half Bridge 3 Enable	0 = High Z
			1 = Enabled
8	HBEN2	Half Bridge 2 Enable	0 = High Z
			1 = Enabled
7	HBEN1	Half Bridge 1 Enable	0 = High Z
			1 = Enabled
6	HBCNF6	Half Bridge 6 Configuration Control	0 = LS6 ON & HS6 OFF
			1 = LS6 OFF & HS6 ON
5	HBCNF5	Half Bridge 5 Configuration Control	0 = LS5 ON & HS5 OFF
			1 = LS5 OFF & HS5 ON
4	HBCNF4	Half Bridge 4 Configuration Control	0 = LS4 ON & HS4 OFF
			1 = LS4 OFF & HS4 ON
3	HBCNF3	Half Bridge 3 Configuration Control	0 = LS3 ON & HS3 OFF
			1 = LS3 OFF & HS3 ON
2	HBCNF2	Half Bridge 2 Configuration Control	0 = LS2 ON & HS2 OFF
			1 = LS2 OFF & HS2 ON
1	HBCNF1	Half Bridge 1 Configuration Control	0 = LS1 ON & HS1 OFF
			1 = LS1 OFF & HS1 ON
0	OVLO	Over Voltage Lock Out Global Effect	0 = Disable
			1 = Enable

8. HBSEL enables bridge selection for the NCV7719 and NCV7720 devices. In the NCV7718B/C it is recommended to set the HBSEL to zero.

Table 2. SPI OUTPUT DATA FRAME

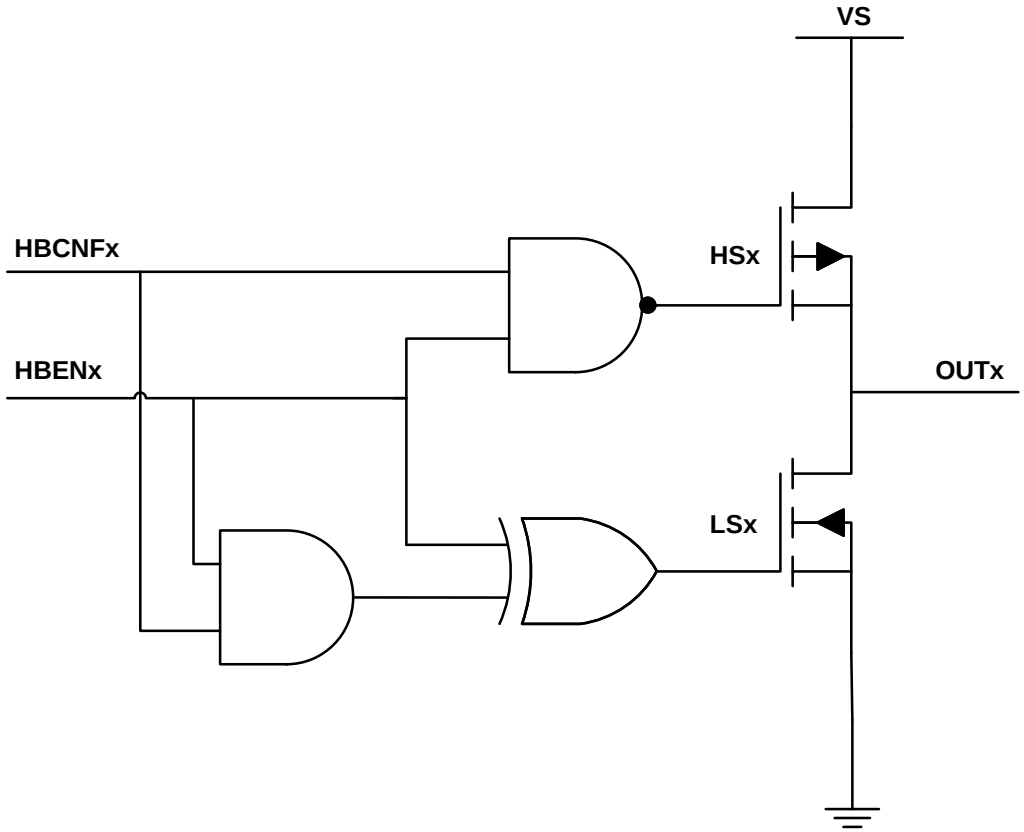
Output Data			
Bit Number	**Bit Name**	**Bit Description**	**Bit Status**
PRE_15	TSD	Latched Thermal Shutdown	0 = No Fault
			1 = Fault
15	OCS	Over Current Shutdown Global Notification	0 = No Fault
			1 = Fault
14	PSF	Power Supply Failure on VS1 and/or VS2 Under Voltage and Over Voltage Monitoring	0 = No Fault
			1 = Fault
13	ULD	Under Load Detection Global Notification	0 = No Fault
			1 = Fault
12	HBST6	Half Bridge 6 Enable Status	0 = High Z
			1 = Enabled
11	HBST5	Half Bridge 5 Enable Status	0 = High Z
			1 = Enabled
10	HBST4	Half Bridge 4 Enable Status	0 = High Z
			1 = Enabled
9	HBST3	Half Bridge 3 Enable Status	0 = High Z
			1 = Enabled
8	HBST2	Half Bridge 2 Enable Status	0 = High Z
			1 = Enabled
7	HBST1	Half Bridge 1 Enable Status	0 = High Z
			1 = Enabled
6	HBCR6	Half Bridge 6 Configuration Reporting	0 = LS6 ON & HS6 OFF
			1 = LS6 OFF & HS6 ON
5	HBCR5	Half Bridge 5 Configuration Reporting	0 = LS5 ON & HS5 OFF
			1 = LS5 OFF & HS5 ON
4	HBCR4	Half Bridge 4 Configuration Reporting	0 = LS4 ON & HS4 OFF
			1 = LS4 OFF & HS4 ON
3	HBCR3	Half Bridge 3 Configuration Reporting	0 = LS3 ON & HS3 OFF
			1 = LS3 OFF & HS3 ON
2	HBCR2	Half Bridge 2 Configuration Reporting	0 = LS2 ON & HS2 OFF
			1 = LS2 OFF & HS2 ON
1	HBCR1	Half Bridge 1 Configuration Reporting	0 = LS1 ON & HS1 OFF
			1 = LS1 OFF & HS1 ON
0	TW	Thermal Warning Global Notification	0 = No Fault
			1 = Fault

If the half−bridge enable status denotes a high impedance condition (HBSTx = 0), the corresponding half−bridge configuration reporting (HBCRx) should be ignored. The latched thermal shutdown (TSD) information is available on SO after CSB goes low until the first rising SCLK edge. The following procedures must be met for a true TSD reading:

1. SCLK and SI are low before the CSB cycle. Violating these conditions will results in an undetermined SPI behavior or/and an incorrect TSD reading.
2. CSB transitioning from high to low.
3. CSB setup time (TcsbSup) is satisfied and the data is captured before the first SCLK rising edge.

Driver Control

The NCV7718B/C has the flexibility of controlling each driver through the 16 bit SPI frame (Bits 12−1) and the logic combination required for bridge control is defined in Figure 14.



HBENx	HBCNFx	OUTx
0	'X'	OUTx in High Impedance State
1	0	HSx Off and LSx On
1	1	HSx On and LSx Off

'X' = Don't Care

Figure 14. Bridge Control Logic

The digital design insures that the high side and low side of the same half bridge will not be active at the same time. Thus the device self protects from a current shoot through condition. Delays (ThsOffLsOn and TlsOffHsOn) between the high side and low side switching are implemented for same reasons.

Frame Detection

To maintain the data integrity, the NCV7718B/C has 16 bit frame detection. A valid frame for a single CSB cycle requires 16 bits to be clocked into SI for the initial 16 bits and *n* x 8 bits thereafter. In an instance of an invalid SPI frame the entire frame is ignored, but the previous states of the corresponding outputs are maintained.

Daisy Chain Operation

Daisy chain communications between multiple of 8−bit SPI compatible IC's is possible by connection of the serial output pin (SO) to the input of the sequential IC (SI). The clock phase and clock polarity respect to the data must be the same for all the devices on the chain. Figure 15 illustrates the hardware configuration of NCV7718B/C daisy chained with a *n*8* bit (ie n = 2; 16 bit) SPI device. The progression of data from the MCU through the sequential devices is also shown. Strict adherence to the frame format illustrated in Figure 16 is required for the proper serial daisy chain operations.

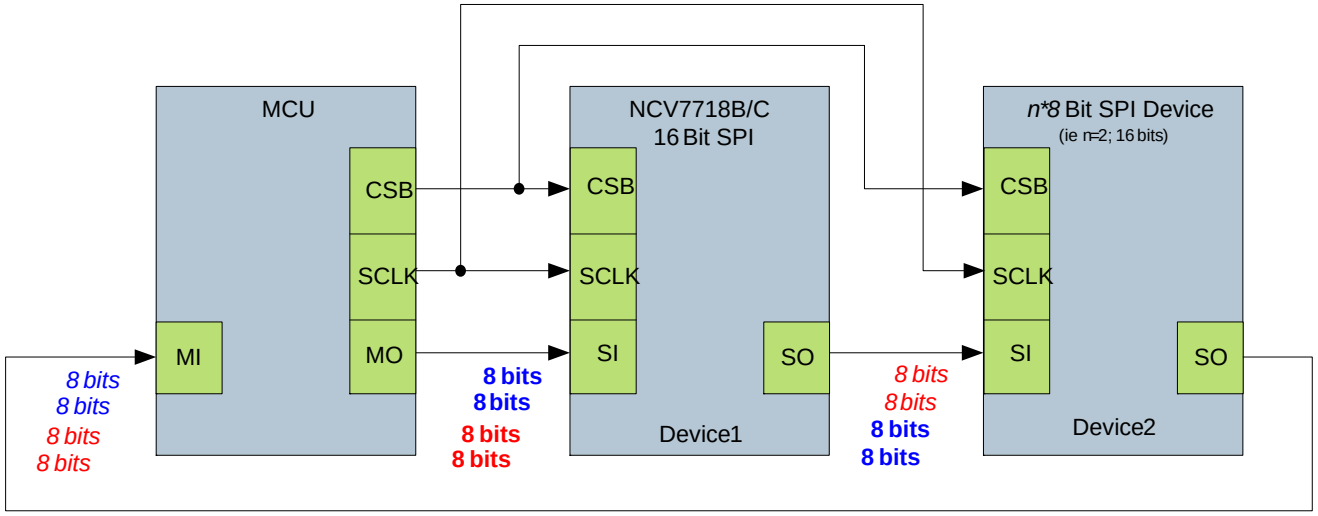


Figure 15. Serial Daisy Chain

If Device 2 is a 16 bit IC, then a total of 32 bits must be generated from the MCU for a complete transport of data in the system. Monitoring of all the devices in the serial chain must be employed on a system level architecture. Thus, pre−cautious measure should be taken to avoid situations where not enough frames were sent to the devices, but the frames transmitted did not violate the internal frame detection counters. For these scenarios, invalid data is accepted by NCV7718B/C and possibly by other devices on the chain depending on their frame detection design. The data shifted in will be transferred to the data registers of the devices on the beginning of the chain and the devices at the end of the chain will get the previous diagnostic data of the preceding devices.

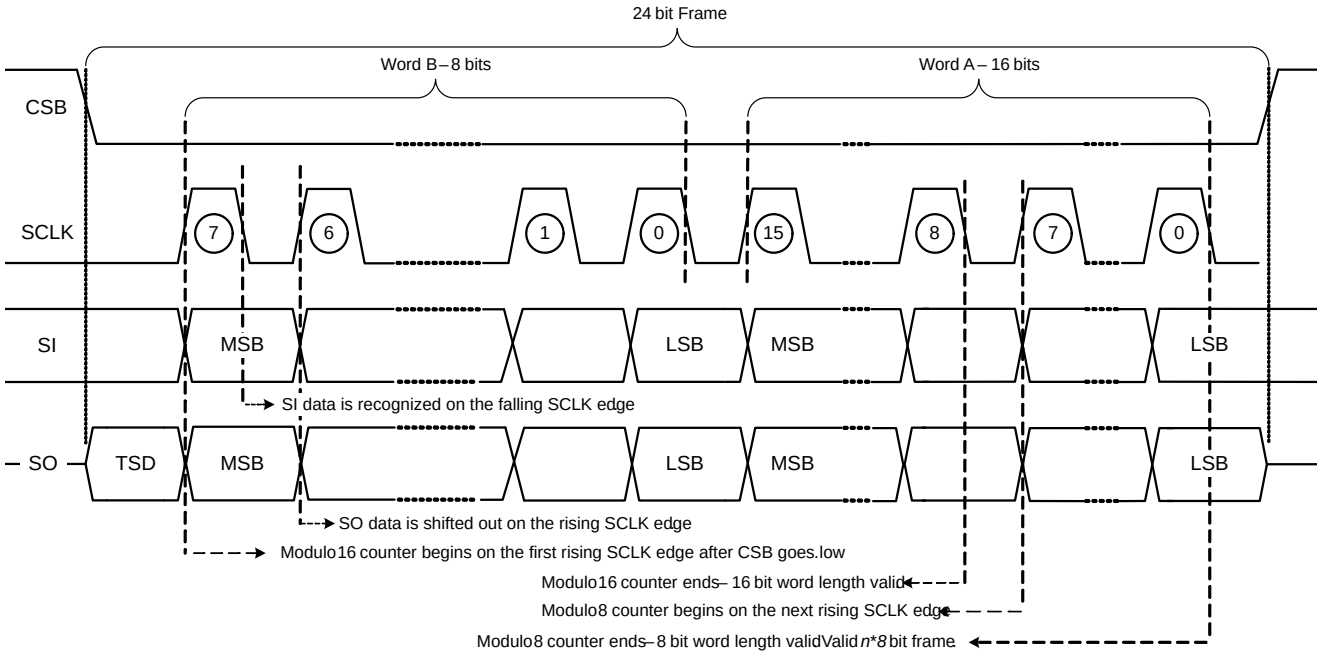


Figure 16. SPI Data Recognition and Frame Detection

The TSD bit is multiplexed with the SPI SO data and OR'd with the SI input (Figure 17) to allow for reporting in a serial daisy chain configuration in devices with the same SPI protocol. A TSD error bit as a "1" automatically propagates through the serial daisy chain circuitry from the SO output of one device to the SI input of the next. This is shown in Figures 18 and 19; first as the daisy chained devices connected with no thermal shutdown latched fault (Figure 18) and subsequently with a TSD fault in device 1 propagating through to device 2 (Figure 19).

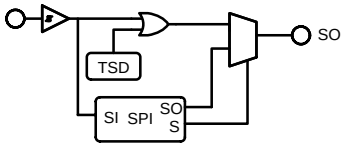


Figure 17. TSD SPI Link

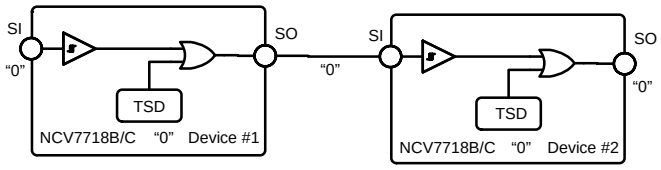


Figure 18. Daisy Chain No TSD Fault

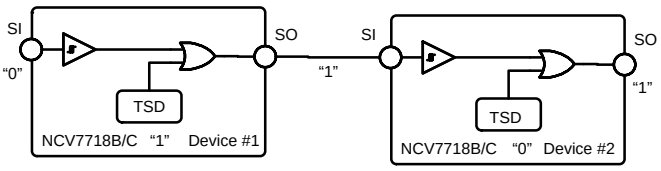


Figure 19. Daisy Chain TSD Error Propagation

DEVICE PROTECTION, DIAGNOSTICS AND FAULT REPORTING

Power Up/Down Control

Each analog power pin (VS1 or VS2) powers their respective output drivers. After a device has powered up and the output drivers are allowed to turn on, the output drivers will not turn off until the voltage on the supply pins is reduced below the initial under voltage threshold, exceeds the over voltage threshold or if shut down by either a SPI command or a fault condition.

Internal power−up circuitry on the logic supply pin supports a smooth turn on transition. VCC power up resets the internal logic such that all output drivers will be off as power is applied. All the internal counters, SI and SO along with all the digital registers will be cleared on VCC POR. Exceeding the under voltage lockout threshold on VCC allows information to be input through the SPI port for turn on control. Logic information remains intact over the entire VS1 and VS2 voltage range.

Under Voltage Shutdown

An under voltage lockout circuit prevents the output drivers from turning on unintentionally. This control is provided by monitoring the voltages on the VS1, VS2 and VCC pins. A built−in hysteresis on the under voltage threshold is included to prevent an unknown region on the power pins; VCC, VS1 and VS2. When the VCC goes below the threshold, all outputs are turned off and the input and output registers are cleared.

An under voltage condition on the VSx pins will result in shutting off all the drivers and the status bit 14 (PSF) will be set. The SPI port remains active during a VSx under−voltage if proper VCC voltage is supplied. Also all driver states will be maintained in the logic circuitry with the valid VCC voltage. Once the input voltage VSx is above the under voltage threshold level the drivers will return to programmed operation and the PSF output register bit is cleared.

Under−voltage timing diagram is provided in Figure 20.

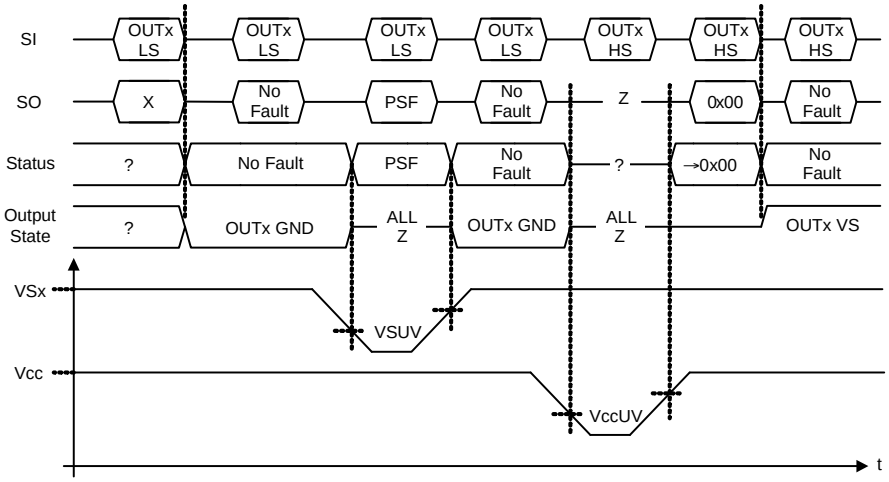


Figure 20. Under−Voltage Timing Diagram

Over Voltage Shutdown

Over voltage shutdown circuitry monitors the voltage on the VS1 and VS2 pins, which permits a 40 V maximum. When the Over−voltage Threshold level has been breached on the VS1or VS2 supply input, the output bit 14 (PSF) will be set. Additionally, if the input bit 0 (OVLO) is asserted, all outputs will turn off. During an Over Voltage Lockout condition the turn on/off status is maintained in the logic circuitry. When proper input voltage levels are re−established, the programmed outputs will turn back on. Over−voltage shutdown can be disabled by using the SPI input bit 0 (OVLO = 0) to run through a load dump situation. It is highly recommended to operate the part with OVLO bit asserted to ensure that the drivers remain off during a load dump scenario.

The table below describes the driver status when enabling/disabling the over voltage lock out feature during normal and overvoltage situations.

Table 3. OVER−VOLTAGE LOCK OUT (OVLO)

OVLO Input Bit	VSx OVLO Condition	Output Data Bit 14 Power Supply Fail (PSF) Status	OUTx Status
0	0	‘0’	Not in Overvoltage Outputs Unchanged
0	1	‘1’ (Clears when VSx within Operating Range)	In Overvoltage → Outputs Unchanged
1	0	‘0’	Not in Overvoltage Outputs Unchanged
1	1	‘1’ (Clears when VSx within Operating Range)	All Outputs Off (Remain off until VSx is out of OVLO)

Over−voltage timing diagram is provided in Figure 21.

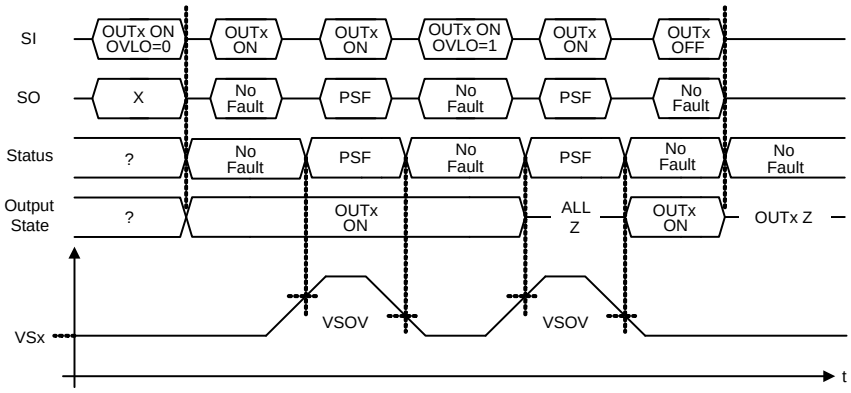


Figure 21. Over−Voltage Timing Diagram

Over Current Detection and Shutdown

The NCV7718B/C offers over current shutdown protection on the OUTx pins by monitoring the current on the high side and low side drivers. If the over current threshold is breached, the corresponding output is latched off (HS and LS driver is latched off) after the specified shutdown time, TdOc. Upon over current shutdown, the serial output bit OCS will be set and the corresponding HBx[1:0] will be changed to “01” to denote a high power dissipation state. Devices can be turned back on via the SPI port once the OCS condition is cleared by setting the SRR to ‘1’ on the next SPI command. The event triggering the over current shutdown condition must be resolved prior to clearing the OCS bit to avoid repetitive stress on the drivers. Failure to do so may result in non reversible fatal damage.

The SO data OCS shown on Figure 22 corresponds to both the global SO bit #15 and the HBx OCS encoding state ‘01’.

Note: high currents could cause a high rise in die temperature. Devices will turn off if the die temperature exceeds the thermal shutdown temperature.

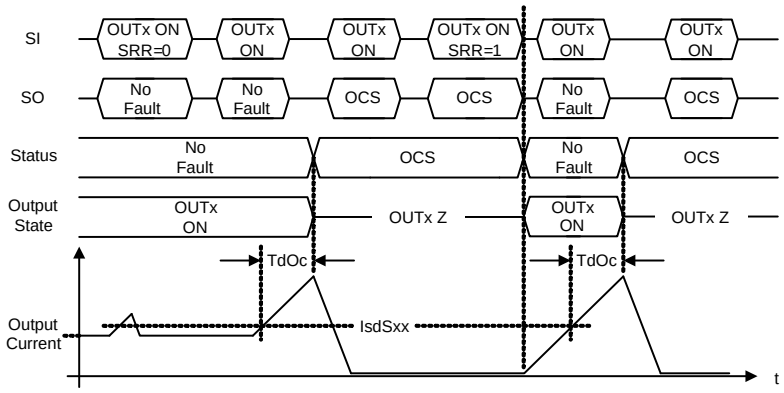


Figure 22. Over−Current Timing Diagram

Under Load Detection

The under−load detection is accomplished by monitoring the current from the low side drivers and one global output bit is used for under load fault reporting. A minimum load current (IuldLS − this is the maximum open circuit detection threshold) is required when the drivers are turned on to avoid an under−load condition. If the under−load detection threshold has been breached longer than the specified under−load timer (TdUld), the ULD output bit is set to ‘1’. Furthermore, if the Under−Load Detection Shutdown Control (ULDSC bit # 13) input bit is set then the offending half−bridge output will be turned off (HS and LS on the driver will be latched off).

There is only one global under load timer for all the drivers. If the TdUld timer is already activated due to one under load, any subsequent under load delays will be the remainder of the TdUld timer.

Table 4. UNDER−LOAD DRIVER STATUS

ULDSC Input Bit 13	OUTx ULD Condition	Output Data Bit Under Load Detect Status	OUTx Status
0	0	‘0’	Unchanged
0	1	‘1’ (Need SRR to reset)	Unchanged
1	0	‘0’	Unchanged
1	1	‘1’ (Need SRR to reset)	OUTx Latches off (Need SRR to reset)

The ULD SO data provided in the under load timing diagram in Figure 24 reflects the global ULD SO bit #13 and the HBx ULD encoding state ‘10’.

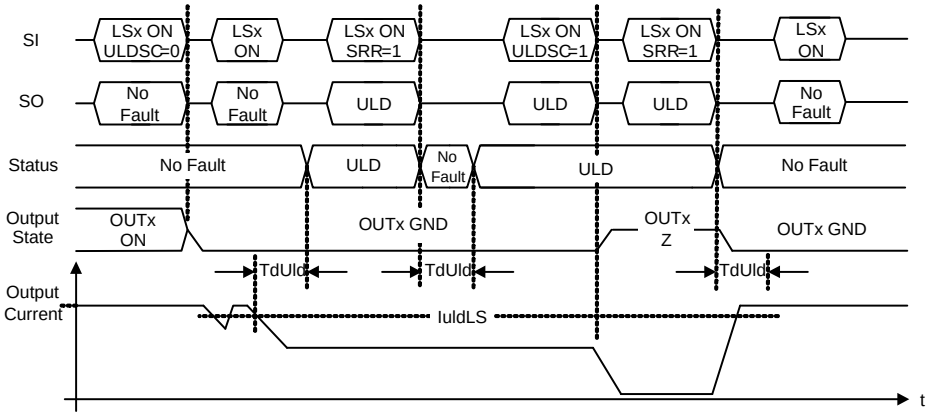


Figure 23. LS Under−load Timing Diagram

Thermal Warning and Thermal Shutdown

The NCV7718B/C provides individual thermal sensors for each half−bridge. Moreover, the sensor reports over temperature warning level and an over temperature shutdown level. The TW status bit (output bit 0) will be set if the temperature exceeds the over temperature warning level, but the drivers will remain active. Once the IC temperature fall below the thermal warning threshold the TW flag is automatically clearly. If any of the individual thermal sensors detects a thermal shutdown level then the drivers on the offending half bridge are latched off. The TSD (PRE_15) bit is set to capture a thermal shutdown event. A valid SPI command with SRR and temperature below the Tsd threshold are required to clear the latched fault. Since thermal warning precedes an over temperature shutdown, software polling of this bit will allow load control and possible prevention of over temperature shutdown conditions.

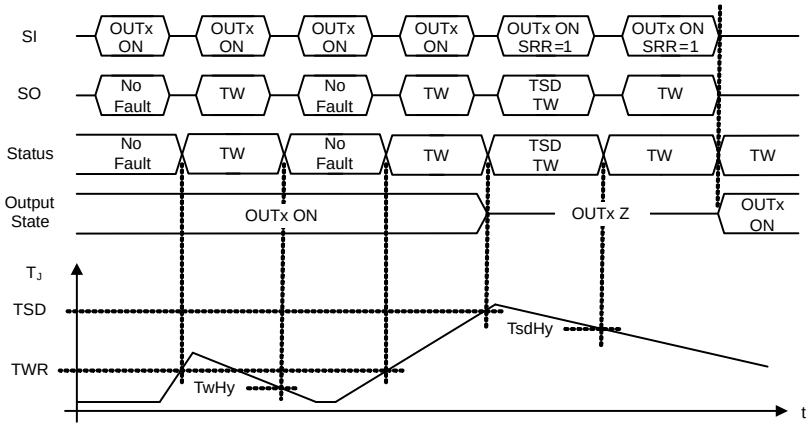


Figure 24. Thermal Warning and Shutdown Timing Diagram

Thermal Performance

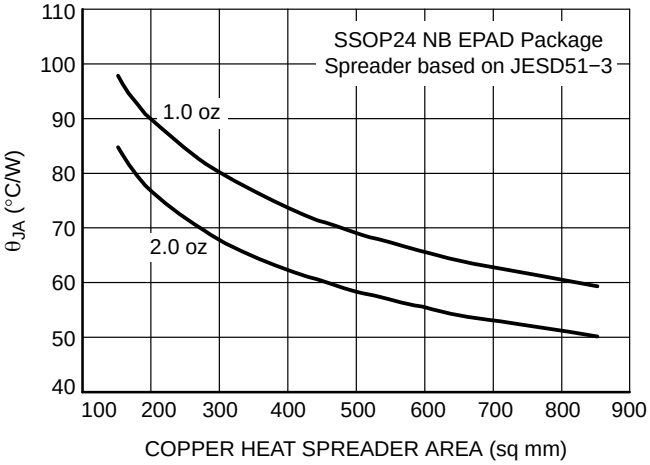


Figure 25. θ_{JA} vs. Cu Area: SSOP24 NB EP

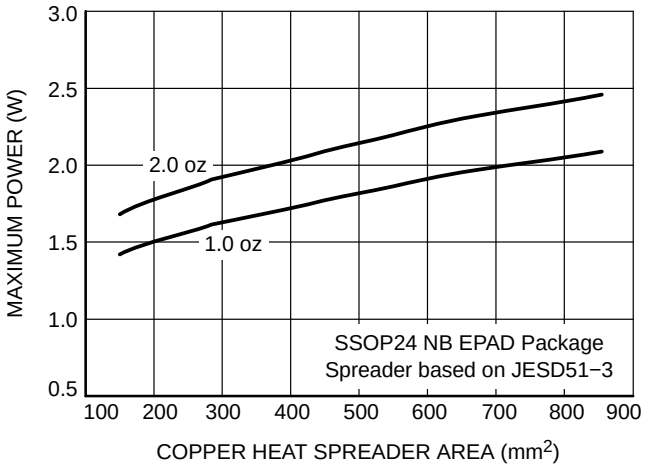


Figure 26. Power vs. Cu Area: SSOP24 NB EP

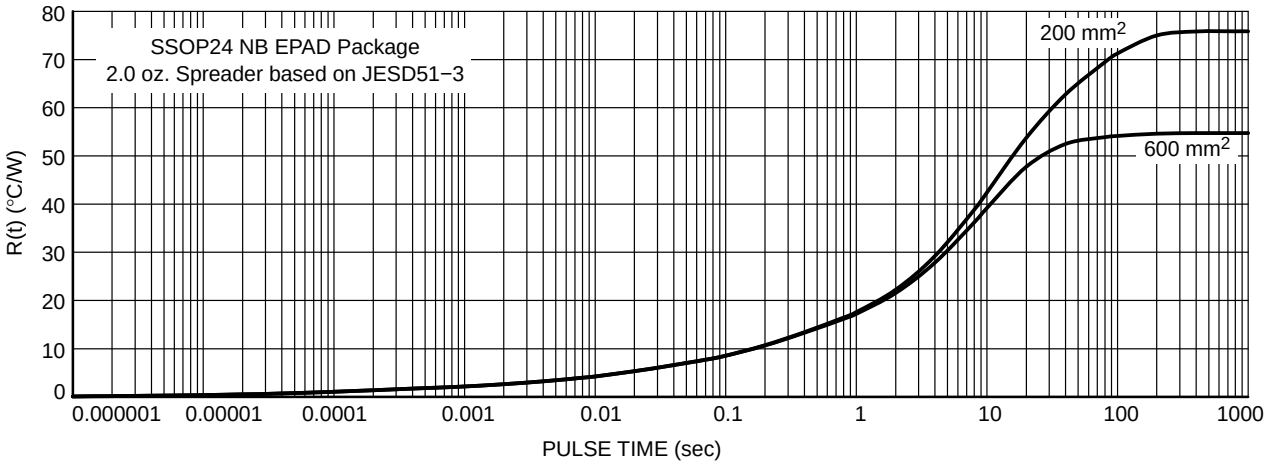


Figure 27. R(t) vs. Duty Cycle: SSOP24 NB EP

Thermal Performance

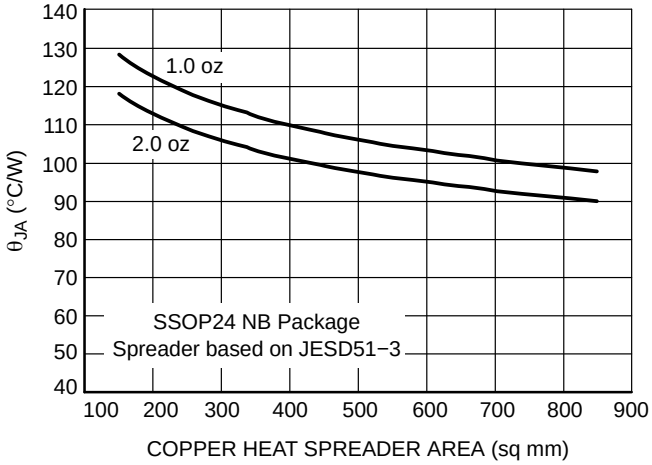


Figure 28. θ_{JA} vs. Cu Area: SSOP24 NB

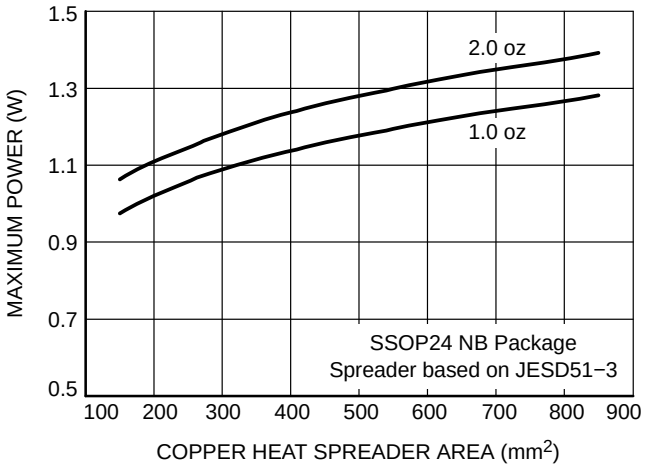


Figure 29. Power vs. Cu Area: SSOP24 NB

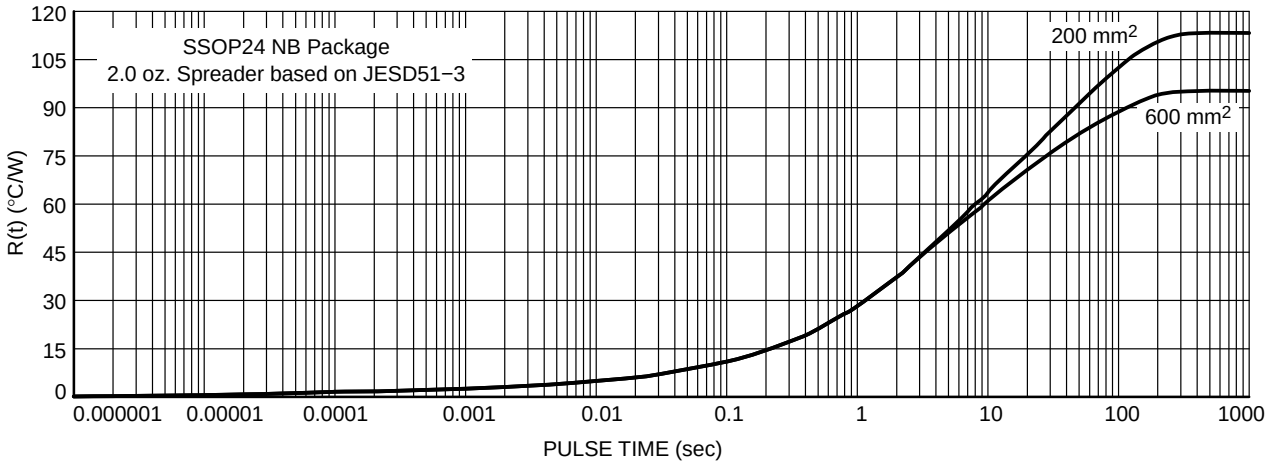


Figure 30. R(t) vs. Duty Cycle: SSOP24 NB

Fault Handling

At an event of a driver latched off fault, the offending half−bridge driver is disabled and the half−bridge configuration is defaulted to zero (HBENx =0, HBCNFx = 0). The user is required to clear the output register fault and to resend the proper SPI frame to turn on the drivers. A driver that is locked out during a fault conditions auto recovers to the previous programmed state when the fault is resolved. A latched fault flag on the serial output doesn't always translate an output latched off fault.

The summary of all fault conditions, the driver status and the clear requirements are provided in Table 5.

Table 5. FAULT SUMMARY

Fault	Fault Memory Serial Output Bit	Driver Condition During Fault	Driver Condition after Parameters Within Specified Limits	Output Register Clear Requirement
Under Load (ULDSC = 0)	Latched	Outputs Unchanged. Allowed to turn/ remain on	Allowed to turn/remain on	Valid SPI frame with SRR set to 1
Under Load (ULDSC = 1)	Latched (Note 9)	Offending Half−Bridge is Latched Off (LS and HS)	Offending Half−Bridge is Latched Off (LS and HS)	Valid SPI frame with SRR set to 1
Over Current	Latched (Note 9)	Offending Output is Latched Off (LS and HS)	Offending Output is Latched Off (LS and HS)	Valid SPI frame with SRR set to 1
Thermal Warning	Non−Latched	Outputs Unchanged. Allowed to turn/ remain on provided that device is not in thermal shutdown	Allowed to turn/remain on	Temp below (thermal warning temp – hysteresis)
Thermal Shutdown	Latched (Note 9)	Offending Half−Bridge Drivers are Latched Off (LS and HS)	Offending Half−Bridge is Latched Off (LS and HS)	Valid SPI frame with SRR set to 1. Temperature blow (thermal shutdown − hysteresis)
VS Power Supply Fail (Over−Voltage: OVLO = 0)	Non−Latched	Outputs Unchanged. Allowed to turn/ remain on	Allowed to turn/remain on	VS below (Over Voltage Threshold – hysteresis)
VS Power Supply Fail (Over−Voltage: OVLO = 1)	Non−Latched	All Drivers are Locked Out. Outx → High Z	Previous Half−Bridge status and driver configuration is maintained. Allowed to turn/remain on	Auto Recovers if the VS voltage is below overvoltage threshold
VS Power Supply Fail (Under Voltage)	Non−Latched	All Drivers are Locked Out. Outx → High Z	Previous Half−Bridge status and driver configuration is maintained. Allowed to turn/remain on	Auto Recovers if the VS voltage is above the Under Voltage threshold

9. Latched conditions are cleared via the SPI SRR input bit = 1, by cycling the EN pin or with a power−on reset of V_{CC}.

APPLICATION DIAGRAM

The application drawing below demonstrates the drive capability of the NCV7718B/C. The VS1 and VS2 pins must be tied together to avoid any potential difference in the supply voltage.

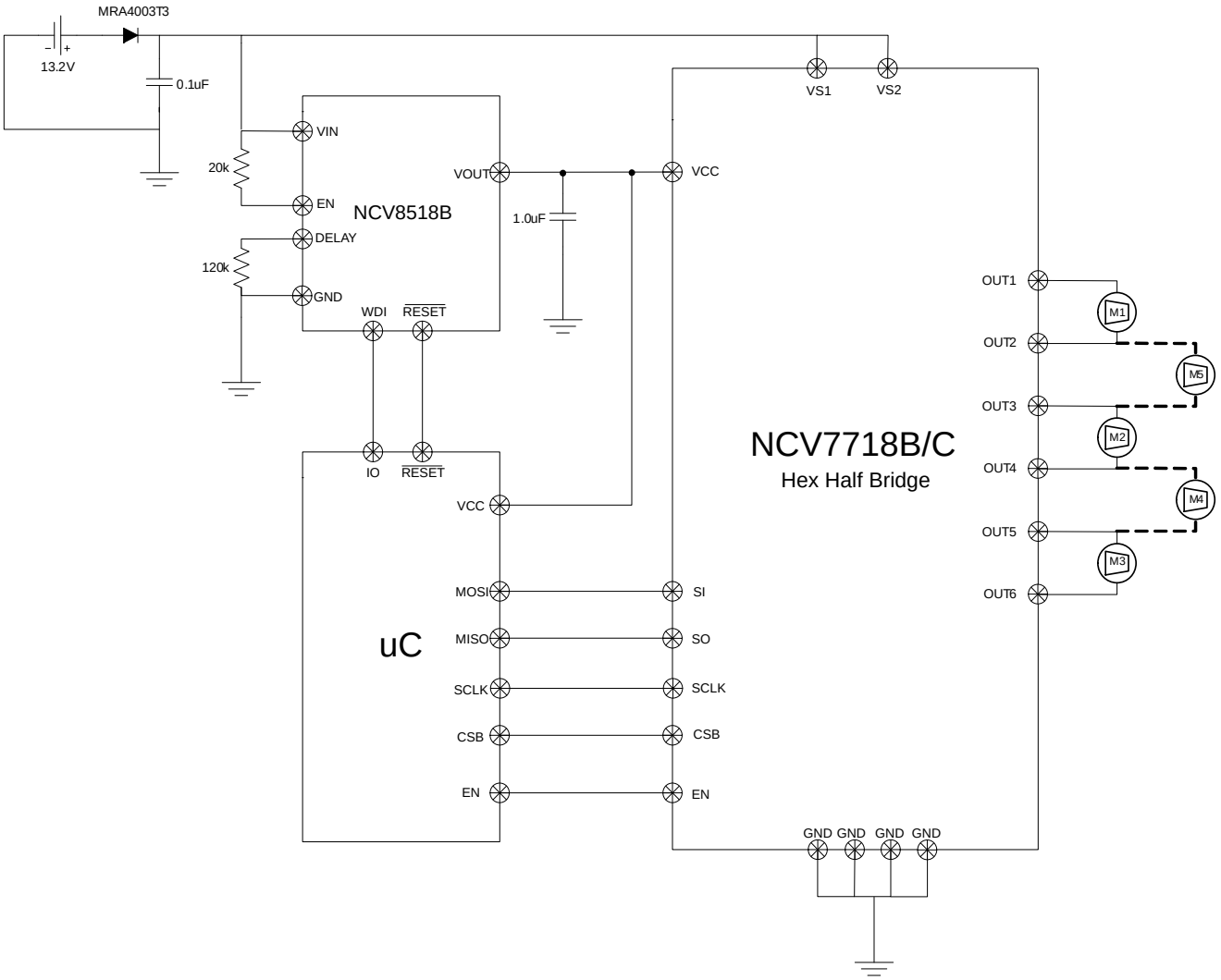


Figure 31. Application Drawing

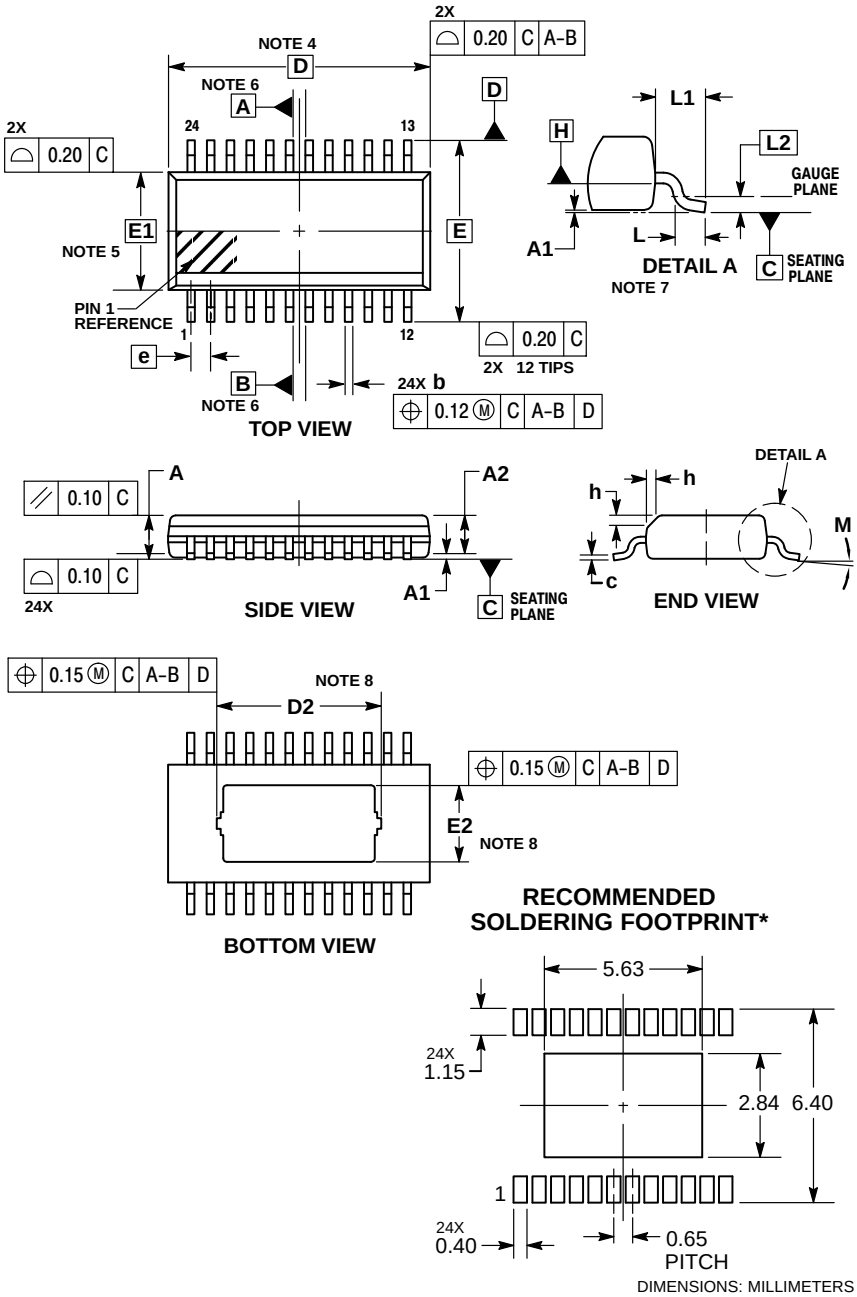
ORDERING INFORMATION

Device	Package	Shipping†
NCV7718BDQR2G	SSOP24 NB EP (Pb−Free)	2500 / Tape & Reel
NCV7718CDPR2G	SSOP24 NB (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SSOP24 NB EP
CASE 940AK
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
A2	1.10	1.65
b	0.19	0.30
c	0.09	0.20
D	8.64 BSC	
D2	5.28	5.58
E	6.00 BSC	
E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°

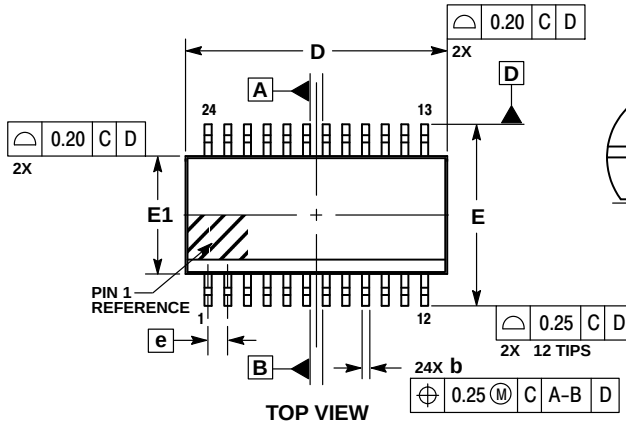
RECOMMENDED SOLDERING FOOTPRINT*

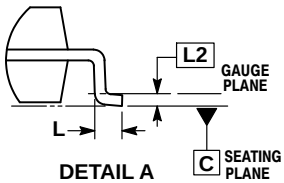
DIMENSIONS: MILLIMETERS

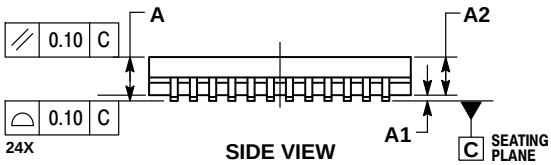
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

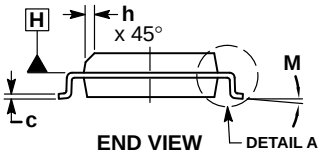
PACKAGE DIMENSIONS

SSOP24 NB
CASE 565AL−01
ISSUE O





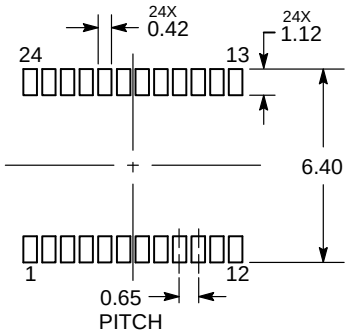




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INLCUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.20	0.30
c	0.19	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.65 BSC	
h	0.22	0.50
L	0.40	1.27
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT



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