NCP502, NCP502A

80 mA CMOS Low Iq, Low-Dropout Voltage Regulator

The NCP502/A series of fixed output linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP502/A series features an ultra−low quiescent current of 40 μA. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

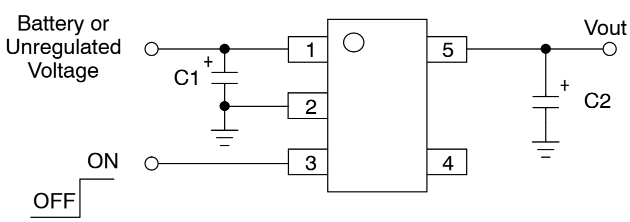
The NCP502/A has been designed to be used with low cost ceramic capacitors. The device is housed in the micro−miniature SC70−5 and TSOP−5 surface mount packages. Standard voltage versions are 1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 3.3 V, 3.4 V, 3.5 V, 3.6 V, 3.7 V and 5.0 V. Other voltages are available in 100 mV steps.

Features

- Low Quiescent Current of 40 μA Typical
- Excellent Line and Load Regulation
- Low Output Voltage Option
- Output Voltage Accuracy of 2.0%
- Industrial Temperature Range of −40°C to 85°C
- NCP502: 1.3 V Enable Threshold High, 0.3 V Enable Threshold Low
- NCP502A: 1.0 V Enable Threshold High, 0.4 V Enable Threshold Low
- These are Pb−Free Devices

Typical Applications

- Cellular Phones
- Battery Powered Consumer Products
- Hand−Held Instruments
- Camcorders and Cameras



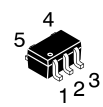
This device contains 86 active transistors

Figure 1. Typical Application Diagram

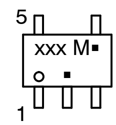
ON Semiconductor®

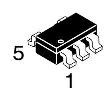
http://onsemi.com

MARKING DIAGRAM

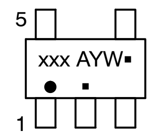


SC70−5
SQ SUFFIX
CASE 419A





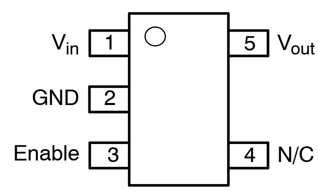
TSOP−5
(SOT23−5, SC59−5)
SN SUFFIX
CASE 483



xxx	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
M	= Date Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{in}	Positive power supply input voltage.
2	GND	Power supply ground.
3	Enable	This input is used to place the device into low−power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to Vin.
4	N/C	No internal connection.
5	V_{out}	Regulated output voltage.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	12	V
Enable Voltage	Enable	−0.3 to V_{in} +0.3	V
Output Voltage	V_{out}	−0.3 to V_{in} +0.3	V
Power Dissipation and Thermal Characteristics Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Latchup capability (85°C) ±100 mA DC with trigger voltage.

THERMAL CHARACTERISTICS

Rating	Symbol	Test Conditions	Value	Unit
Thermal Characteristics, TSOP−5 (Note 2) Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	1 oz Copper Thickness, 100 mm^2	205	°C/W
Thermal Resistance, Junction−to−Ambient, SC70−5	$R_{\theta JA}$		400	W °C/W

NOTE: Single component mounted on a 80 x 80 x 15 mm FR4 PCB with stated copper head spreading area. Using the following boundary conditions as stated in EIA/JESD 51−1, 2, 3, 7, 12.

2. True no connect. Printed circuit board traces are allowable.
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V..

ELECTRICAL CHARACTERISTICS (V_{in} = $V_{out(nom.)}$ + 2.0 V, V_{enable} = V_{in}, C_{in} = 1.0 μF, C_{out} = 1.0 μF, T_J = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_A = 25°C, I_{out} = 10 mA) V_{in} = V_{out} (nom.) +1.0 V	V_{out}				V
1.5 V		1.455	1.5	1.545	
1.8 V		1.746	1.8	1.854	
2.5 V		2.425	2.5	2.575	
2.7 V		2.646	2.7	2.754	
2.8 V		2.744	2.8	2.856	
2.9 V		2.842	2.9	2.958	
3.0 V		2.94	3.0	3.06	
3.1 V		3.038	3.1	3.162	
3.3 V		3.234	3.3	3.366	
3.4 V		3.332	3.4	3.468	
3.5 V		3.43	3.5	3.57	
3.6 V		3.528	3.6	3.672	
3.7 V		3.626	3.7	3.774	
5.0 V		4.900	5.0	5.100	
Output Voltage (T_A = −40°C to 85°C, I_{out} = 10 mA) V_{in} = V_{out} (nom.)	V_{out}				V
1.5 V		1.455	1.5	1.545	
1.8 V		1.746	1.8	1.854	
2.5 V		2.425	2.5	2.575	
2.7 V		2.619	2.7	2.781	
2.8 V		2.716	2.8	2.884	
2.9 V		2.813	2.9	2.987	
3.0 V		2.910	3.0	3.09	
3.1 V		3.007	3.1	3.193	
3.3 V		3.201	3.3	3.399	
3.4 V		3.298	3.4	3.502	
3.5 V		3.43	3.5	3.57	
3.6 V		3.528	3.6	3.672	
3.7 V		3.626	3.7	3.774	
5.0 V		4.900	5.0	5.100	
Line Regulation (V_{in} = V_{out} + 1.0 V to 12 V, I_{out} = 10 mA)	Reg_{line}	–	0.4	3.0	mV/V
Load Regulation (I_{out} = 1.0 mA to 80 mA)	Reg_{load}	–	0.2	0.8	mV/mA
Output Current (V_{out} = (V_{out} at I_{out} = 80 mA) −3%)	$I_{o(nom.)}$	80	180	–	mA
Dropout Voltage (T_A = −40°C to 85°C, I_{out} = 80 mA, Measured at V_{out} −3.0%)	V_{in}−V_{out}				mV
1.5 V−1.7 V		–	1500	1900	
1.8 V−2.4 V		–	1300	1700	
2.5 V−2.6 V		–	1000	1400	
2.7 V−2.9 V		–	850	1300	
3.0 V−4.0 V		–	850	1200	
4.1 V−5.0 V		–	600	900	
Quiescent Current	I_Q				μA
(Enable Input = 0 V)		–	0.1	1.0	
(Enable Input = V_{in}, I_{out} = 1.0 mA to $I_{o(nom.)}$)		–	40	90	
Output Short Circuit Current (V_{out} = 0 V)	$I_{out(max)}$	90	200	500	mA
Ripple Rejection (f = 1.0 kHz, 15 mA)	RR	–	55	–	dB
Output Voltage Noise (f = 100 Hz to 100 kHz)	V_n	–	180	–	μVrms
Enable Input Threshold Voltage (NCP502)	$V_{th(en)}$				V
(Voltage Increasing, Output Turns On, Logic High)		1.3	–	–	
(Voltage Decreasing, Output Turns Off, Logic Low)		–	–	0.3	
Enable Input Threshold Voltage (NCP502A)	$V_{th(en)}$				V
(Voltage Increasing, Output Turns On, Logic High)		1.0	–	–	
(Voltage Decreasing, Output Turns Off, Logic Low)		–	–	0.4	
Output Voltage Temperature Coefficient	T_C	–	100	–	ppm/°C

4. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

5. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

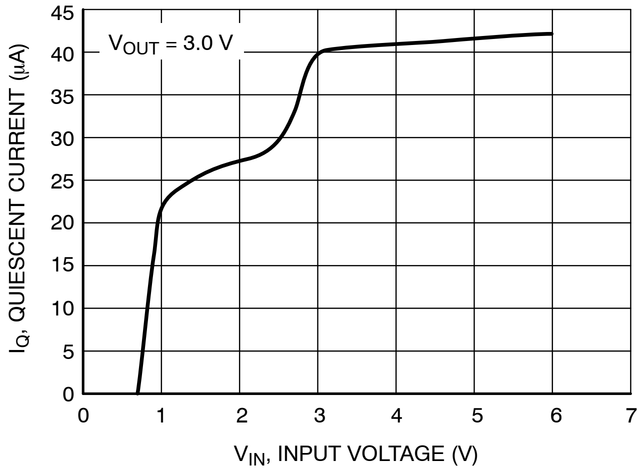


Figure 2. Quiescent Current versus Input Voltage

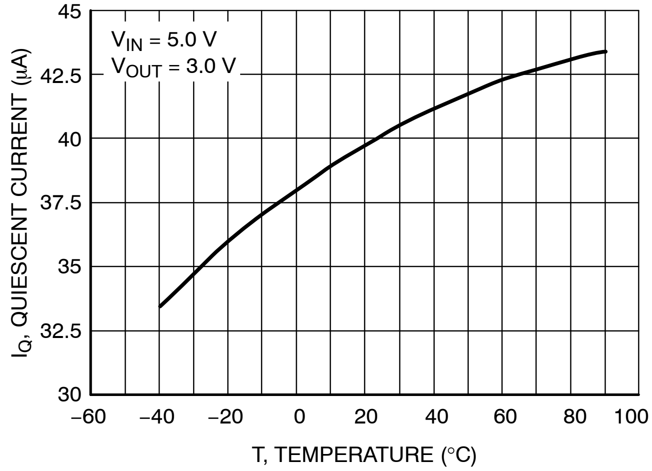


Figure 3. Quiescent Current versus Temperature

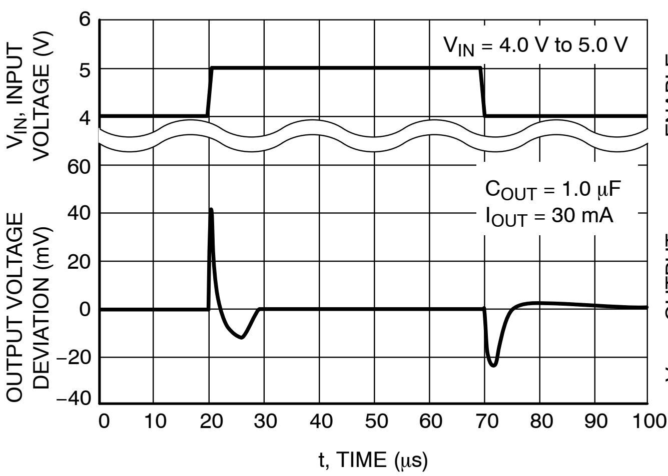


Figure 4. Line Transient Response

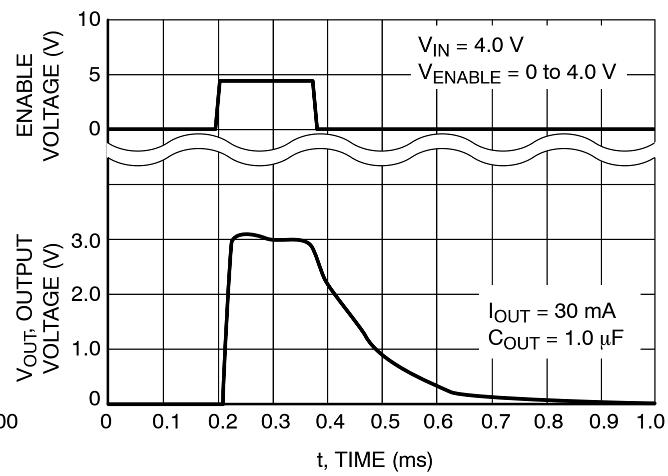


Figure 5. Enable Response

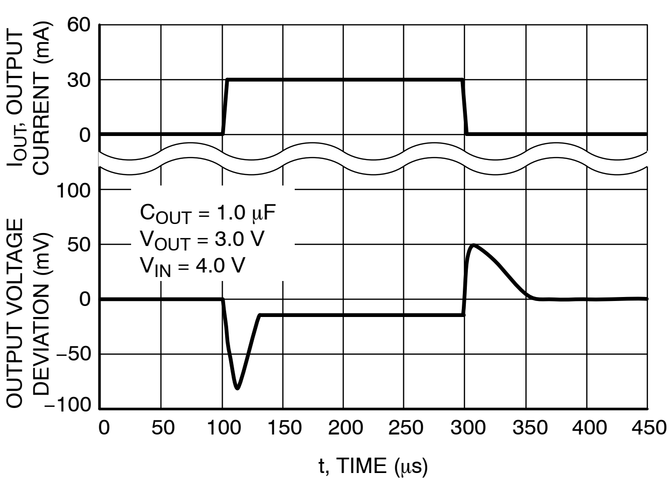


Figure 6. Load Transient Response

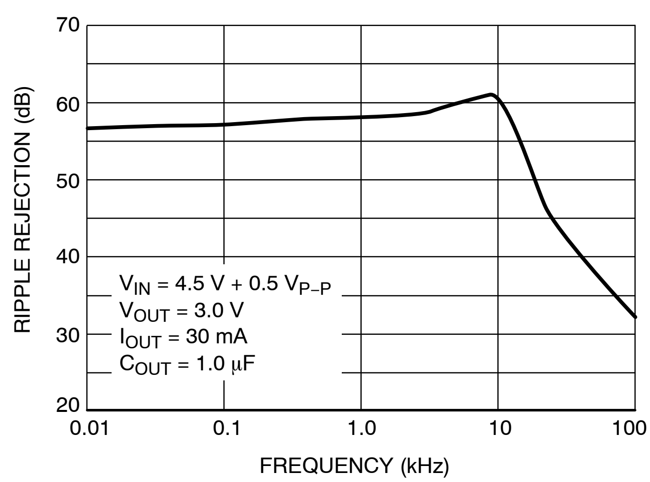


Figure 7. Ripple Rejection/Frequency

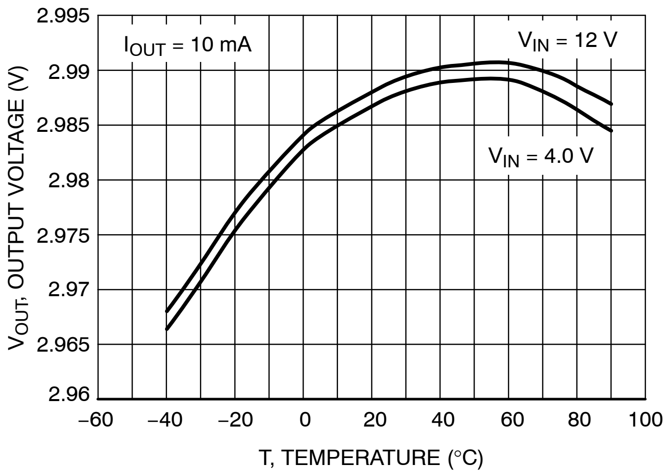


Figure 8. Output Voltage versus Temperature

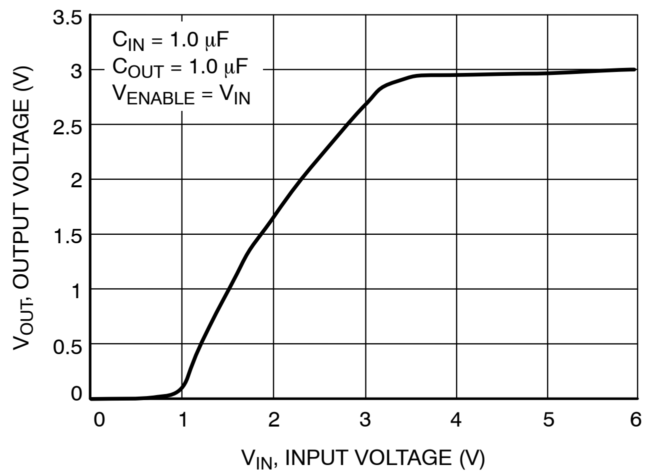


Figure 9. Output Voltage versus Input Voltage

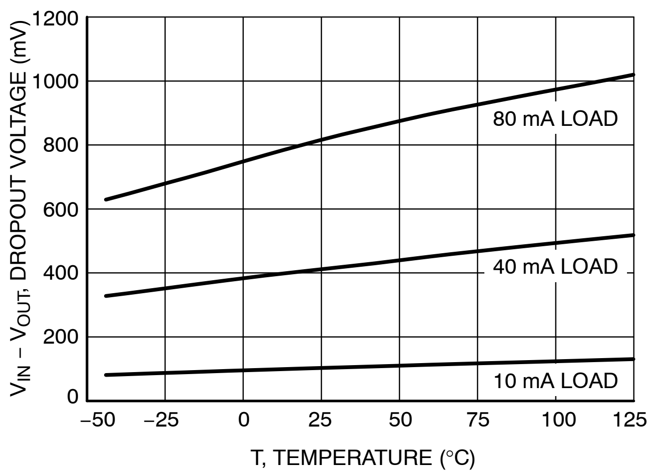


Figure 10. Dropout Voltage versus Temperature

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3.0% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient power dissipation and thus the maximum available output current.

APPLICATIONS INFORMATION

A typical application circuit for the NCP502/A series is shown in Figure 1, front page.

Input Decoupling (C1)

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP502/A package. Higher values and lower ESR will improve the overall line transient response. If large line or load transients are not expected, then it is possible to operate the regulator without the use of a capacitor.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

Output Decoupling (C2)

The NCP502/A is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 5.0 Ω can thus safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to V_{in}.

Hints

Please be sure the Vin and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Thermal

As power across the NCP502/A increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP502/A has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum 125°C, then the NCP502/A can dissipate up to 250 mW @ 25°C.

The power dissipated by the NCP502/A can be calculated from the following equation:

$$P_{tot} = \left[V_{in} * I_{gnd}\,(I_{out})\right] + [V_{in} - V_{out}] * I_{out}$$

or

$$V_{inMAX} = \frac{P_{tot} + V_{out} * I_{out}}{I_{gnd} + I_{out}}$$

If an 80 mA output current is needed then the ground current from the data sheet is 40 μA. For an NCP502/A (3.0 V), the maximum input voltage will then be 6.12 V.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP502SQ15T1G	1.5	LCC	SC70−5 (Pb−Free)	3000 / Tape & Reel
NCP502SQ15T2G				
NCP502SQ18T1G	1.8	LCD		
NCP502SQ18T2G				
NCP502SQ25T1G	2.5	LCE		
NCP502SQ25T2G				
NCP502SQ27T1G	2.7	LCF		
NCP502SQ27T2G				
NCP502SQ28T1G	2.8	LCG		
NCP502SQ28T2G				
NCP502SQ29T1G	2.9	LJI		
NCP502SQ29T2G				
NCP502SQ30T1G	3.0	LCH		
NCP502SQ30T2G				
NCP502SQ31T1G	3.1	LJJ		
NCP502SQ31T2G				
NCP502SQ33T1G	3.3	LCI		
NCP502SQ33T2G				
NCP502SQ34T1G	3.4	LJK		
NCP502SQ34T2G				
NCP502SQ35T1G	3.5	LGO		
NCP502SQ35T2G				
NCP502SQ36T1G	3.6	LIU		
NCP502SQ36T2G				
NCP502SQ37T1G	3.7	LJQ		
NCP502SQ37T2G				
NCP502SQ50T1G	5.0	LCJ		
NCP502SQ50T2G				
NCP502ASQ15T1G	1.5	LGP		
NCP502ASQ18T1G	1.8	LGQ		
NCP502ASQ25T1G	2.5	LGR		
NCP502ASQ27T1G	2.7	LGS		
NCP502ASQ28T1G	2.8	LGT		
NCP502ASQ30T1G	3.0	LGU		
NCP502ASQ33T1G	3.3	LGV		
NCP502ASQ35T1G	3.5	LGW		
NCP502ASQ50T1G	5.0	LGX		

ORDERING INFORMATION

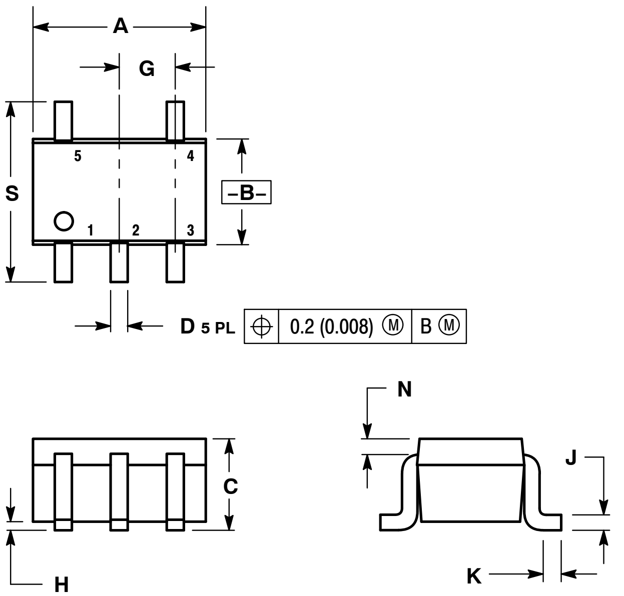
Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP502SN28T1G	2.8	LKD	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP502SN29T1G	2.9	LJN		
NCP502SN30T1G	3.0	LKE		
NCP502SN31T1G	3.1	LJO		
NCP502SN33T1G	3.3	LKF		
NCP502SN34T1G	3.4	LJK		
NCP502SN35T1G	3.5	LJ6		
NCP502SN36T1G	3.6	AC4		
NCP502SN37T1G	3.7	LKC		
NCP502SN50T1G	5.0	LKG		

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

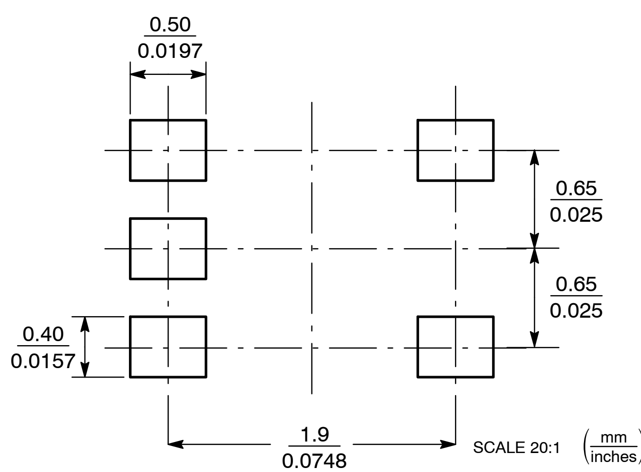
SC70−5, SC−88A, SOT−353
SQ SUFFIX
CASE 419A−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

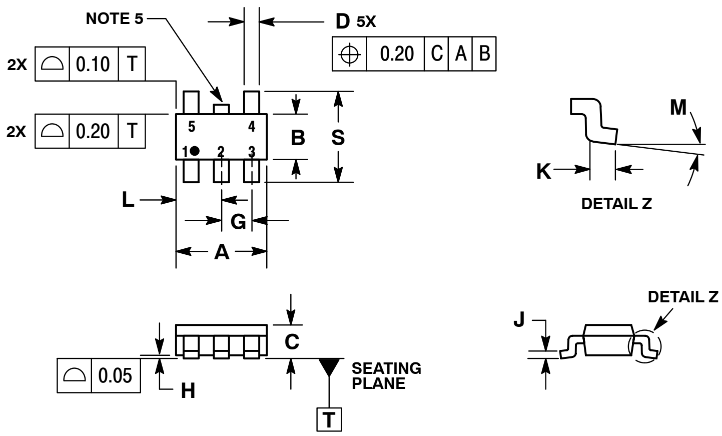
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

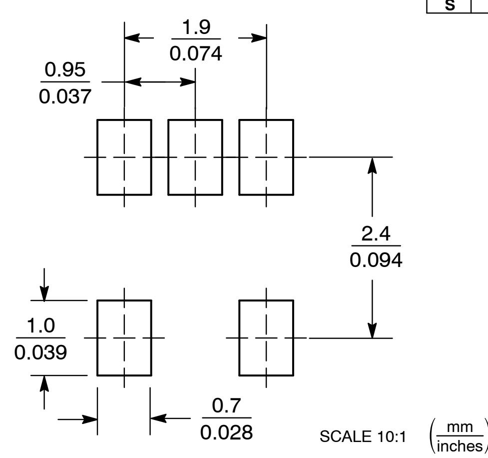
TSOP−5
CASE 483−02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

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