

SIGNETICS DIGITAL 54/74 TTL SERIES — S54H73 • N74H73

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S54H73 Circuits	4.5	5	5.5	V
N74H73 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A : S54H73 Circuits	-55	25	125	$^{\circ}\text{C}$
N74H73 Circuits	0	25	70	$^{\circ}\text{C}$
Normalized Fan-Out from each Output, N			10	
Width of Clock Pulse, $t_{p(\text{clock})}$	12			ns
Width of Clear Pulse, $t_{p(\text{clear})}$	16			ns
Input Setup Time, t_{setup} (See above)	$\geq t_{p(\text{clock})}$			
Input Hold Time, t_{hold}	0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS**	MIN	TYP†	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}$, $I_{\text{load}} = -500\mu\text{A}$	2.4			V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}$, $I_{\text{sink}} = 20\text{mA}$			0.4	V
$I_{in(0)}$ Logical 0 level input current at J, K, or clock	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-2	mA
$I_{in(0)}$ Logical 0 level input current at clear	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-4	mA
$I_{in(1)}$ Logical 1 level input current at J or K	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			50 1	μA mA
$I_{in(1)}$ Logical 1 level input current at clock	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			50 1	μA mA
$I_{in(1)}$ Logical 1 level input current at clear	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			100 1	μA mA
I_{OS} Short circuit output current**	$V_{CC} = \text{MAX}$, $V_{in} = 0$	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$		32	50	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$, N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock} Maximum clock frequency	$C_L = 25\text{pF}$, $R_L = 280\Omega$	25	30		MHz
t_{pd1} Propagation delay time to logical 1 level from clear to output	$C_L = 25\text{pF}$, $R_L = 280\Omega$		6	13	ns
t_{pd0} Propagation delay time to logical 0 level from clear to output	$C_L = 25\text{pF}$, $R_L = 280\Omega$		12	24	ns
t_{pd1} Propagation delay time to logical 1 level from clock to output	$C_L = 25\text{pF}$, $R_L = 280\Omega$		16	21	ns
t_{pd0} Propagation delay time to logical 0 level from clock to output	$C_L = 25\text{pF}$, $R_L = 280\Omega$		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$