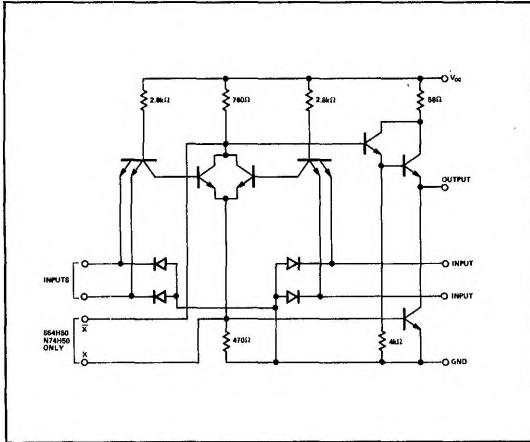


S54H50—A,F,W • S54H51—A,F,W • N74H50—A,F • N74H51—A,F

DIGITAL 54/74 TTL SERIES

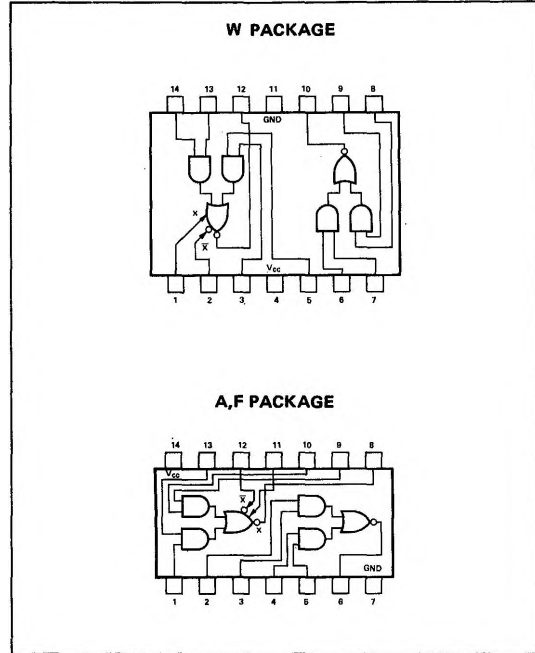
#### SCHEMATIC (each gate)



#### NOTES:

1. Component values are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and X pins open.
4. Expander inputs X and X are functional on the S54H50 and N74H50 circuits only. Make no external connection to X and X pins of the S54H51 and N74H51.
5. A total of four S54H60/N74H60 expander gates or one S54H62/N74H62 expander gate may be connected to the expander inputs.

#### PIN CONFIGURATIONS



#### RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage $V_{CC}$ : S54H50, S54H51 Circuits N74H50, N74H51 Circuits	4.5	5	5.5	V
	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, $T_A$ : S54H50, S54H51 Circuits N74H50, N74H51 Circuits	-55	25	125	°C
	0	25	70	°C

#### ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output $V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output $V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage $V_{CC} = \text{MIN}$ , $I_{load} = -500\mu\text{A}$	2.4			V
$V_{out(0)}$	Logical 0 output voltage $V_{CC} = \text{MIN}$ , $I_{sink} = 20\text{mA}$			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input) $V_{CC} = \text{MAX}$ , $V_{in} = 0.4\text{V}$			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input) $V_{CC} = \text{MAX}$ , $V_{CC} = \text{MAX}$ , $V_{in} = 2.4\text{V}$ , $V_{in} = 5.5\text{V}$			50 1	$\mu\text{A}$ mA

# DIGITAL 54/74 TTL SERIES ■ S54H50, S54H51, N74H50, N74H51

## ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{OS}$	Short circuit output current **			-40	-100	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 4.5\text{V}$		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX}$ , $V_{in} = 0$		8.2	12.8	mA

## ELECTRICAL CHARACTERISTICS (S54H50 circuits only) using expander inputs, $V_{CC} = 4.5\text{V}$ , $T_A = -55^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{X}}$	Expander-node input current	$V_{\bar{X}} = 1.4\text{V}$		-5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	$I_{\text{sink}} = 20\text{mA}$ , $I_1 = 700\mu\text{A}$ , $R_1 = 0$		1	V
$V_{out(1)}$	Logical 1 output voltage	$I_{\text{load}} = -500\mu\text{A}$ , $I_2 = -320\mu\text{A}$	$I_1 = 320\mu\text{A}$	2.4	V
$V_{out(0)}$	Logical 0 output voltage	$I_{\text{sink}} = 20\text{mA}$ , $I_1 = 470\mu\text{A}$ , $R_1 = 68\Omega$		0.4	V

## ELECTRICAL CHARACTERISTICS (N74H50 circuits only) using expander inputs, $V_{CC} = 4.5\text{V}$ , $T_A = 0^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in\bar{X}}$	Expander-node input current	$V_{\bar{X}} = 1.4\text{V}$		-6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	$I_{\text{sink}} = 20\text{mA}$ , $I_1 = 1.1\text{mA}$ , $R_1 = 0$		1	V
$V_{out(1)}$	Logical 1 output voltage	$I_{\text{load}} = -500\mu\text{A}$ , $I_2 = -570\mu\text{A}$	$I_1 = 570\mu\text{A}$	2.4	V
$V_{out(0)}$	Logical 0 output voltage	$I_{\text{sink}} = 20\text{mA}$ , $I_1 = 600\mu\text{A}$ , $R_1 = 63\Omega$		0.4	V

## SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$ , expander pins are open

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 25\text{pF}$ , $R_L = 280\Omega$		6.2	11	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 25\text{pF}$ , $R_L = 280\Omega$		6.8	11	ns

## SWITCHING CHARACTERISTICS, (S54H50/N74H50 circuits only), $V_{CC} = 5\text{V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$ , $C_X = 15\text{pF}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$	Propagation delay time to logical 0 level	$C_L = 25\text{pF}$ , $R_L = 280\Omega$		7.4	ns
$t_{pd1}$	Propagation delay time to logical 1 level	$C_L = 25\text{pF}$ , $R_L = 280\Omega$		11	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

\*\* Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .