

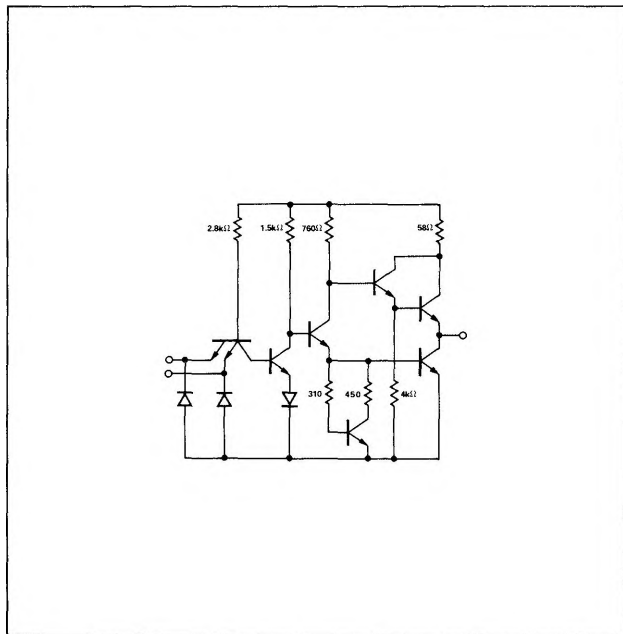
QUADRUPLE 2-INPUT POSITIVE AND GATE

S54H08 N74H08

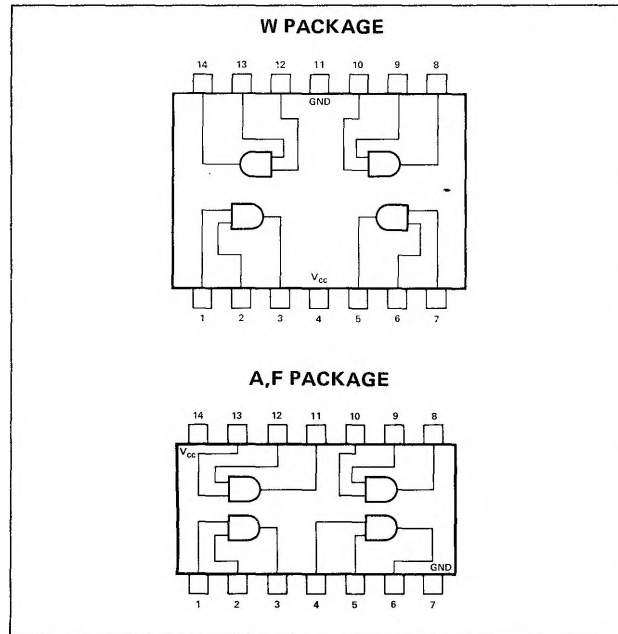
S54H08-A,F,W • N74H08-A,F

DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} :				
S54H08 Circuits	4.5	5	5.5	V
N74H08 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A :				
S54H08 Circuits	-55	25	125	°C
N74H08 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP**	MAX	UNIT	
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	$V_{CC} = \text{MIN},$	$V_{out(0)} \leq 0.4V$	2	V	
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	$V_{CC} = \text{MIN},$	$V_{out(1)} \geq 2.4V$	0.8	V	
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN},$ $I_{load} = 500\mu A$	$V_{in} = 0.8V$	2.4	V	
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN},$ $I_{sink} = 20mA$	$V_{in} = 2V$	0.4	V	
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX},$	$V_{in} = 0.4V$	-2	mA	
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX},$ $V_{CC} = \text{MAX},$	$V_{in} = 2.4V$ $V_{in} = 5.5V$	50 1	μA mA	
I_{OS}	Short-circuit output current †	$V_{CC} = \text{MAX},$		-40	-100	mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX},$	$V_{in} = 4.5V$	40	64	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX},$	$V_{in} = 0$	24	40	mA

SIGNETICS DIGITAL 54/74 TTL SERIES — S54H08 • N74H08

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CI}	Input negative clamp voltage	$V_{CC} = 5V$ $T_A = 25^\circ C$	$I_{in} = -12.0mA$			-1.5	V

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	$C_L = 25pF$,	$R_L = 280\Omega$		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	$C_L = 25pF$,	$R_L = 280\Omega$		7.6	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values at: $V_{CC} = 5V$, $T_A = 25^\circ C$.

† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.