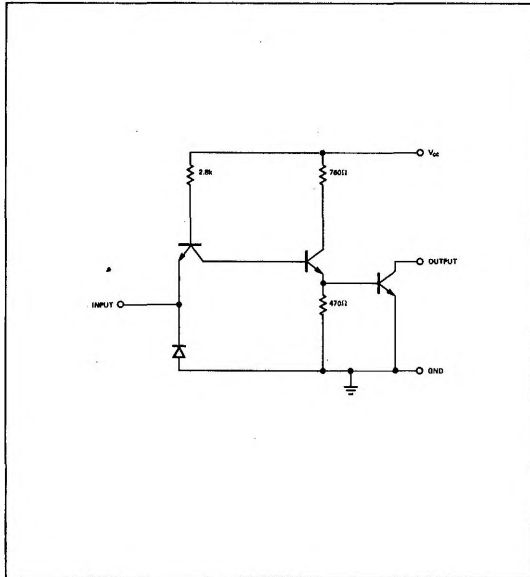


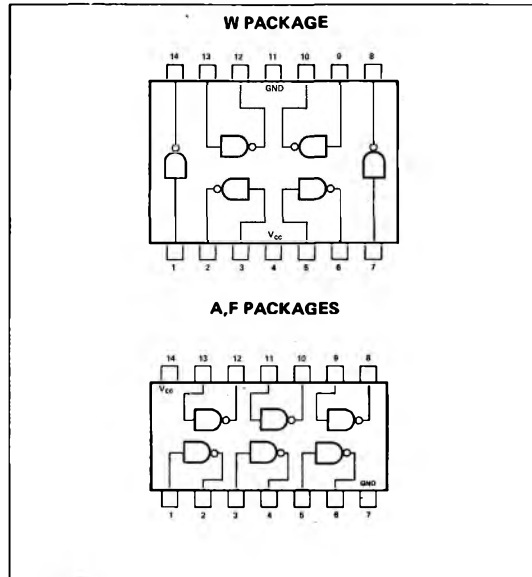
S54H05-A,F,W • N74H05-A,F

DIGITAL 54/74 TTL SERIES

SCHEMATIC (each inverter)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S54H05 Circuits	4.5	5	5.5	V
N74H05 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A : S54H05 Circuits	-55	25	125	$^{\circ}C$
N74H05 Circuits	0	25	70	$^{\circ}C$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 _(on) level at output	$V_{CC} = \text{MIN},$	2		V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 _(off) level at output	$V_{CC} = \text{MIN},$		0.8	V
$I_{out(1)}$	Output reverse current	$V_{CC} = \text{MIN},$ $V_{out(1)} = 5.5V$	$V_{in} = 0.8V,$	250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	$V_{CC} = \text{MIN},$ $I_{sink} = 20mA$	$V_{in} = 2V,$	0.4	V
$I_{in(0)}$	Logical 0 level input current	$V_{CC} = \text{MAX},$	$V_{in} = 0.4V$	-2	mA
$I_{in(1)}$	Logical 1 level input current	$V_{CC} = \text{MAX},$ $V_{CC} = \text{MAX},$	$V_{in} = 2.4V$ $V_{in} = 5.5V$	50 1	μA mA
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX},$	$V_{in} = 4.5V$	40.0 58.0	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX},$	$V_{in} = 0$	16.0 26.0	mA

DIGITAL 54/74 TTL SERIES ■ S54H05, N74H05**SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	$C_L = 25pF$,	$R_L = 280\Omega$		10	15	ns
t_{pd1}	Propagation delay time to logical 1 level	$C_L = 25pF$,	$R_L = 280\Omega$		13	18	ns

- * For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- ** All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
- † Load resistor R_L is connected from V_{CC} to the output, and load capacitor C_L is connected from the output to ground.