DESCRIPTION

The S5474/N7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

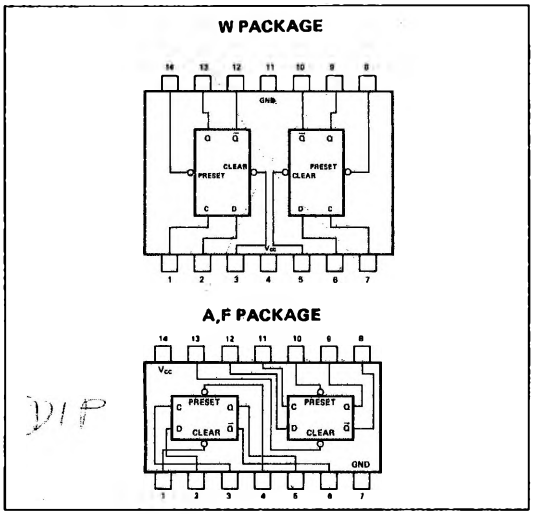
TRUTH TABLE

D_n	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1

Preset	Clear	Q
1	1	Q
1	0	0
0	1	1
0	0	†

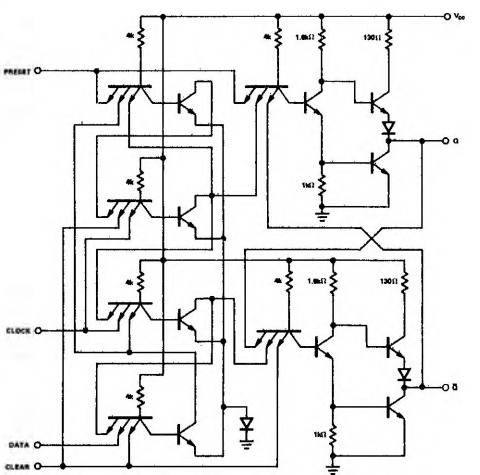
† Both outputs in 1 state
n is time prior to clock
n+1 is time following clock

PIN CONFIGURATIONS



POSITIVE LOGIC – Low input to preset sets Q to logical 1 Low input to clear sets Q to logical 0; Preset and clear are independent of clock

SCHEMATIC DIAGRAM



NOTE: 1/2 of unit shown. Component values are typical.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5474 Circuits		4.5	5	5.5	V
N7474 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5474 Circuits	-55	25	125	°C
	N7474 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 0.4V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				120 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5474 N7474	−20 −18		−57 −57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			17	30	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	25		MHz
t_{setup}	Minimum input setup time	C_L = 15pF,	R_L = 400Ω		15	20	ns
t_{hold}	Minimum input hold time	C_L = 15pF,	R_L = 400Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	20	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.