

S54150-N,Q,F • N74150-N,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

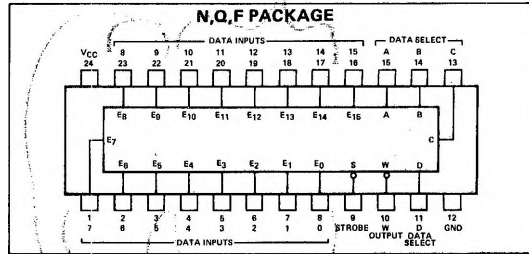
The S4/74150 is a one-of-sixteen data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line.

The S54150/N74150 is provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

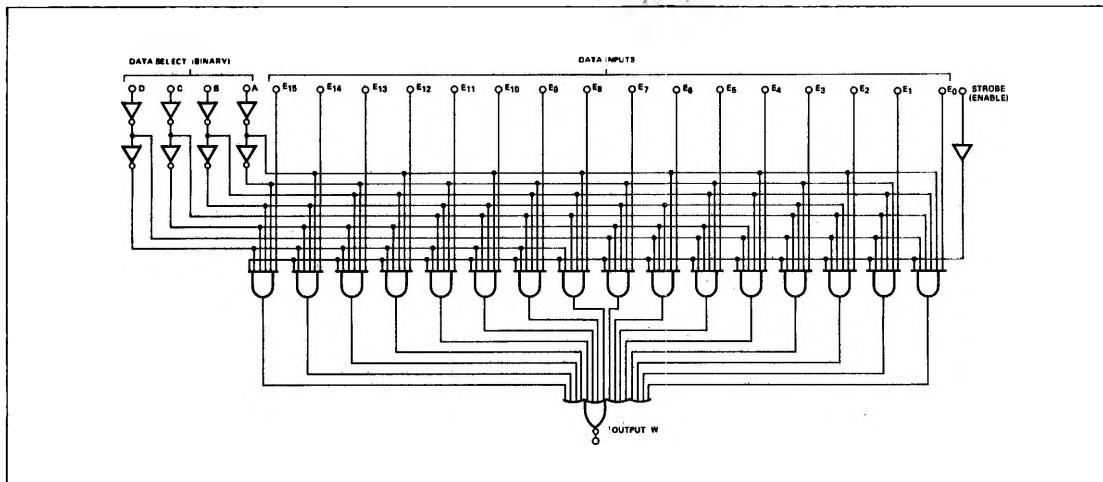
This data selector/multiplexer is fully compatible for use with other TTL or DTL circuit. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

S54150/N74150 - 200 milliwatts.

PIN CONFIGURATIONS



LOGIC DIAGRAM



TRUTH TABLE

DATA SELECT (BINARY)				DATA INPUTS																STROBE (ENABLE)
D	C	B	A	E ₁₅	E ₁₄	E ₁₃	E ₁₂	E ₁₁	E ₁₀	E ₉	E ₈	E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀	W
0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S54150 Circuits	4.5	5	5.5	V
N74150 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: Logical 0			10	
Logical 1			20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}$, $V_{in(1)} = 2V$, $V_{in(0)} = 0.8V$, $I_{load} = -800\mu A$	2.4			V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}$, $V_{in(1)} = 2V$, $V_{in(0)} = 0.8V$, $I_{sink} = 16mA$			0.4	V
$I_{in(1)}$ Logical 1 level input (each input)	$V_{CC} = \text{MAX}$, $V_{in} = 2.4V$			40	μA
	$V_{CC} = \text{MAX}$, $V_{in} = 5.5V$			1	mA
$I_{in(0)}$ Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$, $V_{in} = 0.4V$			-1.6	mA
I_{OS} Short circuit output current†	$V_{CC} = \text{MAX}$, $V_{OUT} = 0$	-20		-55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, $V_{in} = 4.5V$		40	68	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A,B,orC(4 levels)	Y	$C_L = 15pF$, $R_L = 400\Omega$		20	30	ns
t_{pd1}	A,B,orC(4 levels)	Y			35	52	ns
t_{pd0}	A,B,C,orD(3 levels)	W			22	33	ns
t_{pd1}	A,B,C,orD(3 levels)	W			23	35	ns
t_{pd0}	STROBE	Y			19	30	ns
t_{pd1}	STROBE	Y			35	52	ns
t_{pd0}	STROBE	W			21	30	ns
t_{pd1}	STROBE	W			15.5	24	ns
t_{pd0}	D ₀ thru D ₇	Y			16	24	ns
t_{pd1}	D ₀ thru D ₇	Y			19	29	ns
t_{pd0}	E ₀ thru E ₁₅	W			8.5	14	ns
t_{pd1}	E ₀ thru E ₁₅	W			13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

† Not more than one output should be shorted at a time.