DESCRIPTION

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The S54100/N74100 features two independent quadruple latches in a single 24-pin dual in-line package. These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of -55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

ABSOLUTE MAXIMUM RATINGS (over operating temperature range unless otherwise noted)

Supply Voltage, V_{CC} (See Note 3)	7V
Input Voltage, V_{in} (See Notes 3 and 4)	5.5V
Operating Free-Air Temperature Range:	
S54100 Circuits	-55°C to 125°C
N74100 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES:

3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

TRUTH TABLE

LOGIC

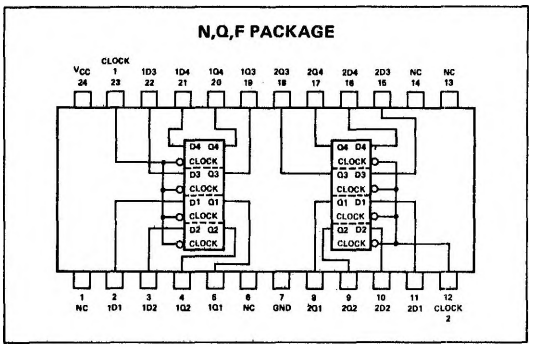
(Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES:

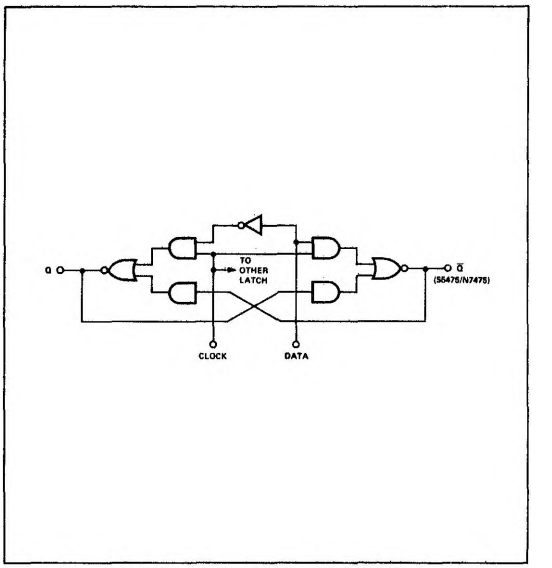
1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

NC – No internal connection.

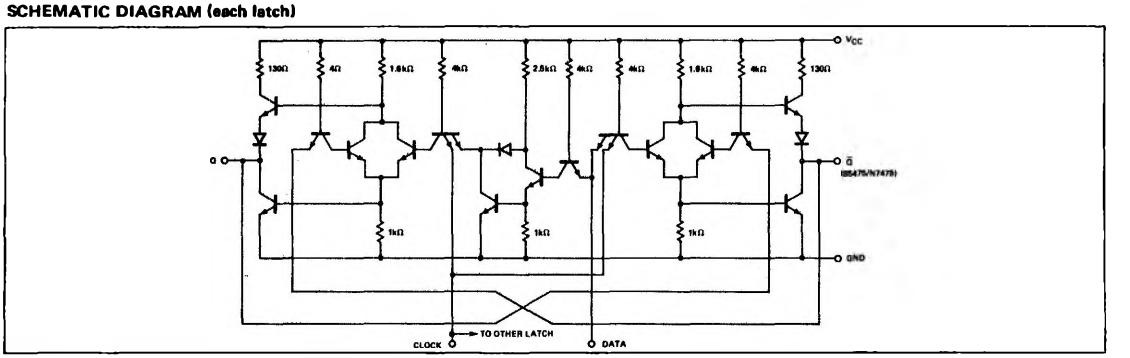
PIN CONFIGURATIONS



LOGIC DIAGRAM (each latch)



SCHEMATIC DIAGRAM (each latch)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3):	S54100	4.5	5	5.5	V
	N74100	4.75	5	5.25	V
Normalized Fan-Out from Output				10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX,	V_{in} = 0.4V			−3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	S54100, N74100			−12.8	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4V			80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,				160	μA
		V_{in} = 2.4V,	S54100, N74100			320	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX,	S54100	−20		−57	mA
		V_{out} = 0	N74100	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX,	S54100		64	92	mA
			N74100		64	106	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS NOTE A		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

NOTE A: AC Test circuit, voltage waveforms and switching times are given on p. 2-76.