

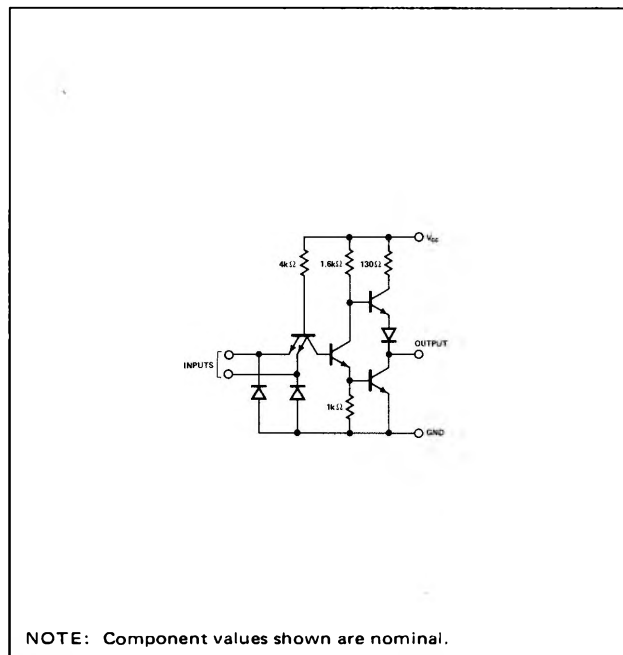
QUADRUPLE 2-INPUT POSITIVE NAND GATE

S5400 N7400

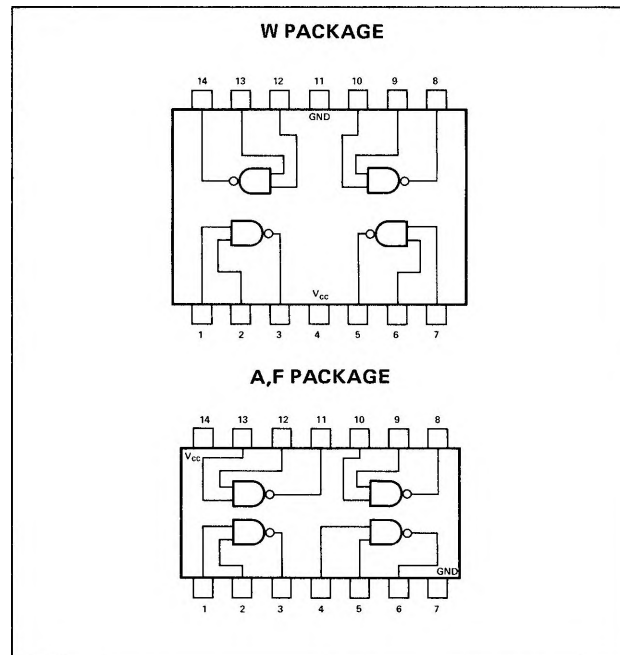
S5400—A,F,W • N7400—A,F

DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)



PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S5400 Circuits	4.5	5	5.5	V
N7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A : S5400 Circuits	-55	25	125	$^{\circ}\text{C}$
N7400 Circuits	0	25	70	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT	
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	$V_{CC} = \text{MIN}$		2	V	
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	$V_{CC} = \text{MIN}$		0.8	V	
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$, $I_{load} = -400\mu\text{A}$	$V_{in} = 0.8\text{V}$,	2.4 3.3	V	
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$, $I_{sink} = 16\text{mA}$	$V_{in} = 2\text{V}$,	0.22 0.4	V	
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$,	$V_{in} = 0.4\text{V}$	-1.6	mA	
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$, $V_{CC} = \text{MAX}$,	$V_{in} = 2.4\text{V}$, $V_{in} = 5.5\text{V}$	40 1	μA mA	
I_{OS}	Short circuit output current†	$V_{CC} = \text{MAX}$	S5400 N7400	-20 -18	-55 -55	mA

SIGNETICS DIGITAL 54/74 TTL SERIES - S5400 • N7400

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	$V_{CC} = \text{MAX},$	$V_{in} = 5V$		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	$V_{CC} = \text{MAX},$	$V_{in} = 0$		4	8	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5V, T_A = 25^\circ C, N = 10$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	$C_L = 15pF,$	$R_L = 400\Omega$		7	15	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level	$C_L = 15pF,$	$R_L = 400\Omega$		11	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5V, T_A = 25^\circ C$

† Not more than one output should be shorted at a time.