MWS5114

1024-Word x 4-Bit LSI Static RAM

March 1997

Features

- **Fully Static Operation**
- **Industry Standard 1024 x 4 Pinout (Same as Pinouts for 6514, 2114, 9114, and 4045 Types)**
- **Common Data Input and Output**
- **Memory Retention for Standby Battery Voltage as Low as 2V Min**
- **All Inputs and Outputs Directly TTL Compatible**
- **Three-State Outputs**
- **Low Standby and Operating Power**

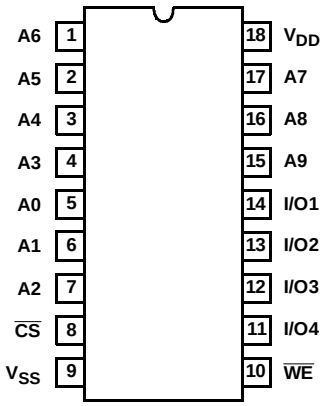
Description

Ordering Information

200ns	250ns	300ns	TEMPERATURE RANGE	PACKAGE	PKG. NO.
MWS5114E3	MWS5114E2 MWS5114E2X	MWS5114E1	0^oC to $+70^oC$	PDIP Burn-In	E18.3 E18.3
MWS5114D3 MWS5114D3X	MWS5114D2	MWS5114D1	0^oC to $+70^oC$	SBDIP Burn-In	D18.3 D18.3

Pinout

MWS5114
(PDIP, SBDIP)
TOP VIEW



OPERATIONAL MODES

FUNCTION	$\overline{CS}$	$\overline{WE}$	DATA PINS
Read	0	1	Output: Dependent on data
Write	0	0	Input
Not Selected	1	X	High Impedance

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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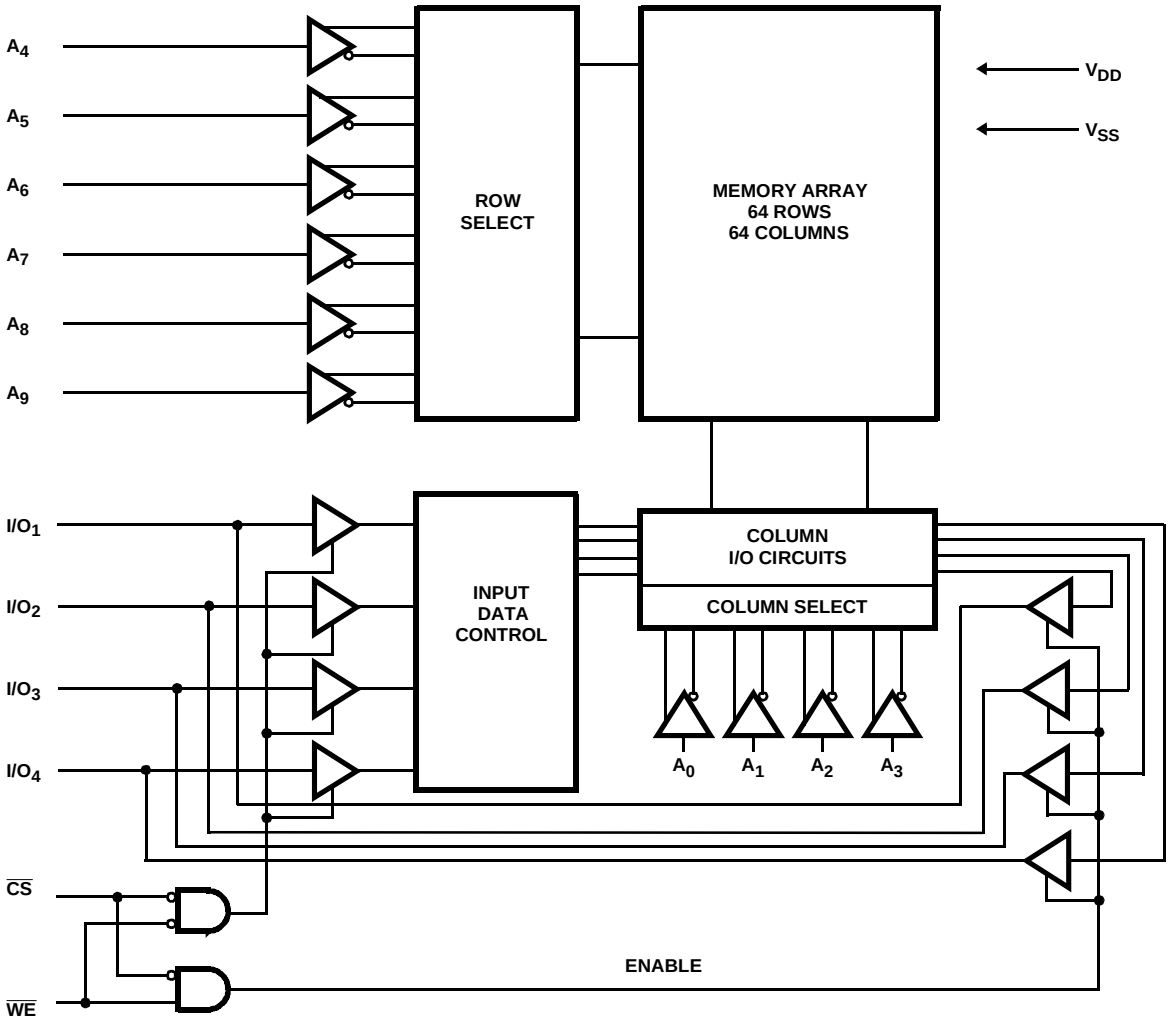
Functional Block Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal) . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input . . . . . ±10mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
Plastic DIP Package	75	N/A
SBDIP Package	75	20

Operating Temperature Range (T_A)
Package Type D . . . . . -55^{o}C to +125^{o}C
Package Type E . . . . . -40^{o}C to +85^{o}C
Maximum Storage Temperature Range (T_{STG}) . . . -65^{o}C to +150^{o}C
Maximum Junction Temperature
Ceramic Package . . . . . +175^{o}C
Plastic Package . . . . . +150^{o}C
Maximum Lead Temperature . . . . . +265^{o}C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS ALL TYPES MIN	LIMITS ALL TYPES MAX	UNITS
DC Operating Voltage Range	4.5	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications

At T_A = 0^{o}C to +70^{o}C, V_{DD} = ±5%, Except as Noted

PARAMETER	SYMBOL	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS MWS5114-3 MIN	MWS5114-3 (NOTE 1) TYP	MWS5114-3 MAX	MWS5114-2 MIN	MWS5114-2 (NOTE 1) TYP	MWS5114-2 MAX	MWS5114-1 MIN	MWS5114-1 (NOTE 1) TYP	MWS5114-1 MAX	UNITS
Quiescent Device Current	IDD	-	0, 5	5	-	75	100	-	75	100	-	75	250	µA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	2	4	-	2	4	-	2	4	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	5	-0.4	-1	-	-0.4	-1	-	-0.4	-1	-	mA
Output Voltage Low-Level	VOL	-	0, 5	5	-	0	0.1	-	0	0.1	-	0	0.1	V
Output Voltage High-Level	VOH	-	0, 5	5	4.9	5	-	4.9	5	-	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	1.2	0.8	-	1.2	0.8	-	1.2	0.8	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	2.4	-	-	2.4	-	-	2.4	-	-	V
Input Leakage Current (Note 2)	IIN	-	0, 5	5	-	±0.1	±5	-	±0.1	±5	-	±0.1	±5	µA
Operating Current (Note 3)	IDD1	-	0, 5	5	-	4	8	-	4	8	-	4	8	mA

Static Electrical Specifications At $T_A = 0^oC$ to $+70^oC$, $V_{DD} = \pm5\%$, Except as Noted **(Continued)**

PARAMETER	SYMBOL	CONDITIONS			LIMITS									UNITS
					MWS5114-3			MWS5114-2			MWS5114-1			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Three-State Output Leakage Current (Note 4)	I_{OUT}	0, 5	0, 5	5	-	±0.5	±5	-	±0.5	±5	–	±0.5	±5	µA
Input Capacitance	CI_N	-	-	-	-	5	7.5	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	-	10	15	pF

NOTES:

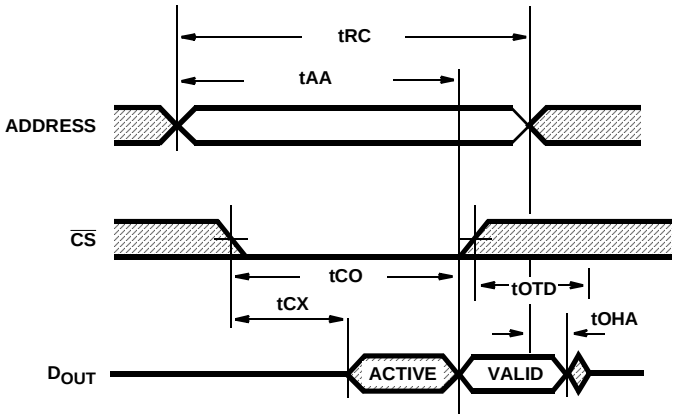
1. Typical values are for $T_A = 25^oC$ and nominal V_{DD}.
2. All inputs in parallel.
3. Outputs open circuited; cycle time = 1µs.
4. All outputs in parallel.

Dynamic Electrical Specifications at $T_A = 0^oC$ to $+70^oC$, $V_{DD} = 5V \pm 5\%$, Input t_R, $t_F = 10ns$; $C_L = 50pF$ and 1 TTL Load

PARAMETER	SYMBOL	LIMITS									UNITS
		MWS5114-3			MWS5114-2			MWS5114-1			
		(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	(NOTE 1) MIN	(NOTE 2) TYP	MAX	
READ CYCLE TIMES (FIGURE 1)											
Read Cycle	tRC	200	160	-	250	200	-	300	250	-	ns
Access from Address	tAA	-	160	200	-	200	250	-	250	300	ns
Chip Selection to Output Valid	tCO	-	110	150	-	150	200	-	200	250	ns
Chip Selection to Output Active	tCX	20	100	-	20	100	-	20	100	-	ns
Output Three-State from Deselection	tOTD	-	75	125	-	75	125	-	75	125	ns
Output Hold from Address Change	tOHA	50	100	-	50	100	-	50	100	-	ns
WRITE CYCLE TIMES (FIGURE 2)											
Write Cycle	tWC	200	160	-	250	200	-	300	220	-	ns
Write	tW	125	100	-	150	120	-	200	140	-	ns
Write Release	tWR	50	40	-	50	40	-	50	40	-	ns
Address to Chip Select Setup Time	$t\overline{ACS}$	0	0	-	0	0	-	0	0	-	ns
Address to Write Setup Time	$t\overline{AW}$	25	20	-	50	40	-	50	40	-	ns
Data to Write Setup Time	tDSU	75	50	-	75	50	-	75	50	-	ns
Data Hold from Write	tDH	30	10	-	30	10	-	30	10	-	ns

NOTES:

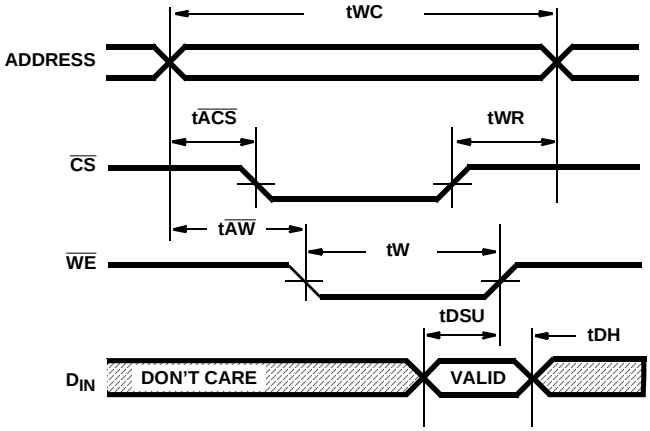
1. Time required by a limit device to allow for the indicated function.
2. Typical values are for $T_A = 25^oC$ and nominal V_{DD}.



NOTE:

1. $\overline{WE}$ is high during the Read Cycle. Timing measurement reference level is 1.5V.

FIGURE 1. READ CYCLE TIMING WAVEFORMS



NOTE:

1. $\overline{WE}$ is low during the Write Cycle. Timing measurement reference level is 1.5V.

FIGURE 2. WRITE CYCLE TIMING WAVEFORMS

Data Retention Specifications at $T_A = 0^oC$ to $+70^oC$; See Figure 3

PARAMETER		SYMBOL	TEST CONDITIONS		LIMITS			UNITS
					ALL TYPES			
			V_{DR} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	
Minimum Data Retention Voltage		VDR	-	-	2	-	-	V
Data Retention Quiescent Current	MWS5114-3	IDD	2	-	-	25	50	µA
	MWS5114-2		2	-	-	25	50	µA
	MWS5114-1		2	-	-	60	125	µA
Chip Deselect to Data Retention Time		tCDR	-	5	300	-	-	ns
Recovery to Normal Operation Time		tRC	-	5	300	-	-	ns
V_{DD} to V_{DR} Rise and Fall Time		t_R, t_F	2	5	1	-	-	µs

Data Retention Specifications at $T_A = 0^oC$ to $+70^oC$; See Figure 3

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
				ALL TYPES			
		V_{DR} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	

NOTE:

1. Typical Values are for $T_A = 25^oC$ and nominal V_{DD}.

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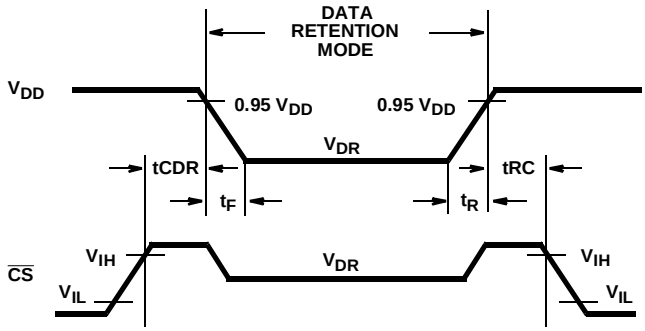

FIGURE 3. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS