Preliminary

OKI semiconductor

MSM37256-AS/RS

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM37256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

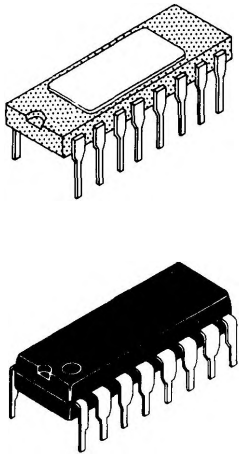
Multiplexed row and column address inputs permit the MSM37256 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MSM37256 is fabricated using silicon gate NMOS and Oki's advanced VLSI Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

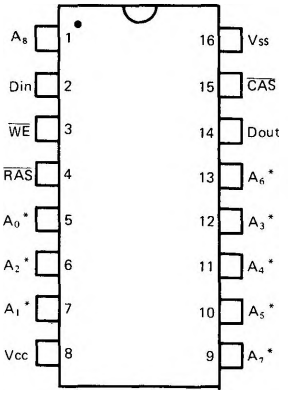
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262,144 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  100 – 120 ns max
- Cycle time,
  200 – 240 ns max
- Low power: 300 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 256 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

* Refresh Address

BLOCK DIAGRAM