Freescale Semiconductor
Product Brief

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MSC8144E Product Brief

Quad-Core Media Packet Signal Processor

The MSC8144E device is a third generation Freescale high-end multicore DSP device that targets the communications infrastructure. It builds upon the proven success of the previous multicore DSPs and is designed to bolster the rapidly expanding multi-channel packetized media and wireless markets.

Contents

1 Example Applications

The applications covered in this section are as follows:

- Generic system example
- DSP farm example using UTOPIA and TDM
- System solution example using Ethernet as the packet interface
- Serial RapidIO (SerDes) connectivity example
- Radio network controller (RNC) application blade example

1.1 Generic System

The MSC8144E promotes easy system building for legacy, transition, and generation system interface requirements through its flexible and varied I/O protocol support. A generic system block diagram is shown in Figure 1. For completeness, DDR SDRAMs are shown attached to the MSC8144E devices, but for most applications the internal device memory is all that is required. The system can self-boot over either the serial RapidIO interface or Ethernet.
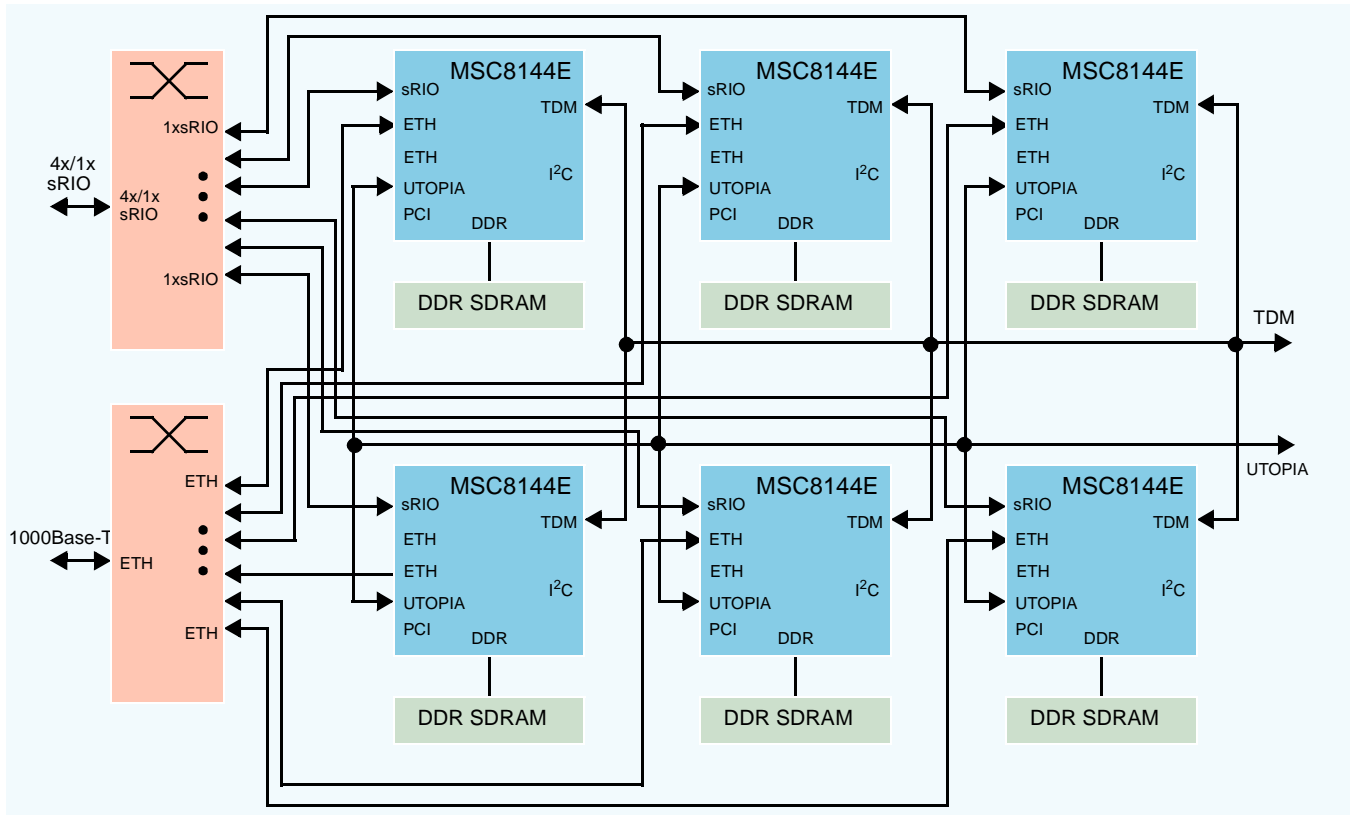

Figure 1. Generic System Block Diagram

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1.2   DSP Farm Using UTOPIA and TDM

In the system shown in Figure 2, the UTOPIA level 2 (UL2) provides the packet (cell) based interface through either AAL2 or AAL5. To provide the PCM side, TDM is used. The UL2 interface on the MSC8144E provides parsing into the IP packet contained in the AAL5 common part sublayer (CPS). For AAL2, it can support multiple AAL2 CPS packets per cell. In both cases, each SC3400 core can have individual buffer rings. In this example, a TDM is chosen.
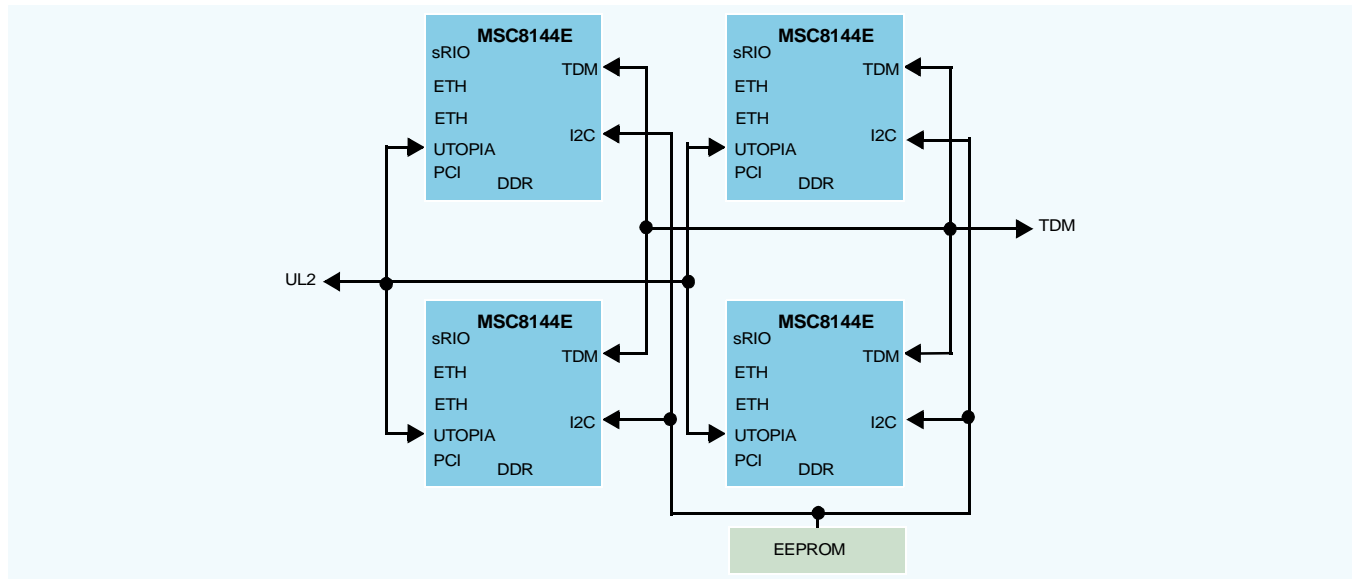

Figure 2. DSP Farm Example Using UTOPIA and TDM

1.3   System Solution with an Ethernet Packet Interface

The example shown in Figure 3 uses Ethernet as the packet interface. To use high volume commodity switches for aggregation, a 1000 BaseT interface is used in MAC-to-MAC configuration. A PowerQUICC™ device connected to the switch provides ingress routing on the UDP destination port number and manages the switch so that the egress data path does not go through the PowerQUICC device. TDM is used for the PCM side. For such solutions, no time-slot assigner is required because the MSC8144E devices can interface with an H.110-like bus.
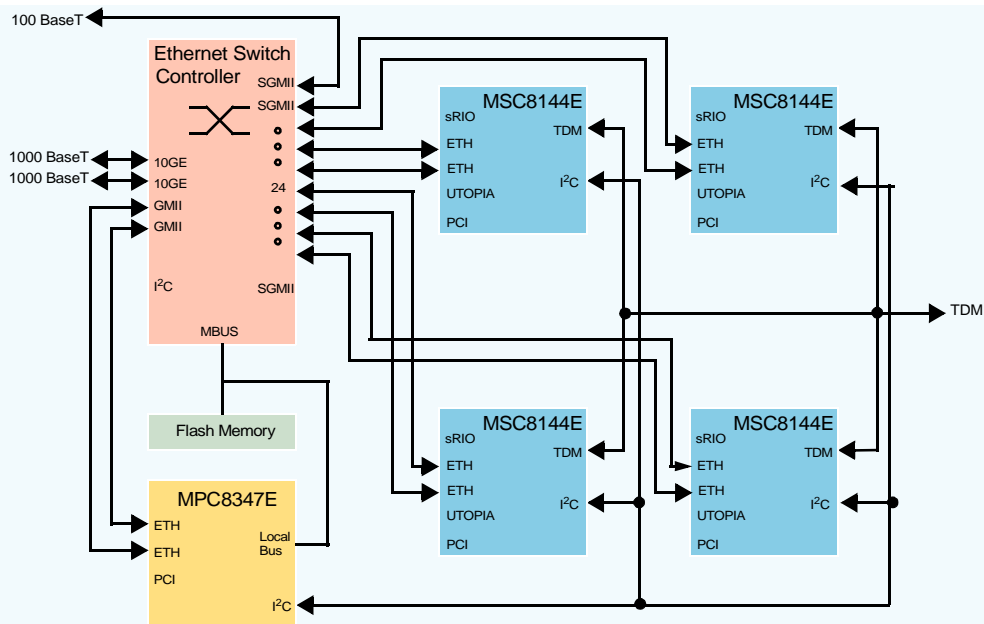
Figure 3. System Solution Using Ethernet as the Packet Interface

1.4   Serial RapidIO Connectivity

The example in Figure 4 uses the serial RapidIO interface. For the MSC8144E, the interface can use either gigabit Ethernet (SGMII) or serial RapidIO. Thus, the MSC8144E is AMC/advanced TCA ready. For AMC, this bus would be on the extended connector with the SerDes in the fabric area.
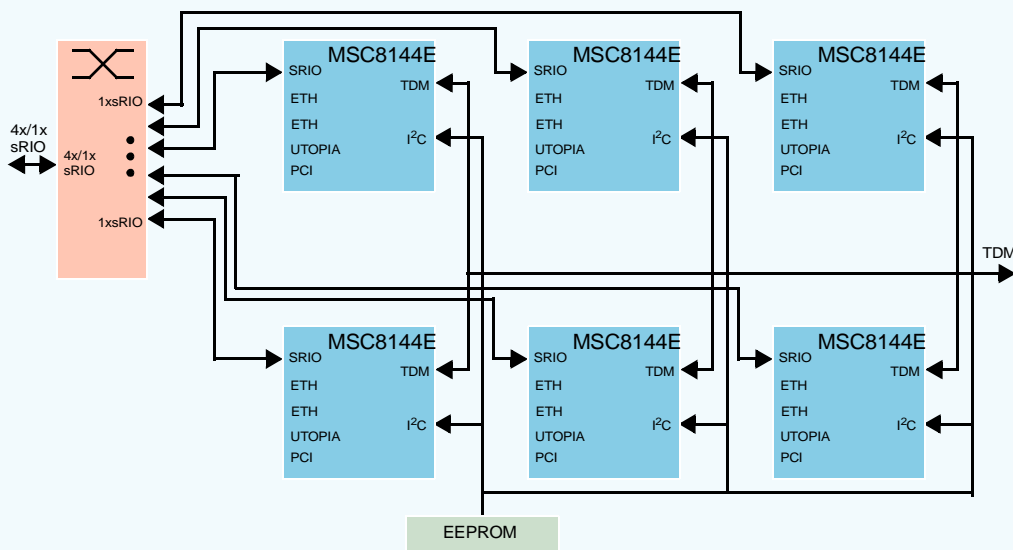

Figure 4. SerDes Connectivity

1.5 Blade Server for RNL

An application blade server that executes the radio network layer (RNL) to process RNC traffic using the MSC8144E is shown in is shown in Figure 5. This example is a farm of MSC8144E devices with external memory. The blade example shows both SerDes type interfaces on the card; however, only one type of interface is required. The system can self-boot over either the serial RapidIO interface or Ethernet.
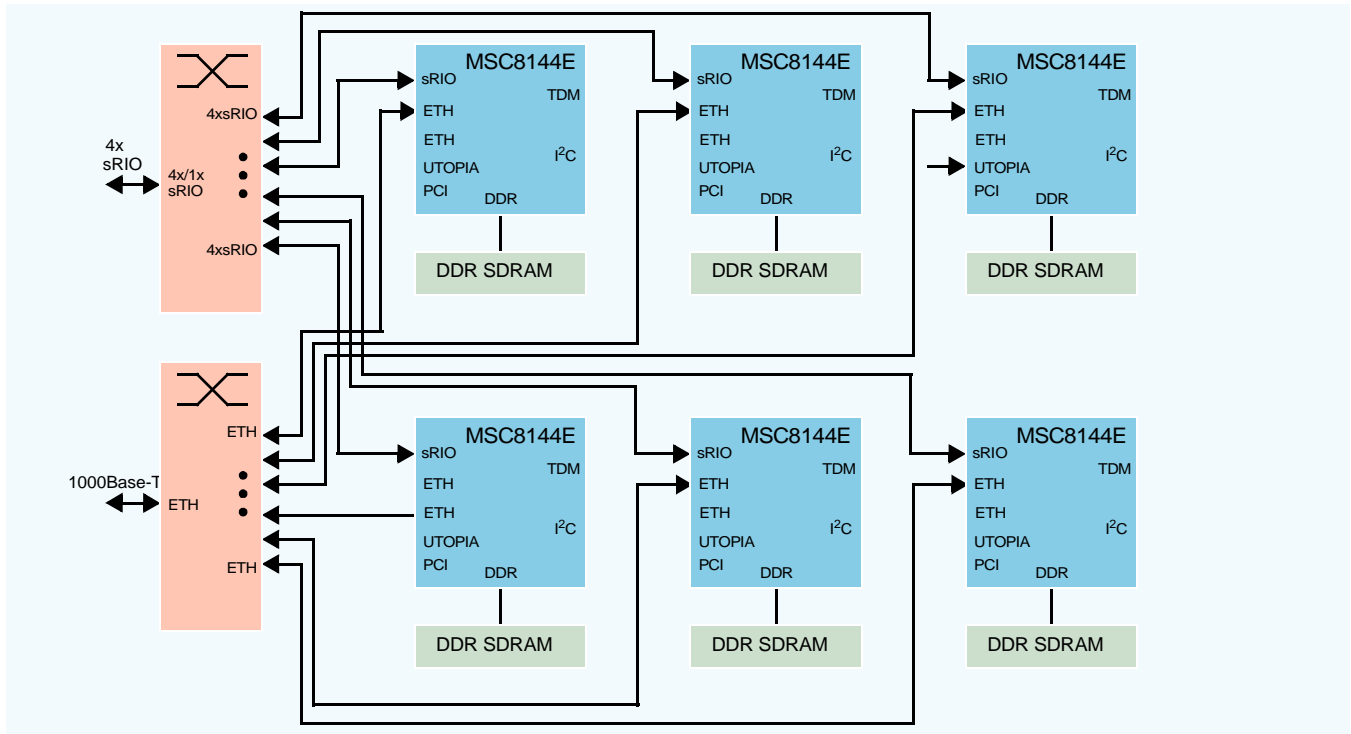

Figure 5. RNC Traffic Processing Board That Executes RNL Block Diagram

2 Features

The MSC8144E device targets high-bandwidth highly computational DSP applications and is optimized for packet telephony, wireless, and video transcoding and radio network controller (RNC) applications.

2.1 Block Diagram

The MSC8144E device is a highly integrated DSP processor that contains four StarCore^{TM} SC3400 DSP subsystems, 512 Kbytes of M2 shared memory, 10 Mbytes of M3 shared memory, L1 instruction and data caches optimized for packet telephony, 128 Kbytes of shared L2 instruction cache, a DDR memory controller, a serial RapidIO interface, two 10/100/1000 BaseT Ethernet controllers, an ATM controller supporting various ATM adaptation layers, eight 256-channel time-division multiplexing (TDM) interfaces, a 16-channel DMA controller, 32-bit PCI interface that runs at 66/33 MHz, a UART interface, and an I^{2}C interface. Each SC3400 DSP core has four ALUs and performs at 3200/4000 16×16-bit million multiply accumulates per second (MMACS) at 800 MHz/1 GHz yielding a maximum total performance of 12800/16000 16×16-bit MMACS per device or 25600/32000 8×8-bit MMACS per device. Each SC3400 core connects to the following:

Features

- 16 Kbyte 8-way level 1 instruction cache (ICache)
- 32 Kbyte 8-way level 1 data cache (DCache)

The MSC8144E has two types of interfaces: TDM and packet (Ethernet, UTOPIA, and RapidIO interface). In TDM-to-packet applications, for example, data received from the TDM interface is stored in the MSC8144E memory, processed by the SC3400 cores, and transmitted on one of the packet interfaces. In the other direction, packets are received, stored in the MSC8144E memory, processed by the SC3400 cores, and transmitted through the TDM interface. A block diagram of the MSC8144E is shown in Figure 6. A separate block diagram for the extended cores is shown in Figure 7.
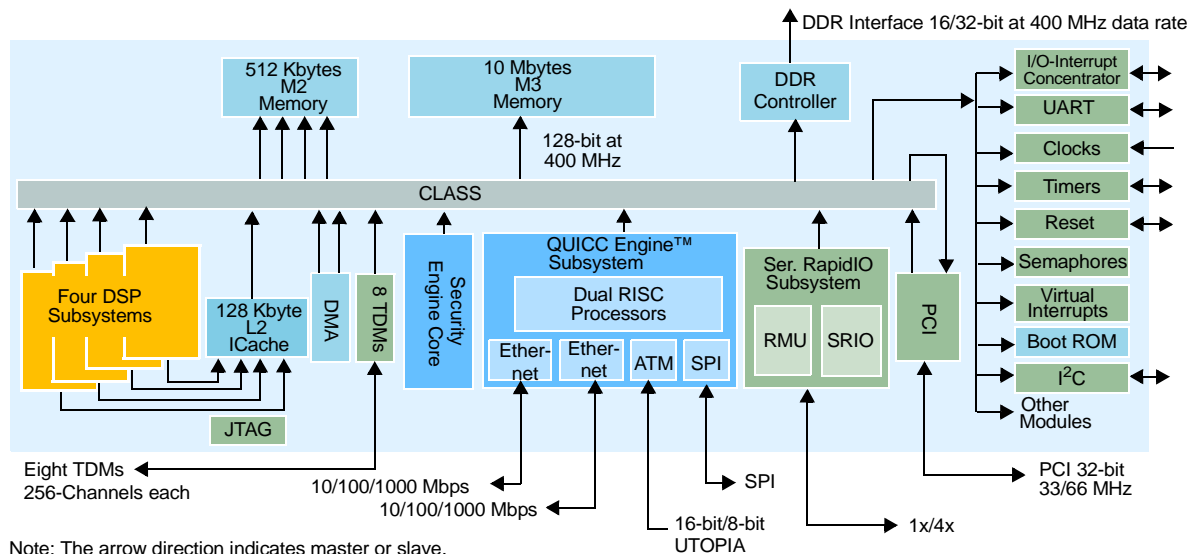

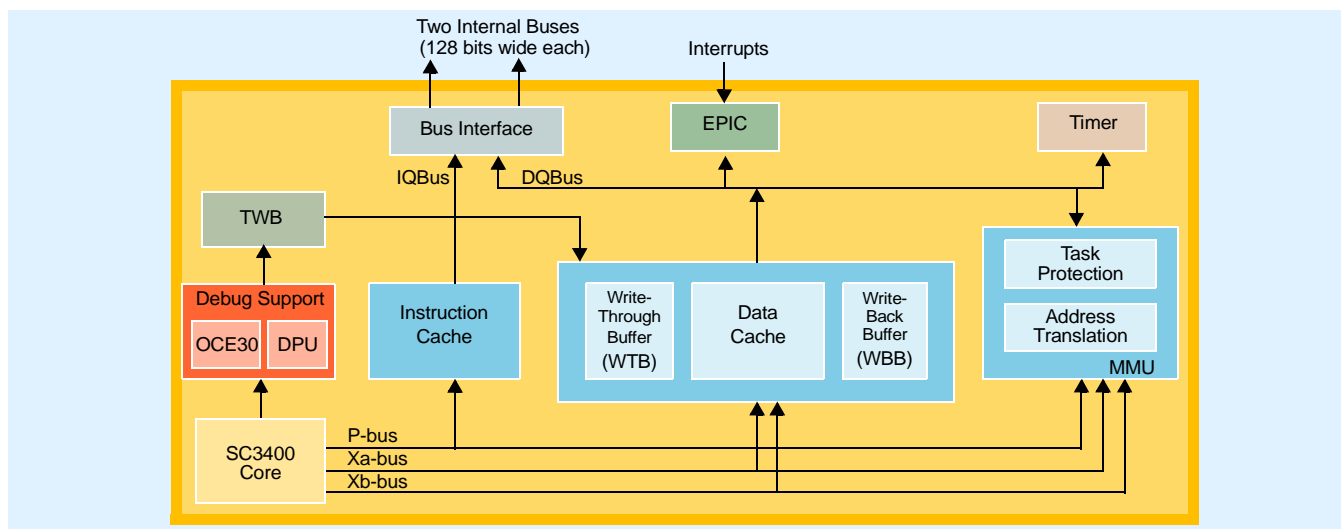**Figure 6. MSC8144E Block Diagram**

Figure 7. StarCore SC3400 DSP Subsystem Block Diagram

2.2   Critical Performance Metrics

- Offered with core frequencies of 800 MHz or 1 GHz, supports:
  - 16×16-bit multiply accumulate instructions. Up to 12800/16000 MMACS at 800 MHz/1 GHz within four SC3400 cores.
  - 8×8-bit multiply accumulate instructions for video applications. Up to 25600/32000 MMACS at 800 MHz/1 GHz within four SC3400 cores.
  - The 16 ALUs deliver a performance equivalent to a single core running at 3.2/4 GHz. A multiply-accumulate operation includes a multiply-add instruction with the associated data move and pointer update.
- Dual RISC engine operating at up to 400 MHz provides parallel packet processing independent of the DSP cores, allowing the cores to process data while the RISC engines manage the data flow and packetization.
- Power supplies:
  - Core power: 1 V nominal
  - M3 power: 1.2 V nominal
  - I/O power: 1.8 V, 2.5 V, and 3.3 V nominal
- Flip Chip-Plastic Ball Grid Array (FC-PBGA), 1 mm pitch, 29 mm $\times$ 29 mm

2.3   Device Level Features

This multicore DSP delivers the industry's highest level of performance and integration, combining four fully-programmable StarCore™ DSP cores, each running at up to 1 GHz with an architecture highly optimized for voice, fax, video, and data compression processing. A security engine core accelerates data plane encryption/decryption with minimal DSP cores intervention. An internal RISC-based QUICC Engine™ subsystem supports multiple networking protocols, including IPSec, to guarantee reliable data transport over packet networks while significantly offloading such processing from the DSP cores. The MSC8144E embeds the industry's largest internal memory and supports a variety of advanced interface types, including high-speed Ethernet and UTOPIA for network communications, DDR controller for high-speed, industry-standard memory interface, multi-channel TDM interfaces for connectivity to the PSTN networks, and serial RapidIO® and PCI interfaces for connectivity to other devices mounted on the same rack or circuit board. The highly flexible, fully-programmable and powerful MSC8144E multimedia DSP offers tremendous processing power while maintaining a competitive price and power per channel. The MSC8144E is pin compatible and fully functional backward compatible to its predecessor, the MSC8144.

2.4   Module Level Features

- StarCore DSP subsystem. The DSP subsystem includes:
  - StarCore SC3400 core
  - L1 ICache:
    - 16 Kbytes
    - 8 way with 8 lines per way.

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- Multitasking support
- Real-time support through locking flexible boundaries
- Prefetch capability
- Software coherency support
— L1 DCache:
  - 32 Kbytes
  - 8 way with 16 lines per way
  - Can service two data accesses in parallel (XA, XB)
  - Multitasking support
  - Real-time support through locking flexible boundaries
  - Software coherency support
  - Writing policy programmable per memory segment as either write-back or write-through
  - 0.25 Kbyte write-back buffer (WBB)
  - Six 64-bit entry write-through buffer (WTB)
  - Prefetch capability
— Memory management unit (MMU):
  - Virtual-to-physical address translation
  - Task protection
  - Multitasking
— Extended programmable interrupt controller (EPIC)
  - Up to 256 interrupts
  - 32 priority levels
— Two general-purpose 32-bit timers
— Debug and profiling support:
  - On-chip emulator (OCE30) for core-related debug and profiling support.
  - Debug and profiling unit (DPU) for platform level debug and profiling support.
  - Debug state, single stepping, and command insertion from the host debugger.
  - Test Access Port (TAP) designed to comply with **IEEE®** Std. 1149.1™.
  - Breakpoints on PC, data address, and data bus values.
  - More than 40 event counting options in 6 parallel counters
  - Cache debug mode enables cache state observation (cache array, tags, valid, and dirty bits) and DCache array content modification
  - Real-time tracing of PC, task ID, and profiling information to the main memory with the virtual trace write buffer
— Low-power design with the following modes of operation:
  - Wait processing state in which the core clocks and caches are gated but peripherals continue to operate
  - Stop processing state for full clock gating.

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- StarCore SC3400 DSP Core. Each high-performance core is binary compatible with the SC140 core used in the MSC81xx DSP family and the SC1400 core used in the MSC711x DSP family and delivers up to 3200/4000 16-bit MMACS using an internal 800 MHz/1 GHz clock at 1 V. Each core includes:
  - Data arithmetic and logic unit (DALU) containing 4 ALUs
  - Address generation unit (AGU) containing two address arithmetic units
  - Up to six instructions execute in a single clock cycle
  - Variable-length execution set (VLES) that can be optimized for code density and performance
  - 16 data registers, 40 bits each
  - 27 address registers, 32 bits each
  - Hardware support for fractional and integer data types
  - Four hardware loops with zero overhead
  - Very rich 16-bit wide orthogonal instruction set
  - Application-specific instructions for video and baseband processing.
  - Special single instruction, multiple data (SIMD) instructions working on 2-word or 4-byte operands packed in a register. Can perform 2 to 4 operations per instruction (8 to 16 operations per VLES). The SIMD instruction supports 2×8-bit multiply and 20-bit accumulate operation.
  - Dynamic interlocking for friendlier programming and more efficient compiler support.
  - User and supervisor privilege levels supporting a protected software model.
  - Precise memory access exceptions enables good RTOS support and soft error corrections.
  - Branch target buffer (BTB) accelerates change-of-flow operations.
- Chip-level arbitration and switching system (CLASS)
  - A full fabric that arbitrates between the processing elements and other initiators to the shared M2 memory, DDR SDRAM controller, the device configuration control and status registers (CCSRs) and other targets.
  - High bandwidth.
  - Non-blocking allows parallel accesses from multiple initiators to multiple targets.
  - Fully pipelined.
  - Low latency.
  - Per target arbitration highly optimized to the target characteristics using prioritized round-robin arbitration.
  - Reduces data flow bottlenecks and enables high-bandwidth internal data transfers.
- Internal memory. The 10.96-Mbyte internal memory space includes:
  - 16 Kbytes ICache.
  - 32 Kbytes DCache.
  - 128 Kbytes L2 shared ICache.
    - Organized in two interleaved banks of 64 Kbyte each.
    - Banks can have simultaneous access.
    - 8-way set associative.

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- – Pass-through port for L2 non-cacheable instructions.
- – Optimized to accelerate core code execution from M3 memory and DDR memory.
- — 512-Kbyte M2 low-latency memory for critical data and temporary data buffering. Accessible from all CLASS masters via four interleaved ports.
    - – Runs at up to 400 MHz.
    - – Four address-interleaved banks.
    - – 128-bit wide port per bank.
    - – Up to four simultaneously accesses.
    - – Burstable access support.
- — 10-Mbyte 128-bit wide M3 memory accessed at up to 400 MHz. Accessible from all DSP subsystems and all CLASS masters. Most applications run with no external memory.
    - – Hidden refresh with low probability of conflict with core accesses.
    - – Burstable accesses.
- — 96-Kbyte boot ROM accessible from the core.

- Clocks
    - — Three input clocks:
        - – Shared input clock.
        - – Global input clock (PCI PLL).
        - – Differential input clock (SRIO PLL).
    - — Four PLLs:
        - – System PLL
        - – Core PLL
        - – Global PLL
        - – Serial RapidIO PLL.
    - — Clock ratios selected during reset via reset configuration pins.
    - — Clock modes user-configurable after reset.

- Security Engine Core (SEC). The SEC is optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP.
    - — Four crypto-channels, each supporting multi-command descriptor chains
    - — Dynamic assignment of crypto-execution units via an integrated controller
    - — Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
    - — PKEU—public key execution unit
        - – RSA and Diffie-Hellman; programmable field size up to 2048 bits
        - – Elliptic curve cryptography with F2m and F(p) modes and programmable field size up to 511 bits
    - — DEU—Data Encryption Standard (DES) execution unit
        - – DES, 3DES
        - – Two key (K1, K2, K1) or three key (K1, K2, K3)

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- – ECB and CBC modes for both DES and 3DES
  — AESU—Advanced Encryption Standard (AES) unit
  - – Implements the Rijndael symmetric key cipher
  - – ECB, CBC, CTR, and CCM modes
  - – 128-, 192-, and 256-bit key lengths
  — AFEU—ARC four execution unit
  - – Implements a stream cipher compatible with the RC4 algorithm
  - – 40- to 128-bit programmable key
  — MDEU—message digest execution unit
  - – SHA with 160- or 256-bit message digest
  - – MD5 with 128-bit message digest
  - – HMAC with either algorithm
  — KEU—Kasumi execution unit
  - – Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - – Also supports A5/3 and GEA-3 algorithms
  — RNG—random number generator
  — XOR engine accelerates parity checking in RAID storage applications
- DDR Controller
  — Up to 200 MHz clock rate (400 MHz data rate).
  — 16/32-bit DDR SDRAM data bus.
  — Supported memory includes 64 Mbits to 4 Gbits DDR and DDR2 devices with x8/x16 data ports (no direct x4 support).
  — DDR SDRAM chip configurations up to 1 Gbyte, including:
  - – Up to two physical banks (chip selects), each independently addressable.
  - – 32/40-bit SDRAM data bus and 16/24-bit SDRAM data bus for DDR and DDR2.
  — Up to two memory chip selects with each chip select independently addressable.
  — Four or eight sub-banks per chip select.
  — DDR SDRAM timing parameters are fully programmable.
  — Data mask (DM) signal and read-modify-write (RMW) for writing less than 4 bytes.
  — Open page management (up to four open pages).
  — Double-bit error detection and single-bit error correction (8 ECC bits).
  — Sleep power management.
  — DDR controller clock independent of the DSP clock to maximize memory performance while decoupling connection to the system clock.
- DMA Controller
  — 32 unidirectional channels, providing up to 16 memory-to-memory channels.
  — Buffer descriptor programming model.

— Up to 1024 buffer descriptors per channel direction provide a total of 32 Kbyte buffer descriptors. Buffer descriptors can reside in M2 or DDR memory.

— Priority-based time-multiplexing between channels, using four internal priority groups with round-robin arbitration between channels on equal priority group.

— Earliest deadline first (EDF) priority scheme that assures task completion on time.

— Flexible channel configuration with all channels supporting all features.

— A flexible buffer configuration, including:

  – Simple buffers

  – Cyclic buffers

  – Single address buffers (I/O device).

  – Incremental address buffers

  – Chained buffers

  – 1D to 4D buffers, optimized for video applications

  – 1D or 2–4D complex buffers, a combination of buffer types

— High bandwidth

— Optimized for DDR SDRAM

- TDM

— Backward-compatible with the MSC8102/MSC8122/MSC8126 TDM interface

— All the eight TDM modules together support up to 2K time-slots for receive and 2K time-slots for transmit

— Up to eight independent TDM modules:

  – *Independent receive and transmit mode*. Independent transmitter and receiver. Transmitter input clock, output data, and frame sync can be configured as either input or output. Up to 256 transmit channels and up to 256 receive channels. Receiver input clock, input data, and input frame sync.

  – *Shared sync and clock mode*. Two receive and two transmit links share the same clock and frame sync. The sync can be configured as either input or output. Up to 128 transmit channels and 128 receive channels.

  – *Shared data link*. Up to four full-duplex data links can operate as either transmit or receive. All links have the same clock and frame sync. Each link supports up to 128 channels.

— Word size of 2, 4, 8, or 16-bit. All the channels share the same size.

— Hardware A-law/μ-law conversion

— Up to 128 Mbps data rate for all TDM modules

— Up to 16 Mbyte per channel buffer (granularity 8 bytes), where A/μ law buffer size has double size (16-byte granularity)

— Separate or shared interrupts for receive and transmit with two programmable receive and two programmable transmit thresholds for double buffering

— Each channel can be programmed as active or inactive

— Support either 0.5 ms (4 frames) or 1 ms (8 frames) latency

- — Glueless interface to E1/T1 framers
- — Can interface with H-MVIP/H.110 device, TSI, and codecs such as AC-97
- The QUICC Engine subsystem includes dual RISC processors and 48-Kbyte multi-master RAM to handle the Ethernet and ATM interfaces, thus offloading the tasks from the cores. The three communication controllers support:
  - — Two Ethernet controllers supporting 10/100/1000 Mbps operation
  - — ATM controller supporting AAL0, AAL2, and AAL5
  - — SPI
- Ethernet Controllers
  - — Five Ethernet physical interfaces:
    - – 10/100 Mbps MII (one controller only)
    - – 10/100 Mbps RMII (consortium standard)
    - – 10/100 Mbps SMII
    - – Designed to comply with the SGMII protocol using a 4-pin SerDes interface at 1000 Mbps data rate only
    - – 10/100/1000 Mbps RGMII (full duplex only)
  - — MAC-to-MAC connection in all modes
  - — Half- and full-duplex operations in 10/100 Mbps mode
  - — Half-duplex back-pressure (10/100 Mbps only)
  - — Full-duplex operations in 1000 Mbps mode
  - — Full-duplex flow control feature (**IEEE** Std. 802.3x™)
  - — Receive flow control frames
  - — Detection of all erroneous frames as defined by **IEEE** Std. 802.3-2002™
  - — Multi-buffer data structure
  - — Diagnostic modes: Internal and external loopback mode and echo mode
  - — Serial management interface MDC/MDIO
  - — Transmitter network management and diagnostics
  - — Receiver network management and diagnostics
  - — VLAN Support
  - — **IEEE** Std. 802.1p/Q™ QoS
  - — Eight Tx/Rx queues
  - — Queuing decision for IP/MAC/UDP filtering based on MAC destination addresses, IP destination address, and UDP destination port
  - — Programmable maximum frame length
  - — Enhanced MIB statistics
  - — Optional shift of data buffer by two bytes for L3 header alignments
  - — Extended features
    - – IP header checksum verification and calculation

- – Parsing of frame headers and adding a frame control block at the frame head, containing L3 and L4 information for CPU acceleration
- Universal test and operations PHY interface for ATM (UTOPIA) controller:
  - UTOPIA level II supports 8/16 bits 25/50 MHz
  - UTOPIA slave mode
  - Cell-level handshake
  - Multiple-PHY polling mode
  - ATM adaptation layers support AAL0, AAL2, and AAL5 protocols in hardware
  - Full duplex segmentation and reassembly at up to 622 Mbps for AAL5
  - Full duplex segmentation and reassembly at up to 155 Mbps for AAL2
  - Up to 255 active VCs internally and up to 64 K VCs using external memory
  - Unassign cells screening option
  - Internal rate transmit mode
  - User-defined cells up to 65 bytes
  - Separate TxBD and RxBD tables for each virtual channel (VC)
  - Special mode of global free buffer pools for dynamic and efficient memory allocation with early packet discard (EPD) support
  - Interrupt report per channel using four priority interrupt queues
  - Compliant with ATMF UNI 4.0 and ITU specification
  - ATM pace control (APC) unit
  - Receive address look-up mechanism
  - Operations and maintenance (OAM) cell
  - ATM layer statistic gathering on a per PHY basis
- SPI
- PCI
  - Designed to be compliant with the PCI specification revision 2.2 per the voltage specifications in the *MSC8144E Technical Data Sheet*
  - 33 MHz and 66 MHz
  - 32-bit PCI interface
  - Supports host and agent modes
  - PCI 3.3-V compatible
  - Accesses to all PCI address spaces
  - PCI-to-system and system-to-PCI streaming
- Serial RapidIO Subsystem
  - Serial RapidIO Port (SRIO) 1x/4x serial RapidIO endpoint complies with the following parts of Specification 1.2 of the RapidIO trade association interconnect specification:
    - – Part I (input and output logical specifications)
    - – Part II (message passing logical specification)

- – Part III (common transport specification)
- – Part VI (physical layer 1x/4x LP-serial specification)
- – Part VIII (error management extension specification)
- — The serial RapidIO port supports read, write, messages, doorbells, and maintenance accesses in inbound mode, and messages and doorbells accesses in outbound mode:
  - – Small and large transport information field only
  - – All priorities flow
- — RapidIO Messaging Unit
  - – Two outbound message queues
  - – Two inbound message queues
  - – One outbound doorbell queue
  - – One inbound doorbell queue
  - – One inbound port-write queue
- • I/O Interrupt Concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes them to INT_OUT, NMI_OUT, and the cores.
- • UART
  - — Bit rate up to 6.25 Mbps
  - — Two signals for transmit data and receive data
  - — Full-duplex operation
  - — Standard mark/space non-return-to-zero (NRZ) format
  - — 13-bit baud rate selection
  - — Programmable 8-bit or 9-bit data format
  - — Separately enabled transmitter and receiver
  - — Programmable transmitter output polarity
  - — Separate receiver and transmitter interrupt requests
  - — Receiver framing error detection
  - — Hardware parity checking
  - — 1/16 bit-time noise detection
  - — Single-wire and loop operations
- • Timers
  - — Two general-purpose 32-bit timers for RTOS support per SC3400 core
  - — Four TMR modules, each with the following features:
    - – Four 16-bit timers
    - – Cascadable timers
    - – Count up/down
    - – Programmable count modulo
    - – Count once or repeatedly
    - – Counters are preload able

- – Compare registers can be preloaded
- – Counters can share available inputs
- – Separate prescaler for each counter
- – Each counter has capture and compare capability
- – Can use one of the following clock sources: system clock, TDM clock input, or external clock input
- — Four software watchdog timer (SWT) modules
- General-purpose input/output (GPIO) ports:
  - — 32 GPIO ports
  - — Each GPIO port can either serve the on-device peripherals or act as a programmable I/O pin
  - — Sixteen GPIO pins can be configured as external interrupt inputs
  - — All ports are bidirectional
  - — All ports are set as GPIO inputs at system reset
  - — All port values can be read while the pin is connected to an internal peripheral
  - — All ports have open-drain output capability
- I^2C interface
  - — Two-wire interface
  - — Multi-master operational
  - — Calling address identification interrupt
  - — START and STOP signal generation/detection
  - — Acknowledge bit generation/detection
  - — Bus busy detection
  - — Programmable clock frequency
  - — On-chip filtering for spikes on the bus
- Serial peripheral interface (SPI)
- Eight programmable hardware semaphores, locked by simple write access without need for read-modify-write operation by the DSP core.
- Virtual interrupts
  - — Generation of 32 virtual interrupts by a simple write access
  - — Generation of virtual $\overline{\text{NMI}}$ by a simple write access
- Boot interface options:
  - — Serial RapidIO port
  - — PCI
  - — I^2C
  - — Ethernet
- JTAG. Test Access Port (TAP) and Boundary Scan Architecture designed to comply with **IEEE** Std. 1149.1.
- Reduced power dissipation

— Very low power CMOS design

— All modules but the DSP subsystem run at 50 percent of the DSP core frequency or less

— Low-power standby modes

— Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

- Technology. The MSC8144E device is manufactured using CMOS 90 nm SOI technology.

3 Developer Environment

Freescale supplies a complete set of DSP development tools for the MSC8144E device. Our tools are focused on providing easier and more robust ways for designers to develop optimized DSP systems. Whether the application targets a wireless base station, IP telephony, or transcoding media gateways, the development environment gives the designers everything they need to exploit the advanced capabilities of the MSC8144E architecture.

3.1 Tools

The MSC8144E tool components include the following:

- *Integrated development environment (IDE)*. Easy-to-use graphical user interface and project manager for configuring and managing multiple build configurations.

- *C compiler with in-line assembly*. The developer can generate highly optimized DSP code by exploiting the StarCore multiple-ALU architecture, with parallel fetch sets and high code density.

- *Librarian*. The developer can create application-specific DSP libraries for modularity.

- *Linker*. The developer can efficiently produce executables from object code and partition memory according to the application architecture; the linker supports code overlay.

- *Debugger*. Seamlessly integrated real-time, non-intrusive, multi-mode and multi-DSP debugger handles highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. Supports RTOS-aware debugger.

- *Royalty-free RTOS*. Included with package.

- *Software Simulator*. Full chip simulation; the developer can design an application and run it on the simulator before running it on the silicon. FCS integrated under IDE, the simulator provides customers with tools to create projects and debug them as they would on silicon.

- *Profiler*. The developer can analyze and identify program design inefficiencies.

- *Data Visualization*. Lets the developer graph variables, registers, regions of memory, and HSST data streams as they change over time. By changing the visualization filter, you can plot this data in a variety of ways; including line charts, logarithmic charts, polar coordinates, and scatter graphs.

- *High Speed Run Control*. PowerTAP high speed host-target interface allows users to program in Flash memory, ROM, and cache.

- *Host Platform Support*. Microsoft Windows and Solaris.

- *Development Board*. The application development system (ADS).

- *Kit for MSC8144E*. A complete system for developing and debugging real-time hardware and software. The kit includes the MSC8144E device with a companion memory, JTAG debug interface, Ethernet interface, PCI interface, digital video interfaces and software device drivers.

3.2 Application Software

Freescale offers a broad range of DSP applications through its third-party application software partners; these applications target IP telephony, telephony modem, wireless and multimedia transcoding, and wireless base stations. Applications and software modules are listed in **Table 1**.

Table 1. Application Software Modules

Application	Modules
ETSI/3GPP1 Vocoders	GSM-FR, GSM-HR, GSM-AMR/EFR, 3GPP AMR-WB
TIA/3GPP2 Vocoders	IS127 EVRC, IS893 SMW
ITU G.7xx Vocoders	G.711, G.711 App. 1 and 2 (PLC and VAD/CNG), G.722, G.723.1, G.726, G.726A, G.728, G.729B, G.729AB, G.729E
Modems	Pumps: V.23 CallerID, V.34, V.90, V.92
	V.42 MNP4 (error correction)
	Compression: V.44, V.42bis, MNP5
	Negotiation: V.8, V.8bis
	HDLC
	Relay: V.150.1 (MoIP)
Fax	Pumps: V.17, V.27ter, V.29
	Relay: T.30 (FoIP), T.38
Echo cancellation	G.165, G.168 (64 ms), G.168 2004 (128 ms, windowed), noise reduction, acoustic level control, Acoustic EC (roadmap)
Telephony support	DTMF detection, universal tone generation, special tone event detect, VAD/CNG, PLC, RTP packetization
Security	AES
Video	MPEG4, H.263, H.264, H.324MDSP (roadmap)
Device Driver	DMA driver, SRIO driver, TDM driver, Ethernet driver, PCI driver, UTOPIA driver, UART driver, memory allocation, interrupt handling

In addition, Freescale provides a complete VoIP framework for channel scheduling, explicit DMA management of channel state data, memory management, network termination, peripheral drivers, framework control API command/status, and more. The Framework is shown in **Figure 8**. Notice that physical drivers are encapsulated in a SmartDSP OS, thus ensuring ease of transfer between different hardware implementations.
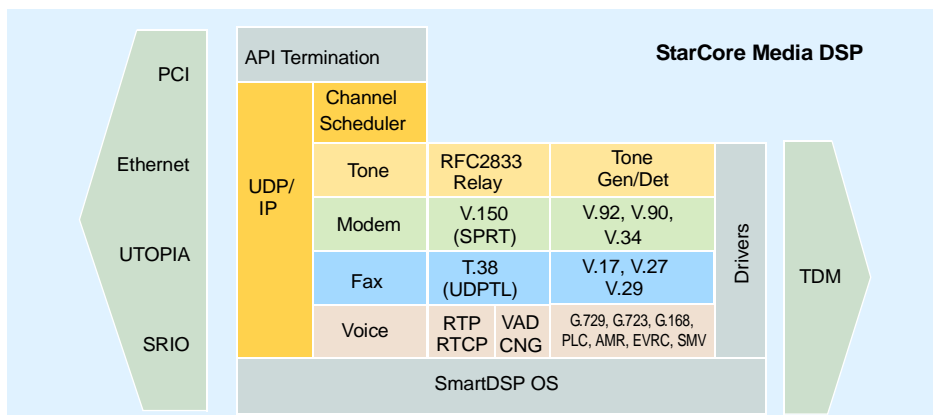
Figure 8. Application Software Model

4　Document Revision History

Table 2 provides a revision history for this product brief.

Table 2. Document Revision History

Rev. No.	Substantive Change(s)
0	This is the first release of this document.
1	Removes preview notice because part is qualified and updates contact information on back page.

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