## **MN6474A**

## D/A Converter for Digital Audio Equipment

#### Overview

The MN6474A is a CMOS digital-to-analog converter with a built-in 16-bit digital filter for pulse code modulation (PCM) digital audio equipment.

It uses noise shaping technology to convert a digital signal into a PWM signal.

It contains a 4-fold oversampling digital filter that permits simplification of the low pass filter after the D/A converter, thus greatly reducing the power consumption of the entire D/A conversion system.

The chip provides both regular and inverted phase outputs for both channels.

The chip contributes to cost and size reductions for CD players and other digital audio equipment.

#### Features

• Built-in 4-fold oversampling digital filter

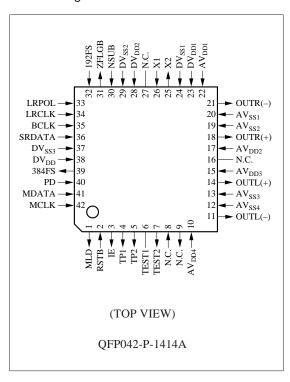
(ripple of only  $\pm 0.0072$  dB within the supported band and attenuation of 62.7 dB within the cutoff band)

- Internal resolution of 18 bits
- Two's complement input (I<sup>2</sup>S input code also supported)
- Built-in overflow limiter
- No zero cross distortion
- Sample-and-hold circuit is unnecessary
- Output pin for detecting zero input
- Single 5V power supply

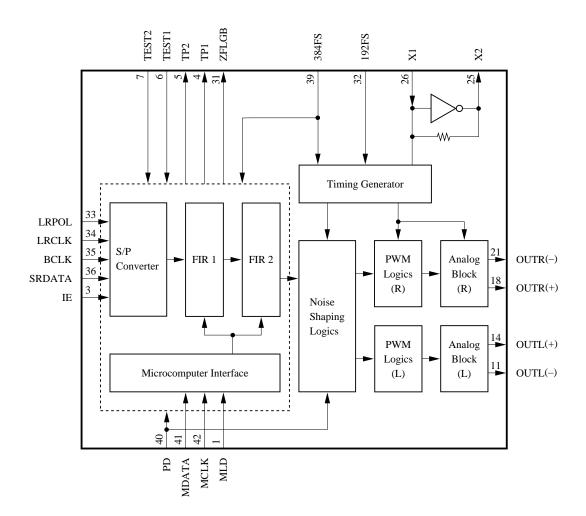
#### Applications

• CD players and other digital audio equipment

#### ■ Pin Assignment



### ■ Block Diagram



## ■ Pin Descriptions

| Pin No. | Symbol                              | Function Description  |  |  |  |  |  |  |
|---------|-------------------------------------|---|--|--|--|--|--|--|
| 1       | MLD                                 | Microcomputer command load input ("L" level to load)                                      |  |  |  |  |  |  |
| 2       | RSTB                                | Reset pin (active "L").   |  |  |  |  |  |  |
| _       | ROID                                | Always pull this pin low after applying the power.  |  |  |  |  |  |  |
| 3       | IE                                  | Input format selection pin. "H" level; I <sup>2</sup> S format                            |  |  |  |  |  |  |
| 5       | IL.                                 | "L" level; signal processing LSI format.  |  |  |  |  |  |  |
| 4       | TP1                                 | Digital filter test output pin 1. Leave this pin open.                                    |  |  |  |  |  |  |
| 5       | TP2                                 | Digital filter test output pin 2. Leave this pin open.                                    |  |  |  |  |  |  |
| 6       | TEST1                               | Digital filter test input pin 1. Keep this pin at "L" level.                              |  |  |  |  |  |  |
| 7       | TEST1                               |   |  |  |  |  |  |  |
| 8       | N.C.                                |   |  |  |  |  |  |  |
| 9       | N.C.                                | No connection Leave these pins open.  No connection Leave these pins open.                |  |  |  |  |  |  |
| 10      |                                     | <u> </u>  |  |  |  |  |  |  |
| 11      | AV <sub>DD4</sub>                   | Power supply pin 4 for analog circuits. (+5V)   |  |  |  |  |  |  |
|         | OUTL(-)                             | Left channel inverted phase PWM output pin.   |  |  |  |  |  |  |
| 12      | AV                                  | Ground pin 4 for analog circuits.   |  |  |  |  |  |  |
| 13      | AV <sub>SS3</sub>                   | Ground pin 3 for analog circuits.   |  |  |  |  |  |  |
| 14      | OUTL(+)                             | Left channel normal phase PWM output pin.   |  |  |  |  |  |  |
| 15      | AV <sub>DD3</sub>                   | Power supply pin 3 for analog circuits. (+5V)   |  |  |  |  |  |  |
| 16      | N.C.                                | No connection Leave this pin open.  |  |  |  |  |  |  |
| 17      | AV <sub>DD2</sub>                   | Power supply pin 2 for analog circuits. (+5V)   |  |  |  |  |  |  |
| 18      | OUTR(+)                             | Right channel through phase PWM output pin.   |  |  |  |  |  |  |
|         | AV <sub>SS2</sub>                   | Ground pin 2 for analog circuits.   |  |  |  |  |  |  |
|         | AV <sub>SS1</sub>                   | Ground pin 1 for analog circuits.   |  |  |  |  |  |  |
| 21      | OUTR(-)                             | Right channel inverted phase PWM output pin.  |  |  |  |  |  |  |
| 22      | AV <sub>DD1</sub>                   | Power supply pin 1 for analog circuits. (+5V)   |  |  |  |  |  |  |
| 23      | DV <sub>DD1</sub>                   | Power supply pin 1 for digital circuits. (+5V) (Power supply for oscillator circuit)      |  |  |  |  |  |  |
| 24      | DV <sub>SS1</sub>                   | Ground pin 1 for digital circuits. (Ground for oscillator circuit)                        |  |  |  |  |  |  |
| 25      | X2                                  | Crystal oscillator pin.   |  |  |  |  |  |  |
| 26      | X1                                  | Crystal oscillator pin. (External clock input pin)  |  |  |  |  |  |  |
| 27      | N.C.                                | No connection Leave this pin open.  |  |  |  |  |  |  |
| 28      | $\mathrm{DV}_{\mathrm{DD2}}$        | Power supply pin 2 for analog circuits. (+5V)   |  |  |  |  |  |  |
| 29      | DV <sub>SS2</sub>                   | Ground pin 2 for digital circuits.  |  |  |  |  |  |  |
| 30      | NSUB                                | Connect to D-V <sub>DD</sub> . (Silicon substrate potential fixing pin)                   |  |  |  |  |  |  |
| 31      | ZFLGB                               | Output pin for detecting zero input.  |  |  |  |  |  |  |
| 32      | 192FS                               | 192f <sub>s</sub> (=9.216 MHz)output pin. Max. load capacity: 30 pF.                      |  |  |  |  |  |  |
| 33      | LRPOL                               | LRCLK polarity selection pin. "H" level; selects the left channel                         |  |  |  |  |  |  |
|         |                                     | "L" level; the right channel.   |  |  |  |  |  |  |
| 34      | LRCLK                               | LRCLK pin. When the LRPOL pin is at "H" level, "H" level in this pin indicates left       |  |  |  |  |  |  |
|         |                                     | channel data input; "L" level indicates right channel data input. When the LRPOL pin      |  |  |  |  |  |  |
|         |                                     | is at "L" level, "L" level in this pin indicates left channel data input; "H" level input |  |  |  |  |  |  |
|         | indicates right channel data input. |   |  |  |  |  |  |  |
| 35      | BCLK                                | Serial input bit clock  |  |  |  |  |  |  |
| 36      | SRDATA                              | Serial input data (digital) input pin.  |  |  |  |  |  |  |
| 37      | DV <sub>SS3</sub>                   | Ground pin 3 for digital circuits.  |  |  |  |  |  |  |

## ■ Pin Descriptions (continued)

| Pin No. | Symbol           | Function Description   |  |  |  |  |  |
|---------|------------------|--|--|--|--|--|--|
| 38      | DV <sub>DD</sub> | Power supply pin for digital circuits. (Silicon substrate potential fixing pin.) (+5V) |  |  |  |  |  |
| 39      | 384FS            | 384f <sub>s</sub> (=18.432 MHz) output pin. Max. load capacitance: 30 pF.              |  |  |  |  |  |
| 40      | PD               | Power down pin. (active "H")   |  |  |  |  |  |
| 41      | MDATA            | Microcomputer command data input pin.  |  |  |  |  |  |
| 42      | MCLK             | Clock input pin for microcomputer command.   |  |  |  |  |  |

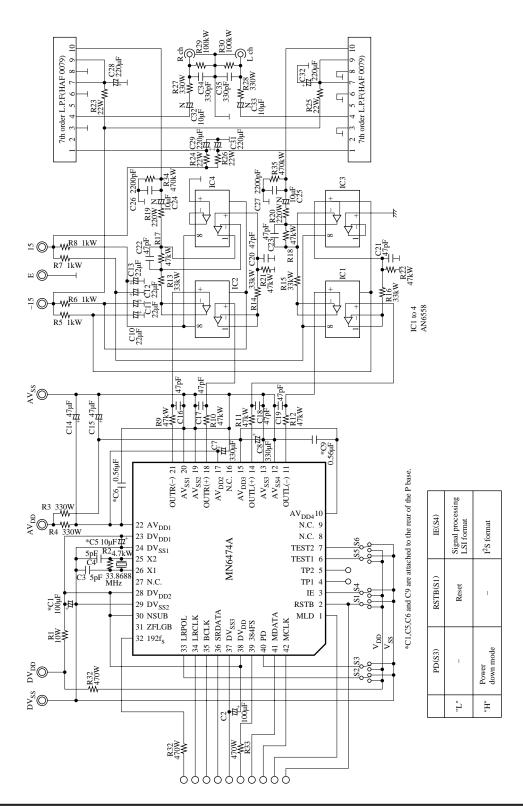
#### ■ Conversion Characteristics

 ${\rm DV_{DD}}{=}5.0{\rm V},\,{\rm DV_{SS}}{=}0{\rm V},\,{\rm AV_{DD}}{=}5.0{\rm V},\,{\rm AV_{SS}}{=}0{\rm V},\,{\rm f}{=}33.8688{\rm MHz},\,{\rm Ta}{=}25^{\circ}{\rm C}$ 

| Parameter                 | Symbol | Test Conditions | min | typ   | max   | Unit             |  |  |  |  |
|---------------------------|--------|-----------------|-----|-------|-------|------------------|--|--|--|--|
| Analog characteristics    |        |                 |     |       |       |                  |  |  |  |  |
| Signal-to-noise ratio     | S/N    | EIAJ (1kHz)     | 95  | 106   |       | dB               |  |  |  |  |
| Dynamic range             | D.R.   | EIAJ (1kHz)     | 90  | 98    |       | dB               |  |  |  |  |
| Total harmonic distortion | THD+N  | EIAJ (1kHz)     |     | 0.003 | 0.005 | %                |  |  |  |  |
| Crosstalk                 |        | EIAJ (1kHz)     | 90  | 98    |       | dB               |  |  |  |  |
| Output level *1           |        | 1kHz F.S.       | 1.4 | 1.7   |       | V <sub>rms</sub> |  |  |  |  |

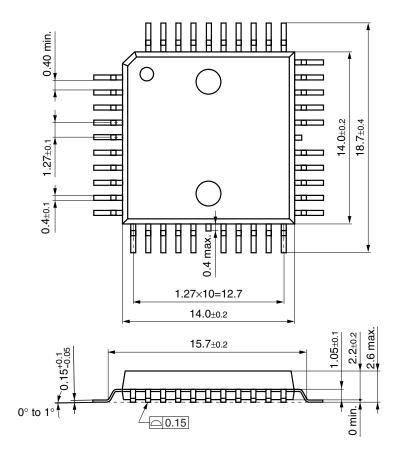
Note\*1: These analog characteristics are for circuits equivalent to the suggested application circuit.

#### ■ Application Circuit Example



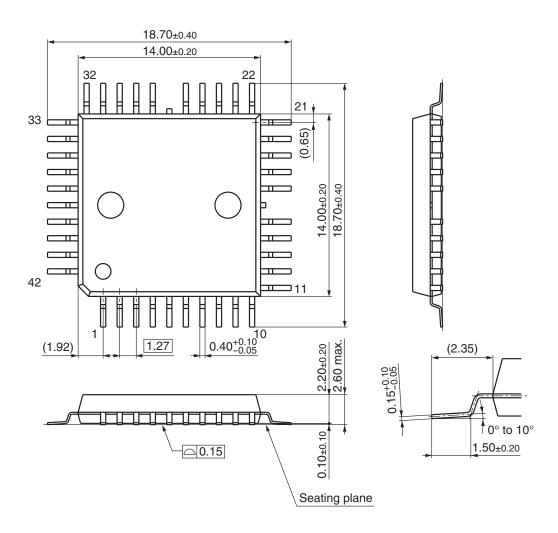
## ■ Package Dmensions (Unit: mm)

## QFP042-P-1414A



Note) The package of this product will be changed to the following lead-free type (QFP042-P-1414D).

- New Package Dimensions (Unit: mm)
- QFP042-P-1414D (Lead-free package)



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