National Semiconductor

# MM54HC4051/MM74HC4051 <br> 8-Channel Analog Multiplexer MM54HC4052/MM74HC4052 Dual 4-Channel Analog Multiplexer MM54HC4053/MM74HC4053 Triple 2-Channel Analog Multiplexer 

## General Description

These multiplexers are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to $\pm 6 \mathrm{~V}$ (peak) analog signals with digital control signals of 0 to 6 V . Three supply pins are provided for $\mathrm{V}_{\mathrm{C}}$, ground, and $\mathrm{V}_{\mathrm{EE}}$. This enables the connection of $0-5 \mathrm{~V}$ logic signals when $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and an analog input range of $\pm 5 \mathrm{~V}$ when $\mathrm{V}_{\mathrm{EE}}=5 \mathrm{~V}$. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to $\mathrm{V}_{\mathrm{CC}}$ and ground.
MM54HC4051/MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is "on", and connects one of the eight inputs to the common output.
MM54HC4052/MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving
a pair of 4-channel multiplexers. The binary code placed on the $A$, and $B$ select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4-channel differential multiplexer.
MM54HC4053/MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configurations. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

## Features

- Wide analog input voltage range: $\pm 6 \mathrm{~V}$
- Low "on" resistance: 50 typ. ( $\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}=4.5 \mathrm{~V}$ )

30 typ. ( $\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}=9 \mathrm{~V}$ )

- Logic level translation to enable 5 V logic with $\pm 5 \mathrm{~V}$ analog signals
■ Low quiescent current: $80 \mu \mathrm{~A}$ maximum ( 74 HC )
- Matched Switch characteristic

Connection Diagrams


See the CMOS Logic Databook for Complete Specifications

