

# MM74C221

## Dual Monostable Multivibrator

### General Description

The MM74C221 dual monostable multivibrator is a monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components  $C_{EXT}$  and  $R_{EXT}$ . The pulse width is stable over a wide range of temperature and  $V_{CC}$ .

Pulse stability will be limited by the accuracy of external timing components. The pulse width is approximately defined by the relationship  $t_{W(OUT)} \approx C_{EXT} R_{EXT}$ . For further information and applications, see AN-138.

### Features

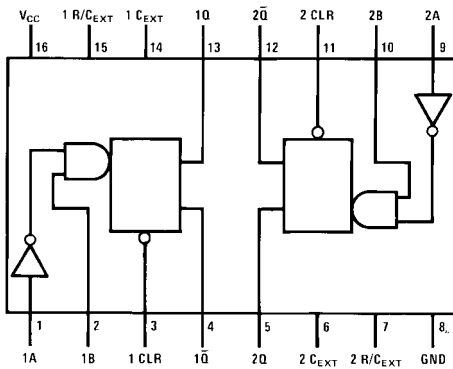
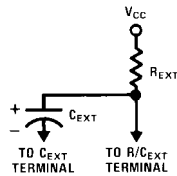
- Wide supply voltage range: 4.5V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45  $V_{CC}$  (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L

### Ordering Code:

| Order Number | Package Number | Package Description  |
|--------------|----------------|--|
| 74MMC221N    | N16E           | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

### Connection Diagrams

#### Timing Component



Top View

### Truth Table

| Inputs |   |   | Outputs |                |
|--------|---|---|---------|----------------|
| Clear  | A | B | Q       | $\overline{Q}$ |
| L      | X | X | L       | H              |
| X      | H | X | L       | H              |
| X      | X | L | L       | H              |
| H      | L | ↑ | ⌋       | ⌋              |
| H      | ↓ | H | ⌋       | ⌋              |

H = HIGH Level  
L = LOW Level  
X = Irrelevant  
↑ = Transition from LOW-to-HIGH  
↓ = Transition from HIGH-to-LOW  
⌋ = One HIGH Level Pulse  
⌋ = One LOW Level Pulse

**Absolute Maximum Ratings**(Note 1)

|   |                          |
|---|--------------------------|
| Voltage at Any Pin                          | -0.3V to $V_{CC} + 0.3V$ |
| Operating Temperature Range                 | -55°C to +125°C          |
| Storage Temperature Range                   | -65°C to +150°C          |
| Power Dissipation                           |                          |
| Dual-In-Line                                | 700 mW                   |
| Small Outline                               | 500 mW                   |
| Operating $V_{CC}$ Range                    | 4.5V to 15V              |
| Absolute Maximum $V_{CC}$                   | 18V                      |
| $R_{EXT} \geq 80 V_{CC} (\Omega)$           |                          |
| Lead Temperature<br>(Soldering, 10 seconds) | 260°C                    |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

**DC Electrical Characteristics**

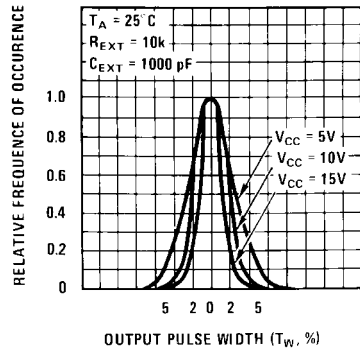
Max/min limits apply across temperature range, unless otherwise noted

| Symbol  | Parameter                                 | Conditions  | Min            | Typ     | Max        | Units    |
|---|---|---|----------------|---------|------------|----------|
| <b>CMOS to CMOS</b>   |   |   |                |         |            |          |
| $V_{IN(1)}$   | Logical "1" Input Voltage                 | $V_{CC} = 5V$<br>$V_{CC} = 10V$   | 3.5<br>8.0     |         |            | V        |
| $V_{IN(0)}$   | Logical "0" Input Voltage                 | $V_{CC} = 5V$<br>$V_{CC} = 10V$   |                |         | 1.5<br>2.0 | V        |
| $V_{OUT(1)}$  | Logical "1" Output Voltage                | $V_{CC} = 5V, I_O = -10 \mu A$<br>$V_{CC} = 10V, I_O = -10 \mu A$   | 4.5<br>9.0     |         |            | V        |
| $V_{OUT(0)}$  | Logical "0" Output Voltage                | $V_{CC} = 5V, I_O = +10 \mu A$<br>$V_{CC} = 10V, I_O = +10 \mu A$   |                |         | 0.5<br>1   | V        |
| $I_{IN(1)}$   | Logical "1" Input Current                 | $V_{CC} = 15V, V_{IN} = 15V$  |                | 0.005   | 1.0        | $\mu A$  |
| $I_{IN(0)}$   | Logical "0" Input Current                 | $V_{CC} = 15V, V_{IN} = 0V$   | -1.0           | -0.005  |            | $\mu A$  |
| $I_{CC}$  | Supply Current (Standby)                  | $V_{CC} = 15V, R_{EXT} = \infty$ ,<br>Q1, Q2 = Logic "0" (Note 2)   |                | 0.05    | 300        | $\mu A$  |
| $I_{CC}$  | Supply Current<br>(During Output Pulse)   | $V_{CC} = 15V, Q1 = \text{Logic "1"}$ ,<br>Q2 = Logic "0" (Figure 4)<br>$V_{CC} = 5V, Q1 = \text{Logic "1"}$ ,<br>Q2 = Logic "0" (Figure 4) |                | 15<br>2 |            | mA<br>mA |
|   | Leakage Current at R/C <sub>EXT</sub> Pin | $V_{CC} = 15V, V_{C_{EXT}} = 5V$  |                | 0.01    | 3.0        | $\mu A$  |
| <b>CMOS/LPTTL Interface</b>   |   |   |                |         |            |          |
| $V_{IN(1)}$   | Logical "1" Input Voltage                 | $V_{CC} = 4.75V$  | $V_{CC} - 1.5$ |         |            | V        |
| $V_{IN(0)}$   | Logical "0" Input Voltage                 | $V_{CC} = 4.75V$  |                |         | 0.8        | V        |
| $V_{OUT(1)}$  | Logical "1" Output Voltage                | $V_{CC} = 4.75V, I_O = -360 \mu A$  | 2.4            |         |            | V        |
| $V_{OUT(0)}$  | Logical "0" Output Voltage                | $V_{CC} = 4.75V, I_O = 360 \mu A$   |                |         | 0.4        | V        |
| <b>Output Drive (See Family Characteristics Data Sheet) (Short Circuit Current)</b> |   |   |                |         |            |          |
| $I_{SOURCE}$  | Output Source Current<br>(P-Channel)      | $V_{CC} = 5V$<br>$T_A = 25^\circ C, V_{OUT} = 0V$   | -1.75          |         |            | mA       |
| $I_{SOURCE}$  | Output Source Current<br>(P-Channel)      | $V_{CC} = 10V$<br>$T_A = 25^\circ C, V_{OUT} = 0V$  | -8             |         |            | mA       |
| $I_{SINK}$  | Output Sink Current<br>(N-Channel)        | $V_{CC} = 5V$<br>$T_A = 25^\circ C, V_{OUT} = V_{CC}$   | 1.75           |         |            | mA       |
| $I_{SINK}$  | Output Sink Current<br>(N-Channel)        | $V_{CC} = 10V$<br>$T_A = 25^\circ C, V_{OUT} = V_{CC}$  | 8              |         |            | mA       |

**Note 2:** In Standby (Q = Logic "0") the power dissipated equals the leakage current plus  $V_{CC}/R_{EXT}$ .

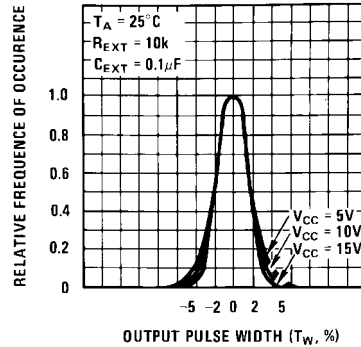
| <b>AC Electrical Characteristics</b> (Note 3)   |  |  |   |                        |          |               |
|---|--|--|---|------------------------|----------|---------------|
| $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , unless otherwise noted  |  |  |   |                        |          |               |
| Symbol  | Parameter  | Conditions   | Min   | Typ                    | Max      | Units         |
| $t_{pd\ A, B}$  | Propagation Delay from Trigger Input (A, B) to Output Q, $\bar{Q}$ | $V_{CC} = 5V$  |   | 250                    | 500      | ns            |
|   |  | $V_{CC} = 10V$   |   | 120                    | 250      |               |
| $t_{pd\ CL}$  | Propagation Delay from Clear Input (CL) to Output Q, $\bar{Q}$     | $V_{CC} = 5V$  |   | 250                    | 500      | ns            |
|   |  | $V_{CC} = 10V$   |   | 120                    | 250      |               |
| $t_S$   | Time Prior to Trigger Input (A, B) that Clear must be Set          | $V_{CC} = 5V$  | 150   | 50                     |          | ns            |
|   |  | $V_{CC} = 10V$   | 60  | 20                     |          |               |
| $t_{W(A, B)}$   | Trigger Input (A, B) Pulse Width                                   | $V_{CC} = 5V$  | 150   | 50                     |          | ns            |
|   |  | $V_{CC} = 10V$   | 70  | 30                     |          |               |
| $t_{W(CL)}$   | Clear Input (CL) Pulse Width                                       | $V_{CC} = 5V$  | 150   | 50                     |          | ns            |
|   |  | $V_{CC} = 10V$   | 70  | 30                     |          |               |
| $t_{W(OUT)}$  | Q or $\bar{Q}$ Output Pulse Width                                  | $V_{CC} = 5V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 0\text{ pF}$                       |   | 900                    |          | ns            |
|   |  | $V_{CC} = 10V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 0\text{ pF}$                      |   | 350                    |          | ns            |
|   |  | $V_{CC} = 15V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 0\text{ pF}$                      |   | 320                    |          | ns            |
|   |  | $V_{CC} = 5V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 1000\text{ pF}$ (Figure 1)         | 9.0   | 10.6                   | 12.2     | $\mu\text{s}$ |
|   |  | $V_{CC} = 10V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 1000\text{ pF}$ (Figure 1)        | 9.0   | 10                     | 11       | $\mu\text{s}$ |
|   |  | $V_{CC} = 15V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 1000\text{ pF}$ (Figure 1)        | 8.9   | 9.8                    | 10.8     | $\mu\text{s}$ |
|   |  | $V_{CC} = 5V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 0.1\ \mu\text{F}$ (Figure 3)       | 900   | 1020                   | 1200     | $\mu\text{s}$ |
|   |  | $V_{CC} = 10V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 0.1\ \mu\text{F}$ (Figure 3)      | 900   | 1000                   | 1100     | $\mu\text{s}$ |
|   |  | $V_{CC} = 15V$ , $R_{EXT} = 10k$ ,<br>$C_{EXT} = 0.1\ \mu\text{F}$ (Figure 3)      | 900   | 990                    | 1100     | $\mu\text{s}$ |
|   |  | $R_{ON}$   | ON Resistance of Transistor between R/ $C_{EXT}$ to $C_{EXT}$ | $V_{CC} = 5V$ (Note 4) |          | 50            |
| $V_{CC} = 10V$ (Note 4)   |  |  |   | 25                     | 65       |               |
| $V_{CC} = 15V$ (Note 4)   |  |  |   | 16.7                   | 45       |               |
|   | Output Duty Cycle  | $R = 10k$ , $C = 1000\text{ pF}$<br>$R = 10k$ , $C = 0.1\ \mu\text{F}$<br>(Note 5) |   |                        | 90<br>90 | %             |
| $C_{IN}$  | Input Capacitance  | R/ $C_{EXT}$ Input (Note 6)  |   | 15                     | 25       | pF            |
|   |  | Any Other Input (Note 6)   |   | 5                      |          |               |
| <p><b>Note 3:</b> AC Parameters are guaranteed by DC correlated testing.</p> <p><b>Note 4:</b> See AN-138 for detailed explanation <math>R_{ON}</math>.</p> <p><b>Note 5:</b> Maximum output duty cycle = <math>R_{EXT}/R_{EXT} + 1000</math>.</p> <p><b>Note 6:</b> Capacitance is guaranteed by periodic testing.</p> |  |  |   |                        |          |               |

Typical Performance Characteristics



0% Point pulse width:  
 At VCC = 5V, TW = 10.6 μs  
 At VCC = 10V, TW = 10 μs  
 At VCC = 15V, TW = 9.8 μs  
 Percentage of units within +4%:  
 At VCC = 5V, 90% of units  
 At VCC = 10V, 95% of units  
 At VCC = 15V, 98% of units

FIGURE 1. Typical Distribution of Units for Output Pulse Width



0% Point pulse width:  
 At VCC = 5V, TW = 1020 μs  
 At VCC = 10V, TW = 1000 μs  
 At VCC = 15V, TW = 982 μs  
 Percentage of units within +4%:  
 At VCC = 5V, 95% of units  
 At VCC = 10V, 97% of units  
 At VCC = 15V, 98% of units

FIGURE 3. Typical Distribution of Units for Output Pulse Width

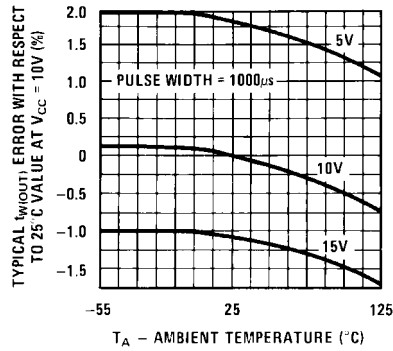


FIGURE 2. Typical Variation in Output Pulse Width vs Temperature

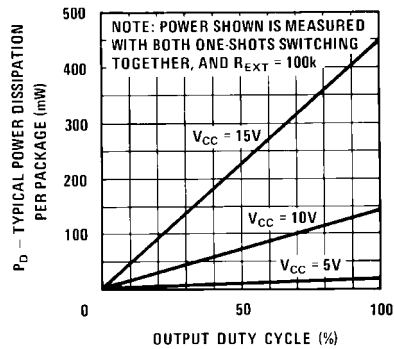
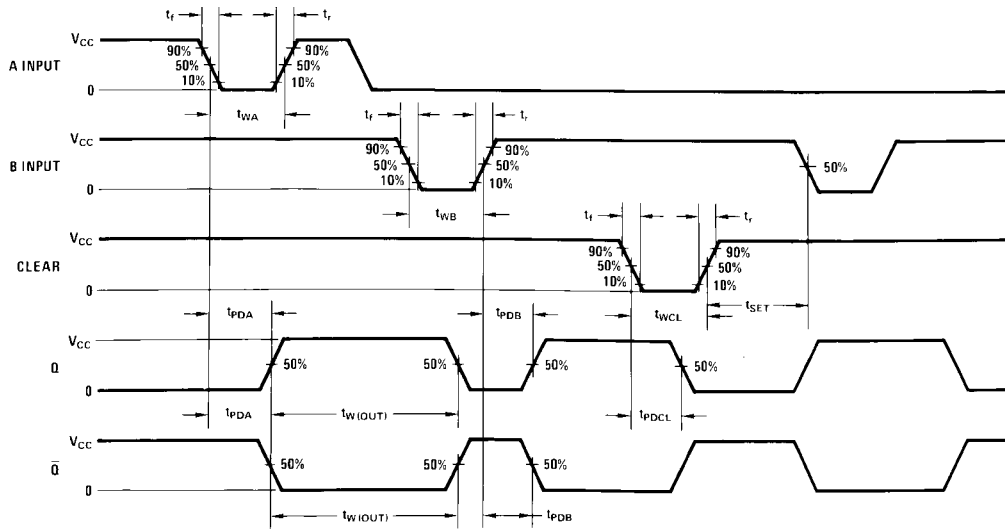


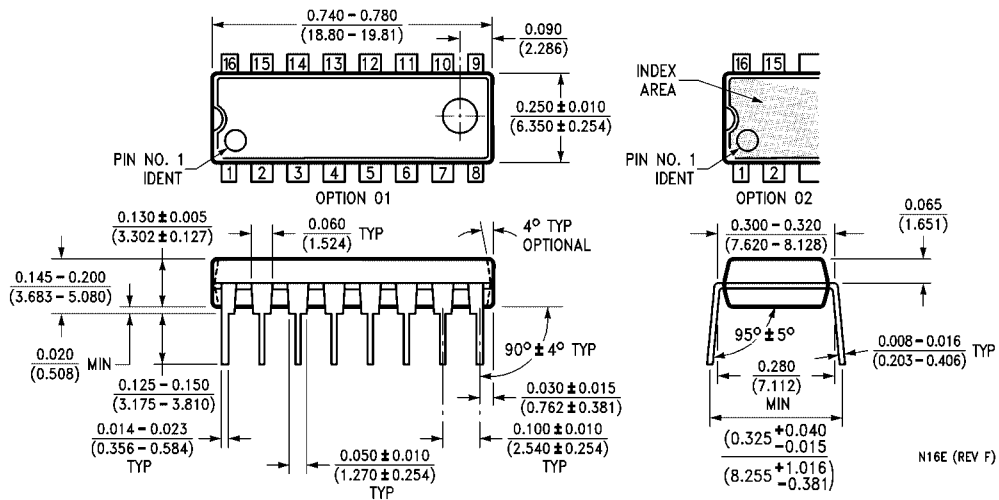
FIGURE 4. Typical Power Dissipation per Package

**Typical Performance Characteristics** (Continued)  
**Switching Time Waveforms**



$t_r = t_f = 20 \text{ ns}$

**Physical Dimensions** inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E

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