National Semiconductor

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MM58342 High Voltage Display Driver

General Description

The MM58342 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58342 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram

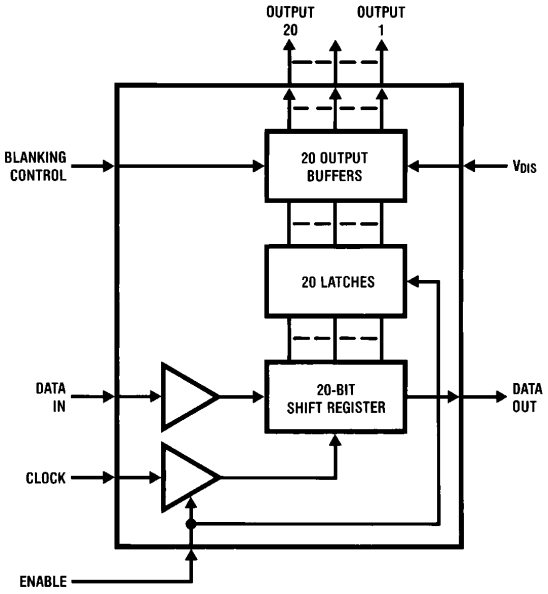

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FIGURE 1

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Input Pin	$V_{DD} + 0.3V$ to $V_{SS} - 0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD} - 36.5V$
$V_{DD} + \lvert V_{DIS} \rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	
Molded DIP Package, Board Mount	2.03W*
Molded DIP Package, Socket Mount	1.83W**
Junction Temperature	130°C
Lead Temperature (Soldering, 10 sec.)	260°C

*Molded DIP Package, Board Mount, $\theta_{JA} = 52°C/W$, derate 19.2 mW/°C above 25°C.

**Molded DIP Package, Socket Mount, $\theta_{JA} = 58°C/W$, derate 17.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS} = 0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN} = V_{SS}$ or V_{DD}, $V_{SS} = 0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD} = 5.5V$, $V_{SS} = 0V$, $V_{DIS} = -30V$ All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	$I_{OUT} = 400\ \mu A$			0.4	V
V_{OH}	Logic '1'	$I_{OUT} = -10\ \mu A$	$V_{DD} - 0.5$			V
V_{OH}	Logic '1'	$I_{OUT} = -500\ \mu A$	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN} = 0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	$V_{DD} = 5.5V$, $V_{SS} = 0V$				
R_{OFF}	Output Off *(Figure 3a)*	$V_{DIS} = -10V$	55		250	kΩ
		$V_{DIS} = -20V$	60		300	kΩ
		$V_{DIS} = -30V$	65		400	kΩ
R_{ON}	Output On *(Figure 3b)*	$V_{DIS} = -10V$		700	800	Ω
		$V_{DIS} = -20V$		600	750	Ω
		$V_{DIS} = -30V$		500	680	Ω
V_{DOL}	Display Output Low Voltage	$V_{DD} = 5.5V$, I_{OUT} = Open Circuit, $-30V \le V_{DIS} \le -10V$	V_{DIS}		$V_{DIS} + 2$	V

Note 1: 74LSTTL $V_{OH} = 2.7V$ @ $I_{OUT} = -400\ \mu A$, TTL $V_{OH} = 2.4V$ @ $I_{OUT} = -400\ \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Clock Input	(Notes 3 and 4)				
f_C	Frequency				800	kHz
t_H	High Time		300			ns
t_L	Low Time		300			ns
	Data Input					
t_{DS}	Set-Up Time		100			ns
t_{DH}	Hold Time		100			ns
	Enable Input	(Note 2)				
t_{ES}	Set-Up Time		100			ns
t_{EH}	Hold Time		100			ns
	Data Output	$C_L = 50$ pF				
t_{CDO}	CLOCK Low to Data Out Time				500	ns

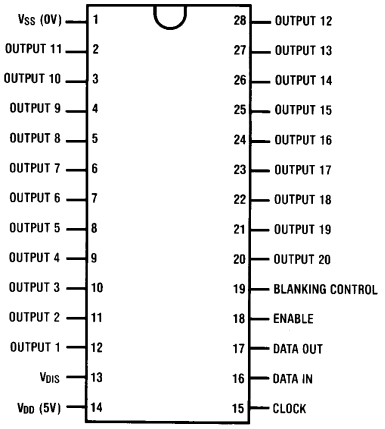
Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, f = 800 kHz, 50% ±10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Connection Diagrams

Dual-In-Line Package



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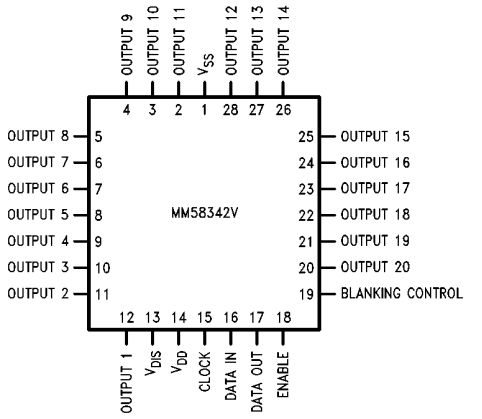
Top View

FIGURE 2

Order Number MM58342N
See NS Package Number N28B

Plastic Chip Carrier



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Top View
Order Number MM58342V
See NS Package Number V28A

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58342 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58342 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58342 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58342, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a*

Functional Description (Continued)

and *3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58342.

To clear (reset) the display driver at power on or any time, the following flushing routine may be used. With the enable signal high, clock in 20 zeroes. Drive the enable signal low and the display will be blank. It is recommended to clear the driver at power on.

In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58342 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58342 is used to provide the grid drive for a 40-digit 2 line 5 x 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.

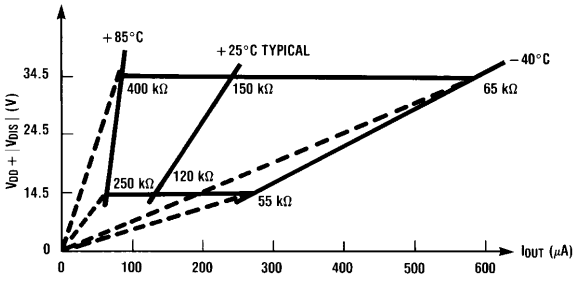

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FIGURE 3a. Output Impedance Off

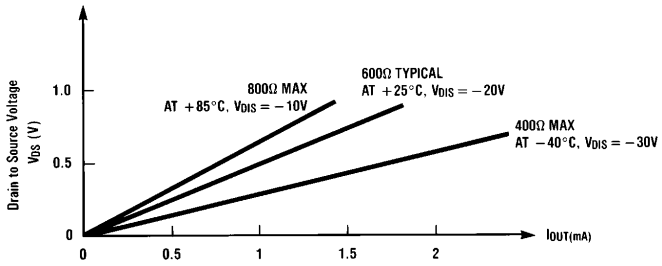

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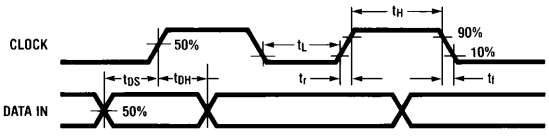
FIGURE 3b. Output Impedance On

Timing Diagrams



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For the purposes of AC measurement, V_{IH} = 2.4V, V_{IL} = 0.8V.

FIGURE 4. Clock and Data Timings

Timing Diagrams (Continued)

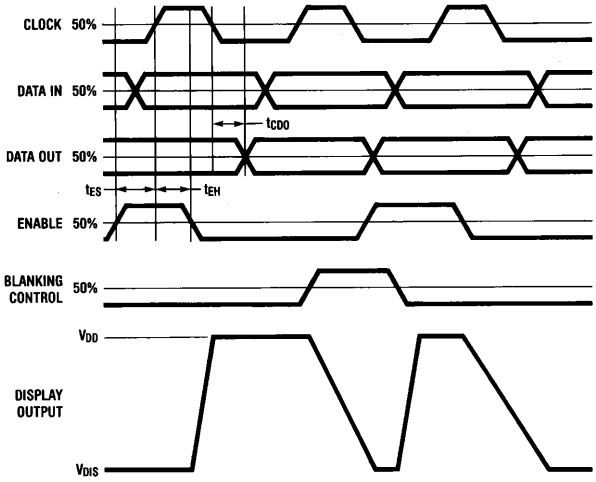

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FIGURE 5. Timings (Data Format)

Typical Application

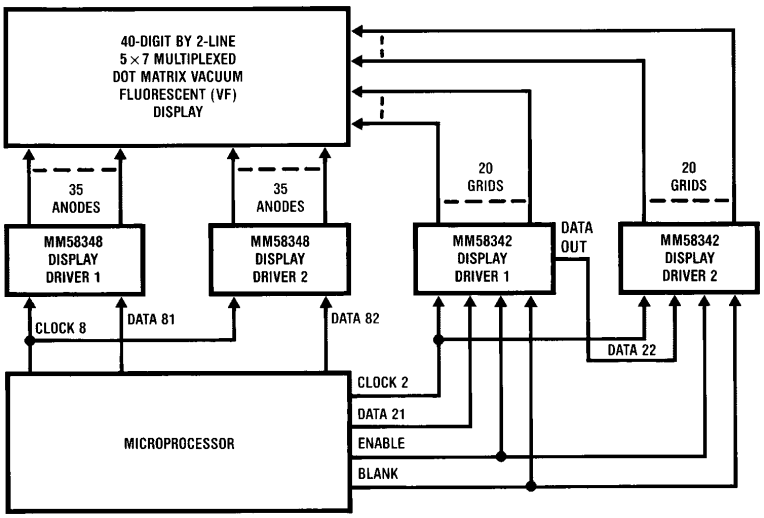

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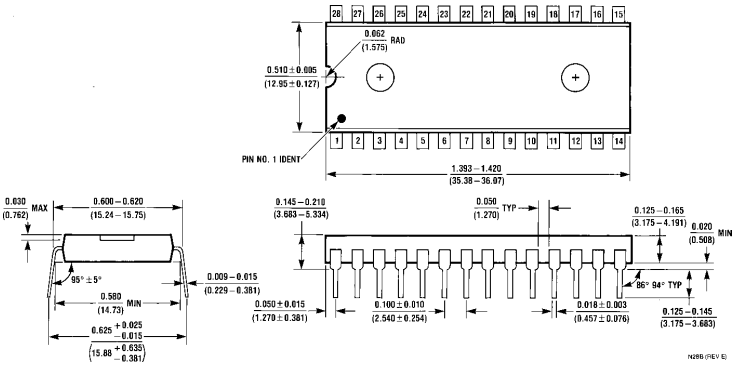
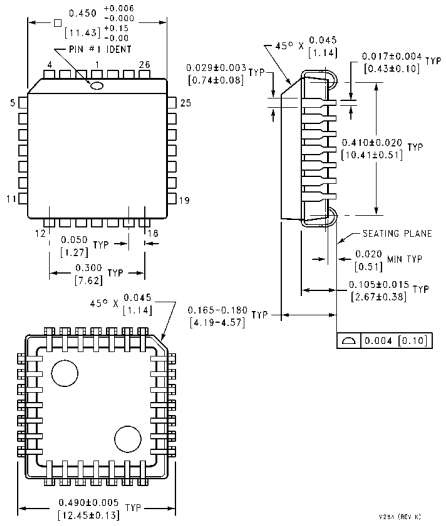
FIGURE 6. Microprocessor-Controlled Word Processor

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number MM58342N
NS Package Number N28B



Plastic Chip Carrier (V)
Order Number MM58342V
NS Package Number V28A

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