MM54C95,MM74C95

MM54C95 MM74C95 4-Bit Right-Shift Left-Shift Register



Literature Number: SNOS348A

MM54C95/MM74C95 4-Bit Right-Shift Left-Shift Register

General Description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip-flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right-shift or left-shift register.

When a logical "0" level is applied to the mode control input, the output of each flip-flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shiftleft operation can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop and serial data is entered at input D.

Features

10 MHz (typ.) ■ Medium speed operation

 $V_{CC} = 10V$, $C_L = 50 pF$ 0.45 V_{CC} (typ.)

■ High noise immunity ■ Low power 100 nW/(typ.)

■ Tenth power TTL compatible Drive 2 LTTL loads ■ Wide supply voltage range 3V to 15V

■ Synchronous parallel load

■ Parallel inputs and outputs from each flip-flop

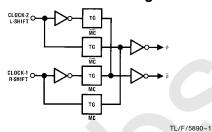
■ Negative edge triggered clocking

■ The MM54C95/MM74C95 follows the MM54L95/ MM74L95 Pinout

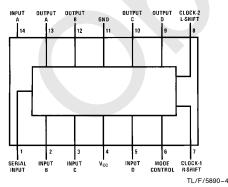
Applications

- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

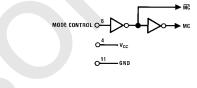
Block and Connection Diagrams

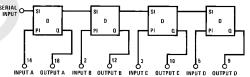


Dual-In-Line Package



Order Number MM54C95 or MM74C95





TL/F/5890-3

TL/F/5890-2

Mode Control = 0 for Right Shift Mode Control = 1 for Left Shift or Parallel Load

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin

-0.3V to $V_{CC} + 0.3V$

Operating Temperature Range (T_A) MM54C95

MM54C95 MM74C95 -55°C to $+125^{\circ}\text{C}$ -40°C to $+85^{\circ}\text{C}$ Storage Temperature (T_S)

 $\begin{array}{l} \text{Maximum V}_{CC} \text{ Voltage} \\ \text{Power Dissipation (P}_{D}) \end{array}$

(Soldering, 10 seconds)

Dual-In-Line Small Outline

Small Outline
Operating V_{CC} Range
Lead Temperature (T₁)

260°C

 -65°C to $+150^{\circ}\text{C}$

18V

700 mW

500 mW

+3V to +15V

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
MOS TO CN	ios					
V _{IN(1)}	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
V _{IN(0)}	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V V
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V			1.0	μΑ
I _{IN(0)}	Logical "0" Input Current	V _{CC} = 15V	-1.0			μΑ
I _{CC}	Supply Current	V _{CC} = 15V		0.050	300	μΑ
OW POWER	TTL/CMOS INTERFACE					
V _{IN(1)}	Logical "1" Input Voltage	54C, V _{CC} = 4.5V 74C, V _{CC} = 4.75V	V _{CC} - 1.5 V _{CC} - 1.5			V V
V _{IN(0)}	Logical "0" Input Voltage	54C, V _{CC} = 4.5V 74C, V _{CC} = 4.75V			0.8 0.8	V V
V _{OUT(1)}	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_{O} = 360 \mu A$ 74C, $V_{CC} = 4.75V$, $I_{O} = 360 \mu A$	2.4 2.4			V V
V _{OUT(0)}	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_{O} = 360 \mu A$ 74C, $V_{CC} = 4.75V$, $I_{O} = 360 \mu A$			0.4 0.4	V V
UTPUT DRI	VE (See 54C/74C Family Chara	cteristics Data Sheet)				
ISOURCE	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25^{\circ}C, V_{OUT} = 0V$	-1.75			mA
ISOURCE	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25^{\circ}C, V_{OUT} = 0V$	-8.0			mA
I _{SINK}	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25^{\circ}C, V_{OUT} = V_{CC}$	1.75			mA
I _{SINK}	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25^{\circ}C, V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25^{\circ}C, C_L = 50 \text{ pF}, \text{ unless otherwise noted}$

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	$V_{CC} = 5V$ $V_{CC} = 10V$		200 80	400 160	ns ns
t _{S0} , t _{S1}	Time Prior to Clock Pulse that Data must be Preset	$V_{CC} = 5V$ $V_{CC} = 10V$	60 25	30 10		ns ns
t _{H0} , t _{H1}	Time After Clock Pulse that Data must be Held	$V_{CC} = 5V$ $V_{CC} = 10V$	25 10	10 50		ns ns
t _{PW}	Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5V$ $V_{CC} = 10V$		100 50		ns ns
t _{SM}	Time Prior to Clock Pulse that Mode Control must be Preset	$V_{CC} = 5V$ $V_{CC} = 10V$	200 100	100 50		ns ns
f _{MAX}	Maximum Input Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	3 6.5	5 10		MHz MHz
C _{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C _{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

^{*}AC Parameters are guaranteed by DC correlated testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, Application Note AN-90.

Function Table

Inputs							Outputs				
Mode Control	Clocks		Serial	Parallel			QA	QB	Qc	Q_D	
	2 (L)	1 (R)	Jocital	Α	В	С	D	G _A	αВ	~ ∪	αD
Н	Н	Χ	X	X	Х	X	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}
Н	↓	Χ	X	a	b	С	С	а	b	С	d
Н	↓	X	X	Q _B †	Q _C †	Q_D^{\dagger}	d	Q _{Bn}	Q_Cn	Q_{Dn}	d
L	L	Н	X	X	X	X	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	\downarrow	Н	/X	X	X	Χ	Н	Q_{An}	Q_{Bn}	Q_Cn
L	X	\downarrow	L	X	X	X	Χ	L	Q_{An}	Q_{Bn}	Q_{Cn}
1	L	L	X	X	X	X	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}
\downarrow	L	L	X	X	X	X	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}
1	L	Н	X	X	X	X	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	Н	L	X	Х	X	X	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}
1	Н	Н	X	X	X	X	Χ	Q _{A0}	Q_{B0}	Q_{C0}	Q_{D0}
1	L	Н	X	X	X	X	Χ	Undefined			
\downarrow	Н	L	Х	Х	Χ	Χ	Χ	Operating Conditions			

†Shifting left requires external connection of QB to A, QC to B, and QD to C. Serial data is entered at input D.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

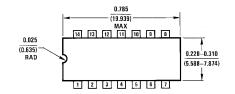
 $[\]downarrow$ = transition from high to low level, \uparrow = transition from low to high level.

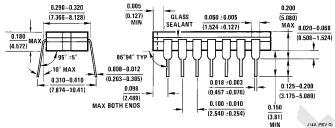
a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

 Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_{A} , Q_{B} , Q_{C} or Q_{D} respectively, before the indicated steady-state input conditions were established.

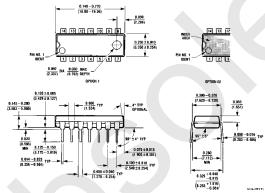
 $Q_{An},\,Q_{Bn},\,Q_{Cn},\,Q_{Dn}\,=\,\,\text{the level of}\,\,Q_A,\,Q_B,\,Q_C\,\,\text{or}\,\,Q_D\,\,\text{respectively, before the most recent transition of the clock}.$

Physical Dimensions inches (millimeters)





Ceramic Dual-In-Line Package (J) Order Number MM54C95J or MM74C95J NS Package Number J14A



Molded Dual-In-Line Package (N) Order Number MM54C95N or MM74C95N NS Package Number N14A

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