ML2302

Recording and Playback LSI with Built-in 2-Bit ADPCM2 Supported FIFO

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

This version: Apr. 2001

GENERAL DESCRIPTION

The ML2302 is a recording and playback LSI with built-in FIFO memories for buffering. It employs the new 2-bit ADPCM2 algorithm in addition to conventional 4-bit OKIADPCM and 4-bit OKIADPCM2 algorithms. The ML2302 operates at 2.7 to 3.6 V and supports a variety of applications.

FEATURES

- Built-in two 1024-bit FIFOs (one for recording, other for playback) (buffering time of 32 ms when using 8 kHz sampling frequency and 4-bit ADPCM)
- Supports five compression algorithms for recording and playback:
 2-bit ADPCM2; 4/5/6/7-bit OKIADPCM2; 4-bit OKIADPCM; 8/16-bit straight PCM; 8-bit OKI Nonlinear PCM
- Source oscillation frequency 16.384 MHz
- Sampling frequency (fsam)

4.0 to 16.0 kHz (OKIADPCM2) 4.0 to 25.6 kHz (8-bit straight PCM)

- Supports 8-bit bus interface.
- Built-in voice level detection function (VAC)
- Built-in noise injection function
- Supports external DAC interface.
- Built-in volume control circuit

(0 dB to -30 dB: -2 dB step, -30 dB to -80 dB: -4 dB step)

- Built-in 14-bit A/D converter and 14-bit D/A converter
- Built-in low pass filter (LPF)

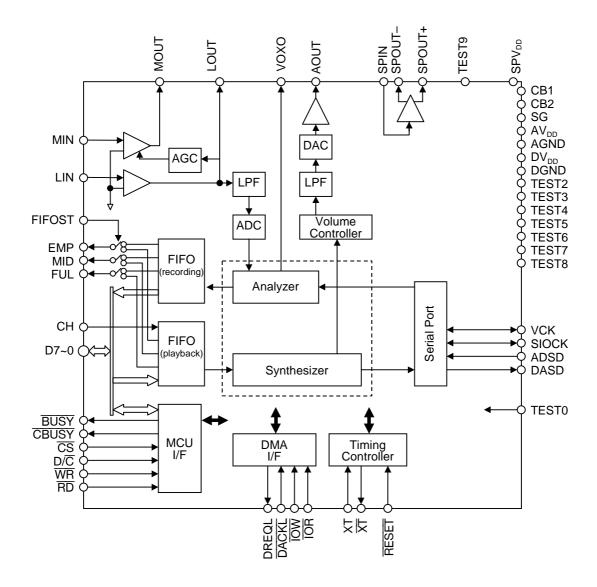
(recording side: analog filter, playback side: digital filter)

- Built-in speaker amplifier (100 mW, 8Ω)
- Power supply voltage : +2.7 to +3.6 V

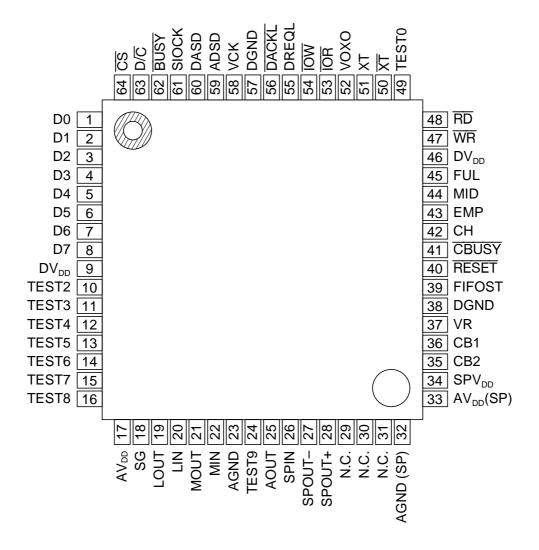
• Package : 64-pin plastic TQFP (TQFP64-P-1010-0.50-K) (Product name: ML2302TS)

: 71-pin W – CSP

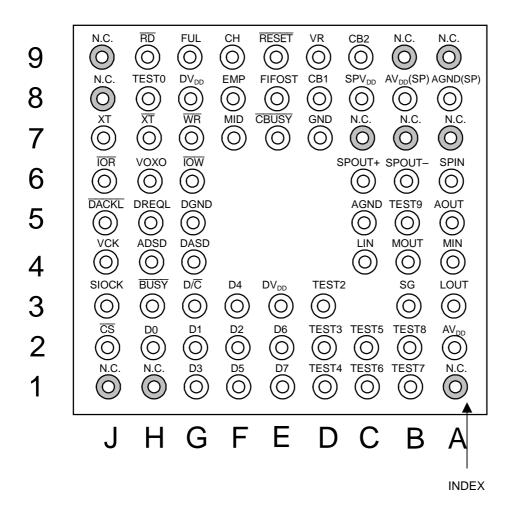
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



N.C.: No Connection 64-pin plastic TQFP



71-pin W-CSP (Bottom View)

PIN DESCRIPTIONS

Symbol	Type	Description			
D7 to 0		Bidirectional data bus.			
	I/O	Command and data inputs from an external microcontroller and memory, and status and data outputs to an external microcontroller and memory.			
WR	1	Write pulse input pin. This pin pulses "L" when command or voice data is input to D7 to D0 pins.			
RD	1	Read pulse input pin. This pin pulses "L" when status or voice data is output to D7 to D0.			
<u>CS</u>	1	Accepts write pulse and read pulse when this pin is "L".			
D/C	I	Voice data is input or output to and from D7 to D0 when this pin is "H".			
BUSY	0	This pin outputs a "L" level during RECORDING, PLAYBACK, or PAUSE.			
CBUSY	0	Accepts a command during this pin is "H".			
		"H" indicates that there is no data in FIFO memory.			
EMP	0	During playback, voice synthesis starts when EMP changes to "L". Active "H" can be changed to active "L".			
MID	0	"H" level indicates that there is more than half of the FIFO memory.			
FUL	0	"H" level indicates that FIFO memory is full of data. During playback, this pin is "H" and data cannot be written in FIFO memory. During recording, data is not written after FIFO memory is full of data.			
		Active "H" can be changed to active "L".			
СН	1	This pin should be set at a "L" level normally and be set at a "H" level when DMA is used.			
DREQL	0	When DMA transfer is selected, "H" level DREQL outputs a signal to request a DMA transfer. Active "H" can be changed to active "L".			
DACKL		Input to DACKL a signal when DMA transfer is permitted by the DMA controller. when DACKL is "L", $\overline{10W}$ and $\overline{10R}$ signals are accepted.			
DACKL	1	Active "L" can be changed to active "H" by command input.			
		If DMA transfer is not used, set this pin to "H" level.			
ĪŌW	I	Write pulse Input pin to write external memory data to ML2302 during DMA transfer. If DMA transfer is not used, set this pin to "H" level.			
ĪŌĒ	ı	Read pulse input pin to read data of ML2302 during DMA transfer.			
ĪOR	ı	If DMA transfer is not used, set this pin to "H" level.			
ADSD	I	16-bit serial data input pin when external A/D converter is used.			
DASD	0	16-bit serial data input pin when external D/A converter is used.			
SIOCK	I/O	16-bit serial data transfer clock when external A/D or D/A converter is used.			

Symbol	Туре	Description			
VCK	I/O	Outputs sampling frequency selected. Input pin when slave mode is selected.			
XT XT	I 0	Oscillator connection pins. when external clock is used, input clock into XT pin and leave $\overline{\text{XT}}$ pin open. Oscillation stops during reset or power down mode. Figure (a) shows Oscillation Equivalent Circuit.			
RESET	I	When this pin is "L", the LSI is initialized and AOUT is set to the GND level.			
FIFOST	I	When this pin is "L", EMP, MID, and FULL of playback FIFO can be monitored. Whis pin is "H", EMP, MID, and FULL of record FIFO can be monitored.			
SG	0	Analog circuit signal ground pin. This pin is connected to GND during reset or power down mode.			
MIN LIN	I	Inverting input pin for built-in OP amplifier. Non-inverting input pin is connected to SG (Signal Ground).			
MOUT LOUT	0	MOUT is the output of internal OP amplifier to MIN, and LOUT is to LIN.			
AOUT	0	This is the output of the analog playback waveform.			
VOXO	0	Voice level detection signal			
TEST0, 8	I	Pins for testing. Set the pins to "L".			
DV_{DD}		Digital power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and DGND pin			
DGND		Digital GND pin.			
AV_{DD}		Analog power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and AGND pin.			
AGND		Analog GND pin.			
CB1	0	This pin is used to connect a capacitor for voltage multiplier power supply. Insert a 1			
CB2	0	μF capacitor between CB1 and CB2.			
SPV_{DD}	0	Voltage multiplier power supply output pin for speaker amplifier. Connect a 1 µF capacitor to this pin in order to stabilize the speaker amplifier circuit.			
VR	0	Bias output pin for speaker amplifier. Set this pin to the GND level during reset or power down mode.			
SPIN	I	Voice signal input pin for speaker amplifier.			
SPOUT-	0	Speaker amplifier output pin. This pin outputs a signal in reverse phase to the signal that is input to the SPIN pin.			
SPOUT+	0	Speaker amplifier output pin. This pin outputs a signal in phase to the signal that is input to the SPIN pin.			
TEST2 to 7, 9	0	Pins for testing. Leave these pins open.			

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}		-0.3 to +7.0	V
Input Voltage	V _{IN}	Ta = 25°C	-0.3 to V_{DD} +0.3	V
Maximum Power Dissipation	PD		689.6	mW
Temperature Storage	T _{STG}	_	-55 to +155	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	DGND = AGND = 0 V	+2.7 to +3.6	V
Operating Temperature	T _{Op}	_	-10 to +70	°C
Master Clock Frequency	f _{osc}	_	16.384	MHz
Speaker Amplifier Load Impedance	R _{LSP}	_	8 to ∞	Ω

ELECTRICAL CHARACTERISTICS

DC Characteristics

 $(DV_{DD} = AV_{DD} = 2.7 \text{ to } 3.6 \text{ V}, DGND = AGND = 0 \text{ V}, Ta = -10 \text{ to } +70^{\circ}\text{C})$

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
High-level Input Voltage	V _{IH}	_	$0.85 \times V_{DD}$	_	_	V
Low-level Input Voltage	V _{IL}	_	_	ı	$0.15 \times V_{DD}$	V
High-level Output Voltage (*1, *5)	V _{OH1}	1 - 40 114	V _{DD} - 0.3	l	_	V
High-level Output Voltage (*2, *5)	V _{OH2}	$I_{OH} = -40 \mu\text{A}$	V _{DD} - 0.3	l	_	V
Low-level Output Voltage (*1, *5)	V _{OL1}	1 - 2 mA	_		0.45	V
Low-level Output Voltage (*2, *5)	V _{OL2}	I _{OL} = 2 mA	_	1	0.8	V
High-level Input Current (*3)	I _{IH1}	V V	_	l	10	μA
High-level Input Current (*4)	I _{IH2}	$V_{IH} = V_{DD}$	_	-	20	μΑ
Low-level Input Current (*3)	I _{IL1}	V CND	-10	-	_	μΑ
Low-level Input Current (*4)	I _{IL2}	V _{IL} = GND	-20	1	_	μΑ
Operating Current Consumption	I _{DD}	f _{osc} = 16 MHz, without load	_	15	20	mA
Standby Current	lana	At reset, without load	_		10	μΑ
Consumption	I _{DDS}	At power down	_	_	10	μΑ

^{*1 :} Applicable to input pins excluding XT pin. *2 : Applicable to XT pin.

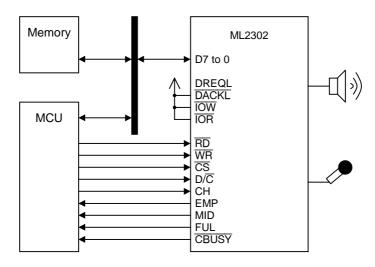
^{*3 :} Applicable to output pins excluding \overline{XT} pin.

^{*4 :} Applicable to \overline{XT} pin.

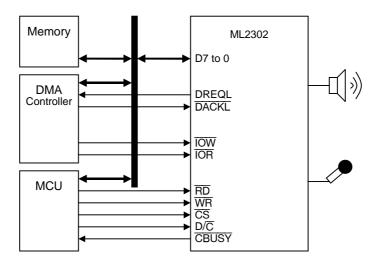
^{*5 :} If an output pin is shortcircuited to $V_{\rm DD}$ or GND, the LSI may be damaged.

APPLICATION CIRCUIT EXAMPLE

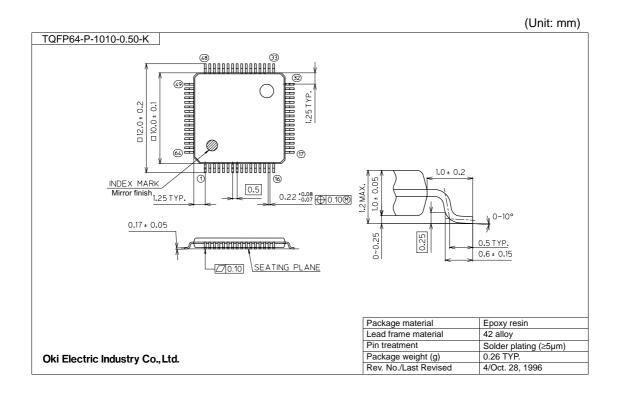
(1) MCU and External Interface



(2) Interface when DMA controller is Used



PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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