SGS-THOMSON MICROELECTRONICS

MK48T87A(B)

ADDRESS / DATA MULTIPLEX TIMEKEEPER™ RAM

ADVANCE DATA

- DROP-IN REPLACEMENT FOR IBM AT COMPUTER CLOCK/CALENDAR
- PIN COMPATIBLE WITH THE MC146818 A
- TOTALLY NONVOLATILE WITH OVER 10 YEARS OF OPERATION IN THE ABSENCE OF POWER
- SELF-CONTAINED SUBSYSTEM INCLUDES LITHIUM BATTERY, QUARTZ CRYSTAL AND SUPPORT CIRCUITRY
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BETWEEN MOTOROLA AND INTEL BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS

  14 Bytes Of Clock And Control Registers

  50 Bytes Of General Purpose Ram
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE

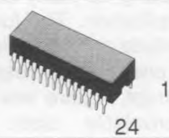
  Time-of-day Alarm Once/second To Once/day

  Periodic Rates From 122 us To 500 ms

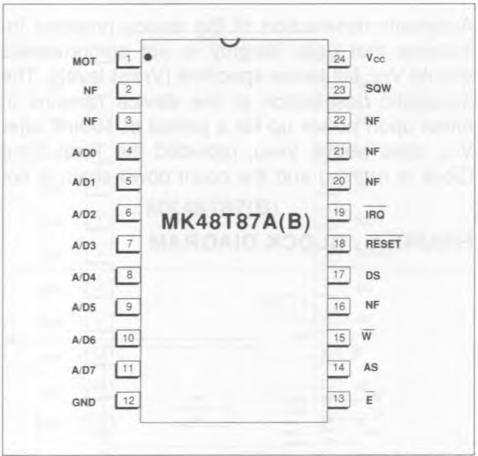
  End Of Clock Update Cycle

* This pin serves no function and may be connected to other signals without affecting device operation. The electrical characteristics are the same as the other inputs pins.

B
DIP-24
(Plastic with battery top Hat)



PIN CONNECTIONS



PIN NAMES

A/D0 - A/D7	ADDRESS / DATA
MOT	BUS TYPE SELECTION
E	CHIP SELECT
AS	ADDRESS STROBE
W	READ / WRITE
SQW	SQUARE WAVE OUT
IRQ	INTERRUPT REQUEST
RESET	RESET
DS	DATA STROBE
V_{CC}	+5 VOLTS
GND	GROUND
RCLR	RAM CLEAR
NF*	NO FUNCTION

DESCRIPTION

The MK48T87 Real Time Clock and RAM is designed to be a compatable replacement for the MC146818. A lithium energy source, a quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. The MK48T87 is, therefore, a complete subsystem replacing as many as 16 components in a typical application. The functions available to the user include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The Real Time Clock/RAM is unique in that the time-of-day and memory are maintained even in the absence of power.

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset, allowing sufficient time for V_{CC} to stabilize and giving the system clock a wake up period so that a valid system reset can be established.

The block diagram in Figure 1 shows the pin connection with the major internal functions of MK48T87 (Real Time Clock/RAM). **FOR COMPLETE DESCRIPTION OF OPERATING CONDITIONS, ELECTRICAL CHARACTERISTICS, BUS TIMING, PACKAGE DIMENSION, AND PIN DESCRIPTIONS OTHER THAN RLCR, SEE THE MK48T87(B) DATASHEET.**

SIGNAL DESCRIPTIONS

RCLR - The RCLR pin is used to clear (set to logic "1") all 50 bytes of general purpose RAM but does not affect the RAM associated with the Real Time Clock. In order to clear the RAM, RCLR must be forced to an input Logic "0" (-0.3 to 0.8 volts) for a minimun of 100 ms when V_{CC} is applied.

FIGURE 1 . BLOCK DIAGRAM