National Semiconductor

PRELIMINARY
July 1995

MCM28F256ACH
256-Mbit (32-Mbit x 8, 16-Mbit x 16) Flash Memory Module with Internal Decoding and Boundary Scan I/O Buffers

General Description

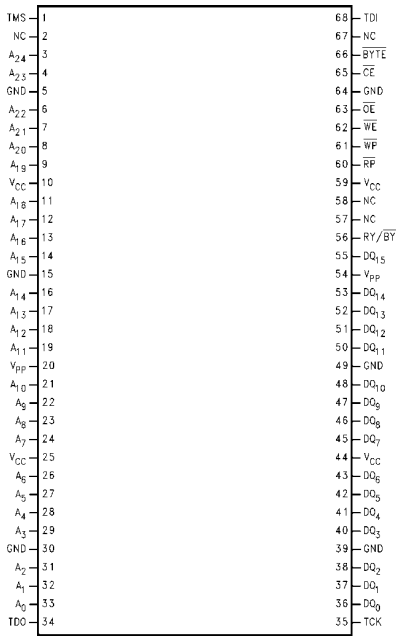
The MCM28F256ACH is a 268,435,456-bit flash memory module, organized as 16 pages with 16,777,216 bytes (8,388,608 words) per page. Utilizing Intel's FlashFile™ Memory and National's SCAN™ I/O buffers, the MCM28F256ACH offers several revolutionary features, including a user-configurable x8/x16 architecture, selective block locking, on-board write buffers, pipelined command execution and boundary scan test capability. Several power reduction features are also incorporated, including Automatic Power Savings (APS), which puts the module into a low current state when it is being accessed by a slowed or stopped CPU.

The MCM28F256ACH includes sixteen 28F016SA flash memories, decoding logic and IEEE 1149.1 compliant I/O buffers. The module is offered in a 68-lead, hermetic package. Both through-hole and surface mount lead configurations are available.

Features

- Read access time of 140 ns over the industrial temperature range (160 ns over the military temperature range)
- Utilizes Intel's FlashFile architecture with 512 independently lockable blocks (16 pages with 32 blocks per page)
- Choice of x8 or x16 architecture (user-configurable)
- Pipelined command execution
- Automated write and erase capability can be executed simultaneously in all 16 pages, greatly improving average write/erase cycle times
- National's IEEE 1149.1 compliant SCAN I/O buffers simplify the integration of design and test
- TTL compatible inputs
- Low noise, TRI-STATE® outputs drive 50Ω transmission line to TTL levels (75Ω transmission line over military temperature range)
- Hermetically sealed, integral substrate package
- DIP and surface mount packaging available

Connection Diagram



TL/Z/12436–1

Pin Names	Description
A_0	Byte-Select Address Input
A_1–A_{24}	Word-Select Address Inputs
DQ_0–DQ_7	Low-Byte Data I/O Bus
DQ_8–DQ_{15}	High-Byte Data I/O Bus
$\overline{CE}$	Chip Enable Input (Active LOW)
$\overline{RP}$	Reset/Power-Down Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
RY/$\overline{BY}$	Ready/Busy Output
$\overline{WP}$	Write Protect Input (Active LOW)
$\overline{BYTE}$	Byte Enable Input (Active LOW)
V_{PP}	Erase/Write Power Supply
V_{CC}	Device Power Supply
GND	Ground
NC	No Connection

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FlashFile™ is a trademark of Intel Corporation

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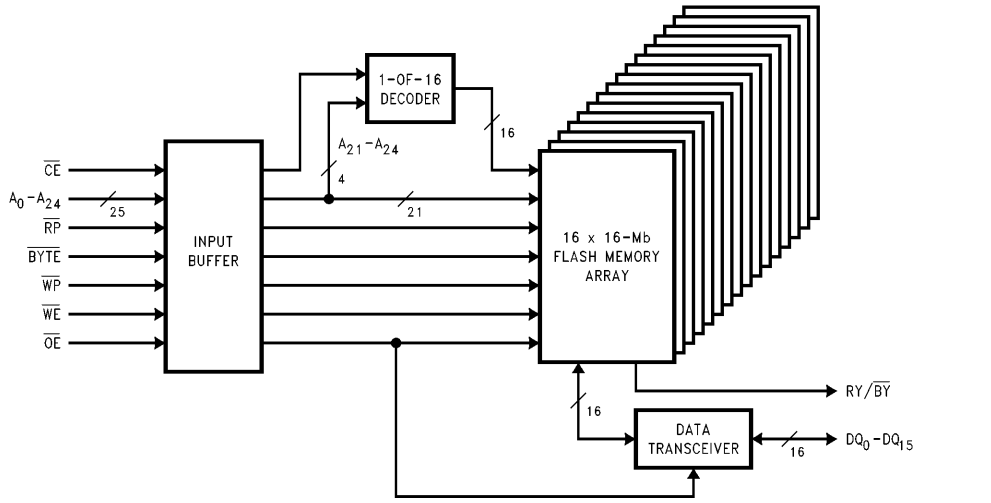
MCM28F256ACH 256-Mbit (32-Mbit x 8, 16-Mbit x 16) Flash Memory Module with Internal Decoding and Boundary Scan I/O Buffers

Block Diagram



TL/Z/12436–2

Functional Description

The MCM28F256ACH is a 268,435,456-bit (256-Mbit) flash memory module, organized as 16 pages with 16,777,216 bytes (8,388,608 words) per page. The module is segmented into 512 independently lockable blocks (32 blocks per page).

A Command User Interface (CUI) serves as the interface between the system controller and each page of internal memory. Automation of the byte/word write and block erase functions allow these commands to be executed using a two-write command sequence to the CUI. An internal Write State Machine (WSM) automatically executes the algorithms, timings and verifications necessary for the write and erase operations, thereby relieving the system controller of these tasks.

Each page of memory has three types of status registers and a RY/$\overline{BY}$ output to provide information on the progress of the requested operation. The Compatible Status Register (CSR) is 100% compatible with status register used in previous FlashFile memory devices. The Global Status Register (GSR) informs the system of command queue status, sector buffer status and WSM status. Block Status Registers (BSR) provide block-specific status information such as the block lock bit status. A choice of four different RY/$\overline{BY}$ configurations can be selected via special CUI commands: level-mode (default), pulse-on-write, pulse-on-erase, or disabled.

Functional Description (Continued)

Memory data is written in byte/word increments typically within 6 μs. Each page of memory incorporates two sector buffers of 256 bytes (128-words) which allow sector data writes at SRAM speeds. Writes from sector buffers to the flash array can be initiated with a single command and will complete independently, freeing the system controller for other tasks.

Any one of the 512 blocks can be erased typically within 0.6 seconds, without affecting the contents of the remaining blocks. Write and erase operations can be executed simultaneously in all 16 pages, greatly improving average write/erase cycle times.

A write protection scheme has been incorporated that provides maximum flexibility for selecting which blocks can be modified by the end user. A non-volatile lock bit is assigned to each block, and is used in conjunction with the master write protect input ($\overline{WP}$). With $\overline{WP}$ at logic low, block locking capability is invoked and the WSM is notified if a requested write or erase operation is not allowed. With $\overline{WP}$ at logic high, the status of all lock bits is overridden, allowing write or erase operations in any block.

The MCM28F256ACH reduces system overhead by allowing a subset of commands to be pipelined to the CUI on each page of memory. Ordinarily the command queue is 3-commands deep. However, if only single block erase commands are queued, the queue becomes virtually 32-commands deep.

Commands in the queue are prioritized. In order to capture data as it arrives in real time, write commands are executed before erase commands regardless of the command order. Also, multiple erase commands are queued in conjunction with write commands. If the CUI receives a write command affecting a block which is in queue to be erased, it will prioritize that block erase command ahead of other erase operations, allowing the complete block modification to occur as quickly as possible.

The $\overline{BYTE}$ input allows either x8 or x16 read/writes to the MCM28F256ACH. With $\overline{BYTE}$ at logic low the device operates in the 8-bit mode. Address A_0 selects either the low or high byte, and the high-byte data bus (DQ_8–DQ_{15}) floats to TRI-STATE. With $\overline{BYTE}$ at logic high the device is in the 16-bit mode of operation. In this case A_1 becomes the lowest order address, A_0 is not used (don't care) and data is input and output on all 16 bits of the data bus (DQ_0–DQ_{15}).

The MCM28F256ACH offers several low power modes of operation. Standby mode is entered when the module is deselected ($\overline{CE}$ at logic high). The typical I_{CC} current draw in this mode is 20 mA. If a WSM is processing a command when the module is deselected, the operation continues and power consumption remains at the non-standby level until the command has completed.

With $\overline{RP}$ at logic low, enters deep power-down mode. The typical I_{CC} current draw in this mode is 4 mA. Bringing $\overline{RP}$ low interrupts any current or pending commands and resets all status registers, CUI and WSM. The contents of any memory location being written or block being erased will no longer be valid.

The Sleep command puts a page of memory in sleep mode, which reduces the power consumption for that page of memory to deep power-down levels. The sleep command allows any current or pending commands to execute before going into sleep mode.

Automatic Power Savings (APS) is a feature which puts the module into a low current state when it is being accessed by a slowed or stopped CPU. After data is read from the memory array, power reduction control circuitry reduces the typical I_{CC} current draw to 20 mA until a new memory location is accessed.

To get the lowest possible power consumption in all modes, input pins should be held at V_{CC} or GND (CMOS levels), rather than V_{IH} or V_{IL} (TTL levels).

For detailed information regarding the operation of the 28F016SA FlashFile Memory, refer to the Intel data sheet (order number 290489) and user's manual (order number 297372).

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Device Power Supply Voltage (V_{CC}) −0.2V to +7.0V

Erase/Write Power Supply Voltage (V_{PP}) −0.2V to +14.0V

DC Input Diode Current (I_{IK})
- V_{IN} = −0.5V: −20 mA
- V_{IN} = V_{CC} + 0.5V: +20 mA

DC Output Diode Current (I_{OK})
- V_{OUT} = −0.5V: −20 mA
- V_{OUT} = V_{CC} +0.5V: +20 mA

DC Output Voltage (V_{OUT}) −0.5V to V_{CC} + 0.5V

DC Output Source/Sink Current (I_{OUT}) ±70 mA

DC V_{CC} or Ground Current
Per Output Pin (I_{CC} or I_{GND}) ±70 mA

Thermal Resistance, Junction to Case (θ_{JC}) 5°C/W

Junction Temperature (T_J) +150°C

Storage Temperature (T_{STG}) −65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of this module outside the datasheet specifications.

Recommended Operating Conditions

Device Power Supply Voltage (V_{CC}) 4.5V to 5.5V

Erase/Write Power Supply Voltage (V_{PP}) (Note 2)
- Read-Only Operations (V_{PPL}): 0.0V to 6.5V
- Erase/Write Operations (V_{PPH}): 11.4V to 12.6V

Input Voltage (V_{IN}) 0V to V_{CC}

Output Voltage (V_{OUT}) 0V to V_{CC}

Case Operating Temperature (T_C)
- Industrial: −45°C to +85°C
- Military: −55°C to +125°C

Minimum Input Edge Rate (dV/dt) 125 mV/ns
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V

Maximum Static Output Current
- High Level (I_{OH}): −32 mA
- Low Level (I_{OL}): +64 mA

Note 2: Erase and write operations are inhibited when V_{PP} = V_{PPL} and not guaranteed In the range betveeen V_{PPL} and V_{PPH}.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Military T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V	Industrial T_C = −45°C to +85°C, V_{CC} = 4.5V to 5.5V	Units
V_{IH}	Minimum High Input Voltage		2.0	2.0	V
V_{IL}	Maximum Low Input Voltage		0.8	0.8	V
I_{IH}	Maximum High Input Current	V_{IN} = V_{CC} All inputs except TCK, TDI, TMS	1.0	1.0	μA
		V_{IN} = V_{CC} TCK, TDI, TMS Inputs	15.0	15.0	μA
I_{IL}	Maximum Low Input Current	V_{IN} = GND All inputs except TCK, TDI, TMS	−1.0	−1.0	μA
		V_{IN} = GND TCK, TDI, TMS Inputs	−1.2	−1.2	mA
I_{OZT}	Maximum I/O Leakage Current	$V_{I/O}$ = V_{CC} or GND	±15.0	±10.0	μA
V_{OH}	Minimum High Output Voltage	I_{OUT}= −50 μA	V_{CC} − 1.35	V_{CC} − 1.35	V
		I_{OUT} = −32 mA		2.4	
		I_{OUT} = −24 mA	2.4		
V_{OL}	Maximum Low Output Voltage	I_{OUT} = 50 μA	0.1	0.1	V
		I_{OUT} = 64 mA		0.55	
		I_{OUT} = 48 mA	0.55		
I_{OLD}	Minimum Dynamic Output Current†	V_{OLD} = 0.8 V_{Max}	63	94	mA
I_{OHD}		V_{OHD} = 2.0 V_{Min}	−27	−40	
I_{OS}	Minimum Output Short Circuit Current†	V_{OUT} = 0V	−100	−100	mA
I_{CCT}	Maximum V_{CC} Current per Input at TTL HIGH	V_{IN} = V_{CC} − 2.1V All inputs except TCK,TDI, TMS	2.0	2.0	mA
I_{CCS}	Maximum V_{CC} Standby Current	$\overline{CE}$ = $\overline{RP}$ = V_{CC}	25	25	mA

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Military $T_C = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$	Industrial $T_C = -45°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$	Units
I_{CCD}	Maximum V_{CC} Deep Power Down Current	$\overline{RP}$ = GND, TDI = TMS = V_{CC}	5	5	mA
I_{CCR}	Maximum V_{CC} Read Current	f = 5 MHz I_{OUT} = 0 mA	120	120	mA
I_{CCW}	Maximum V_{CC} Write Current	Single Write Operation	70	70	mA
		16 Simultaneous Write Operations	650	650	mA
I_{CCE}	Maximum V_{CC} Block Erase Current	Single Erase Operation	60	60	mA
		16 Simultaneous Erase Operations	480	480	
I_{CCES}	Maximum V_{CC} Erase Suspend Current	Single Erase Operation Suspended	45	45	mA
		16 Erase Operations Simultaneously Suspended	220	220	
I_{PPS}	Maximum V_{PP} Standby Current	$V_{PP} \geq V_{CC}$	1	1	mA
I_{PPD}	Maximum V_{PP} Deep Power Down Current	$\overline{RP}$ = GND	1	1	mA
I_{PPR}	Maximum V_{PP} Read Current	$V_{PP} = V_{PPH}$	5	5	mA
I_{PPW}	Maximum V_{PP} Byte Write Current	Single Write Operation	18	18	mA
		16 Simultaneous Write Operations	290	290	
I_{PPE}	Maximum V_{PP} Block Erase Current	Single Erase Operation	15	15	mA
		16 Simultaneous Erase Operations	240	240	
I_{PPES}	Maximum V_{PP} Erase Suspend Current	1–16 Erase Operations Suspended	5	5	mA

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics Read Operations

Symbol	Parameter	Military $T_C = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		Industrial $T_C = -45°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$		Units
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time (No Page Change)	160		140		ns
	Read Cycle Time (With Page Change)	180		160		
t_{AVEL}	Address Setup to $\overline{CE}$ Going Low	20		15		ns
t_{AVGL}	Address Setup to $\overline{OE}$ Going Low	0		0		ns
t_{AVQV}	Address A_0–A_{20} to Output Delay		160		140	ns
	Address A_{21}–A_{24} to Output Delay		180		160	
t_{ELQV}	$\overline{CE}$ to Output Delay		200		180	ns
t_{PHQV}	$\overline{RP}$ to Output Delay		800		700	ns
t_{GLQV}	$\overline{OE}$ to Output Delay		80		70	ns
t_{ELQX}	$\overline{CE}$ to Output Low Z	0		0		ns
t_{EHQZ}	$\overline{CE}$ to Output High Z		50		40	ns
t_{GLQX}	$\overline{OE}$ to Output Low Z	0		0		ns
t_{GHQZ}	$\overline{OE}$ to Output High Z		70		60	ns

AC Electrical Characteristics Read Operations (Continued)

Symbol	Parameter	Military $T_C = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		Industrial $T_C = -45°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$		Units
		Min	Max	Min	Max	
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{RE}$ Change, Whichever Occurs First	0		0		ns
t_{FLQV} t_{FHQV}	$\overline{BYTE}$ to Output Delay		160		140	ns
t_{FLQZ}	$\overline{BYTE}$ Low to Output High Z		35		30	ns
t_{ELFL} t_{ELFH}	$\overline{CE}$ Low to $\overline{BYTE}$ Low or High		0		0	ns

AC Electrical Characteristics $\overline{WE}$ Controlled Command Write Operations

Symbol	Parameter	Military $T_C = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		Industrial $T_C = -45°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$		Units
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	160		140		ns
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going High	300		250		ns
t_{PHEL}	$\overline{RP}$ Setup to $\overline{CE}$ Going Low	700		600		ns
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low	40		35		ns
t_{AVWL}	Address A_{20}–A_{24} Setup to $\overline{WE}$ Going Low†	20		15		ns
t_{AVWH}	Address A_0–A_{20} Setup to $\overline{WE}$ Going High	70		60		ns
t_{DVWH}	Data Setup to $\overline{WE}$ Going High	70		60		ns
t_{WLWH}	$\overline{WE}$ Pulse Width Low	70		60		ns
t_{WHDX}	Data Hold from $\overline{WE}$ High	10		5		ns
t_{WHAX}	Address Hold from $\overline{WE}$ High	20		15		ns
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High	20		15		ns
t_{WHWL}	$\overline{WE}$ Pulse Width High	70		60		ns
t_{GHWL}	Read Recovery before Write	0		0		ns
t_{WHRL}	$\overline{WE}$ High to $\overline{RY/BY}$ Going Low		150		130	ns
t_{RHPL}	$\overline{RP}$ Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/$\overline{BY}$ High	0		0		ns
t_{PHWL}	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low	1.5		1.25		μs
t_{WHGL}	Write Recovery before Read	110		100		ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/$\overline{BY}$ High	0		0		μs
t_{WHQV1}	Duration of Word/Byte Write Operation (Measured to Valid Status Register Data)	3.0		3.6		μs
t_{WHQV2}	Duration of Block Erase Operation (Measured to Valid Status Register Data)	0.2		0.24		μs

†Address lines A_{20}–A_{24} must be valid during the entire $\overline{WE}$ Low pulse.

AC Electrical Characteristics $\overline{CE}$ Controlled Command Write Operations

Symbol	Parameter	Military $T_C = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		Industrial $T_C = -45°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$		Units
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	160		140		ns
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going High	300		250		ns
t_{PHWL}	$\overline{RP}$ Setup to $\overline{WE}$ Going Low	700		600		ns
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low	0		0		ns
t_{AVEL}	Address $A_{20}-A_{24}$ Setup to $\overline{CE}$ Going Low†	0		0		ns
t_{AVEH}	Address A_0-A_{20} Setup to $\overline{CE}$ Going High	55		45		ns
t_{DVEH}	Data Setup to $\overline{CE}$ Going High	55		45		ns
t_{ELEH}	$\overline{CE}$ Pulse Width Low	70		60		ns
t_{EHDX}	Data Hold from $\overline{CE}$ High	40		35		ns
t_{EHAX}	Address Hold from $\overline{CE}$ High	55		45		ns
t_{ENWH}	$\overline{WE}$ Hold from $\overline{CE}$ High	55		45		ns
t_{EHEL}	$\overline{CE}$ Pulse Width High	70		60		ns
t_{GHEL}	Read Recovery before Write	0		0		ns
t_{EHRL}	$\overline{CE}$ High to RY/$\overline{BY}$ Going Low		190		165	ns
t_{RHPL}	$\overline{RP}$ Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/$\overline{BY}$ High	0		0		ns
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low	1.5		1.25		μs
t_{EHGL}	Write Recovery before Read	110		100		ns
t_{QVVL}	V_{PP} Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/$\overline{BY}$ High	0		0		μs
t_{EHQV1}	Duration of Word/Byte Write Operation (Measured to Valid Status Register Data)	3.0		3.6		μs
t_{EHQV2}	Duration of Block Erase Operation (Measured to Valid Status Register Data)	0.2		0.24		s

†Address lines $A_{20}-A_{24}$ must be valid during the entire $\overline{WE}$ Low pulse.

AC Electrical Characteristics $\overline{WE}$ Controlled Page Buffer Write Operations

Symbol	Parameter	Military $T_C = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		Industrial $T_C = -45°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$		Units
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	160		140		ns
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low	40		35		ns
t_{AVWL}	Address Setup to $\overline{WE}$ Going Low†	20		15		ns
t_{DVWH}	Data Setup to $\overline{WE}$ Going High	70		60		ns
t_{WLWH}	$\overline{WE}$ Pulse Width Low	70		60		ns
t_{WHDX}	Data Hold from $\overline{WE}$ High	10		5		ns
t_{WHAX}	Address Hold from $\overline{WE}$ High	20		15		ns
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High	20		15		ns
t_{WHWL}	$\overline{WE}$ Pulse Width High	70		60		ns
t_{GHWL}	Read Recovery before Write	0		0		ns
t_{WHGL}	Write Recovery before Read	110		100		ns

†Address must be valid during the entire $\overline{WE}$ Low pulse.

AC Electrical Characteristics $\overline{CE}$ Controlled Page Buffer Write Operations

Symbol	Parameter	Military $T_C = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		Industrial $T_C = -45°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$		Units
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	160		140		ns
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low	0		0		ns
t_{AVEL}	Address Setup to $\overline{CE}$ Going Low†	0		0		ns
t_{DVEH}	Data Setup to $\overline{CE}$ Going High	55		45		ns
t_{ELEH}	$\overline{CE}$ Pulse Width Low	70		60		ns
t_{EHDX}	Data Hold from $\overline{CE}$ High	40		35		ns
t_{EHAX}	Address Hold from $\overline{CE}$ High	55		45		ns
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ High	55		45		ns
t_{EHEL}	$\overline{CE}$ Pulse Width High	70		60		ns
t_{GHEL}	Read Recovery before Write	0		0		ns
t_{EHGL}	Write Recovery before Read	110		100		ns

†Address must be valid during the entire $\overline{CE}$ Low pulse.

AC Electrical Characteristics Write and Erase Performance (Excluding System Level Overhead)

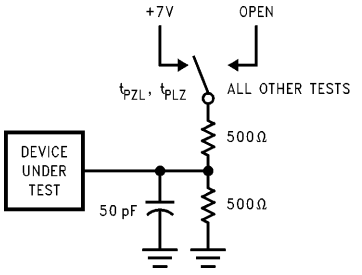
Symbol	Parameter	Military $T_C = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		Industrial $T_C = -45°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$		Units
		Typ†	Max	Typ†	Max	
t_{WHRH1}	Word/Byte Write Time	6		6		μs
t_{WHRH2}	Block Write Time (Byte Write Mode)	0.4	3.0	0.4	2.5	s
t_{WHRH3}	Block Write Time (Word Write Mode)	0.2	1.4	0.2	1.2	s
	Block Erase Time	0.6	1.4	0.6	12	s
	Full Page Erase Time	19.2		19.2		s

†25°C, $V_{PP} = 12.0V$, $V_{CC} = 5.0V$.

Capacitance

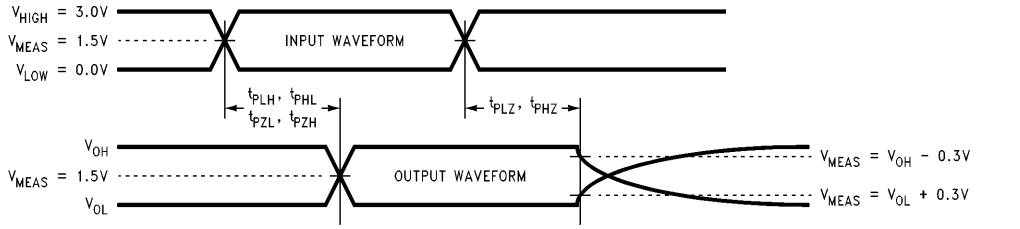
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	10	pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Pin Capacitance	25	pF	V_{CC} = 5.0

AC Testing Load Circuit



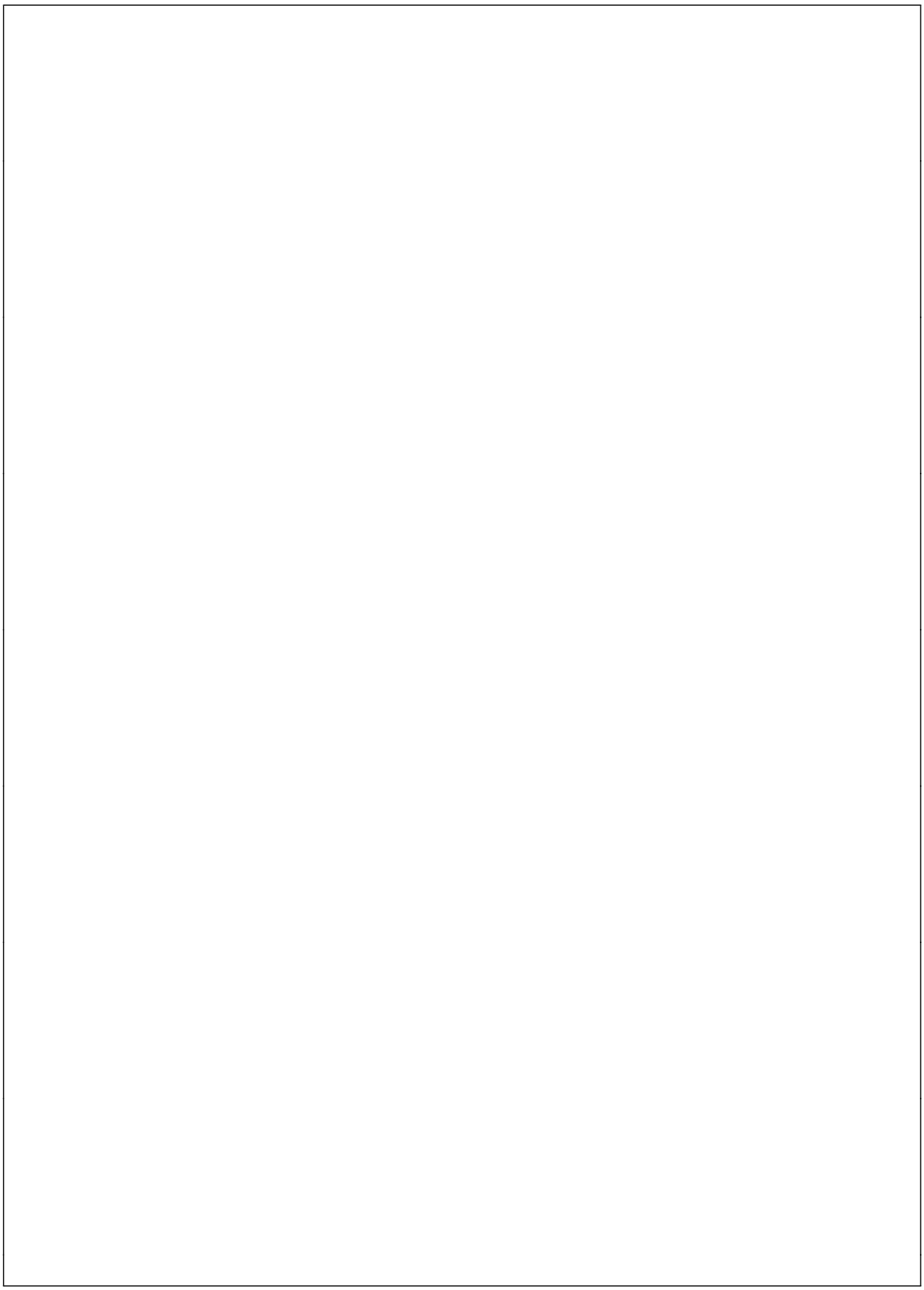
TL/Z/12436–3

AC Reference Waveforms

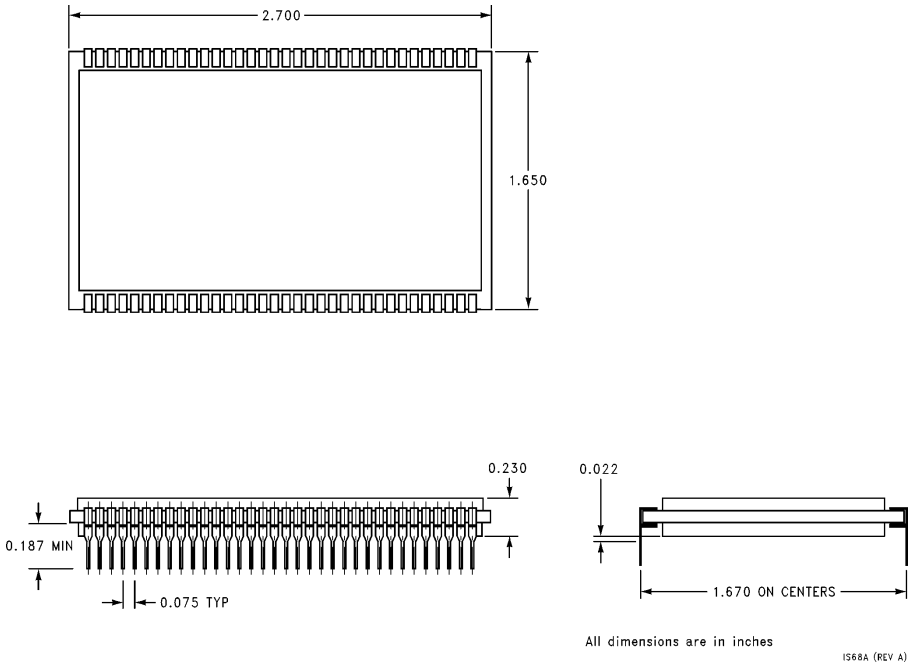


TL/Z/12436–4

Input rise and fall times (10%–90%) = 3 ns

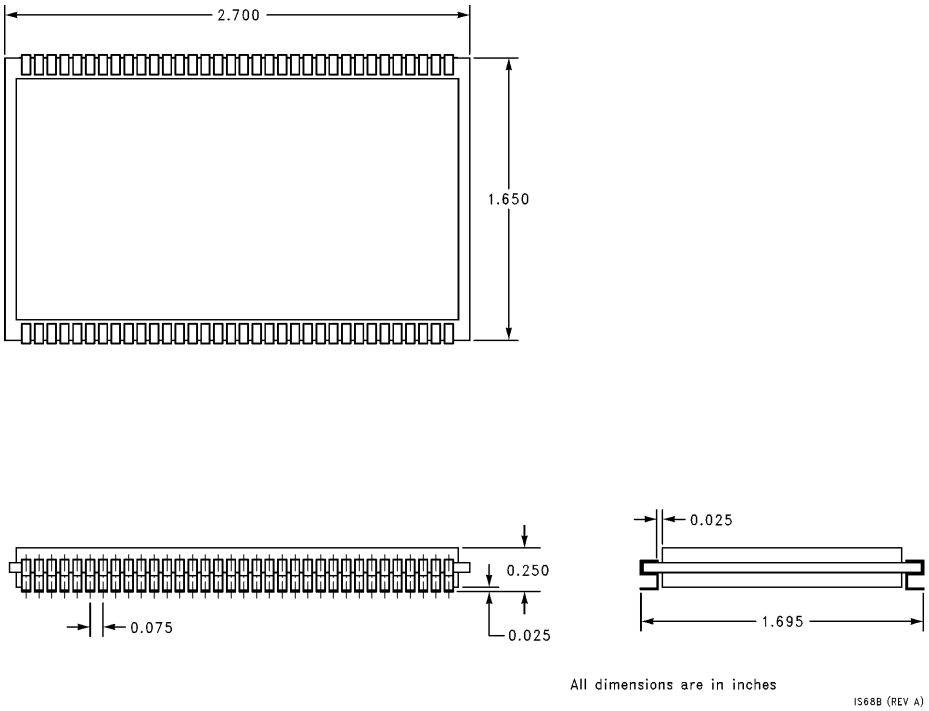


Physical Dimensions (inches)



68-Lead, Hermetic, Dual-In-Line, Custom, ISPMCM-DC Package
NS Package Number IS68A

Physical Dimensions (inches) (Continued)



All dimensions are in inches

IS68B (REV A)

68-Lead, Hermetic, Surface Mount, Custom, ISPMCM-DC Package
NS Package Number IS68B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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