MC74VHC541

Octal Bus Buffer

The MC74VHC541 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC541 is a noninverting type. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: t_{PD} = 3.7ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

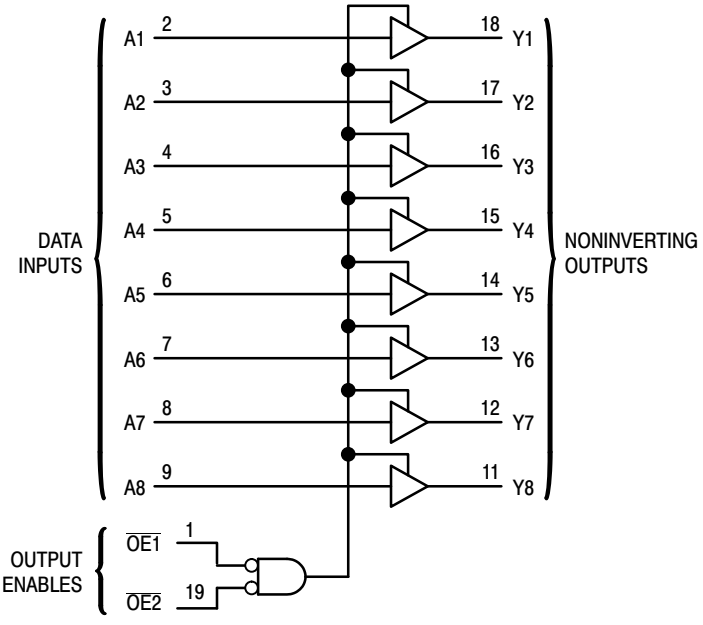

Figure 1. Logic Diagram

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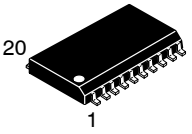
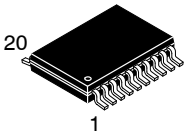
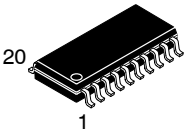


SOIC−20WB
SUFFIX DW
CASE 751D

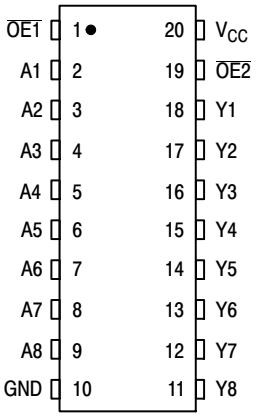


TSSOP−20
SUFFIX DT
CASE 948E



SOEIAJ−20
SUFFIX M
CASE 967

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage	− 0.5 to + 7.0	V
V_{out}	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	− 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Packages: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−55	+125	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3V ±0.3V V_{CC} = 5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = − 55 to 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = − 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = − 4mA I_{OH} = − 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A = -55$ to $125°C$ Min	$T_A = -55$ to $125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 3.3 \pm 0.3V$	$C_L = 15pF$		5.0	7.0	1.0	8.5	ns
			$C_L = 50pF$		7.5	10.5	1.0	12.0	
		$V_{CC} = 5.0 \pm 0.5V$	$C_L = 15pF$		3.5	5.0	1.0	6.0	
			$C_L = 50pF$		5.0	7.0	1.0	8.0	
t_{PZL}, t_{PZH}	Output Enable TIme, $\overline{OE}$ to Y	$V_{CC} = 3.3 \pm 0.3V$, $R_L = 1k\Omega$	$C_L = 15pF$		6.8	10.5	1.0	12.5	ns
			$C_L = 50pF$		9.3	14.0	1.0	16.0	
		$V_{CC} = 5.0 \pm 0.5V$, $R_L = 1k\Omega$	$C_L = 15pF$		4.7	7.2	1.0	8.5	
			$C_L = 50pF$		6.2	9.2	1.0	10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Y	$V_{CC} = 3.3 \pm 0.3V$, $R_L = 1k\Omega$	$C_L = 50pF$		11.2	15.4	1.0	17.5	ns
		$V_{CC} = 5.0 \pm 0.5V$, $R_L = 1k\Omega$	$C_L = 50pF$		6.0	8.8	1.0	10.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3V$ (Note 1)	$C_L = 50pF$			1.5		1.5	ns
		$V_{CC} = 5.0 \pm 0.5V$ (Note 1)	$C_L = 50pF$			1.0		1.0	ns
C_{in}	Maximum Input Capacitance				4	10		10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High Impedance State)				6				pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 2)	18	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0V$)

Symbol	Parameter	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.9	− 1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

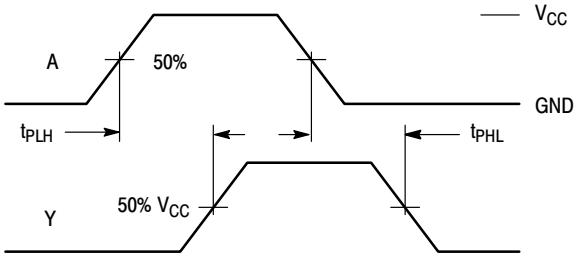


Figure 2.

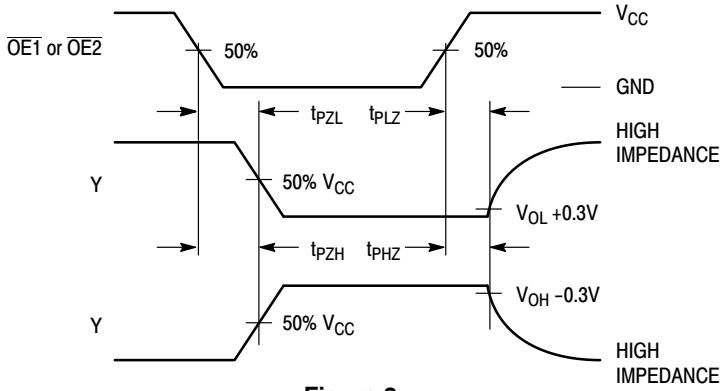
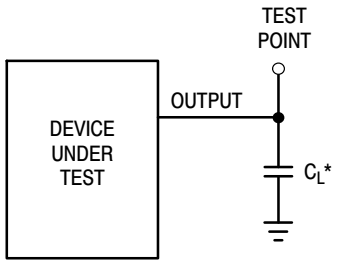


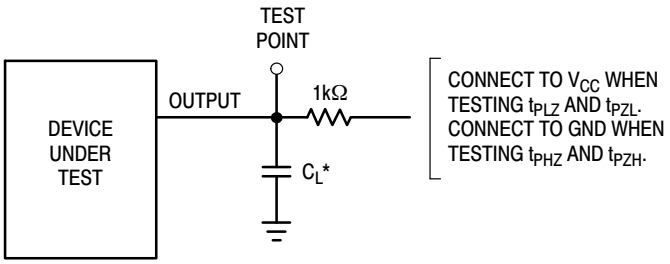
Figure 3.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 4.



*Includes all probe and jig capacitance

Figure 5.

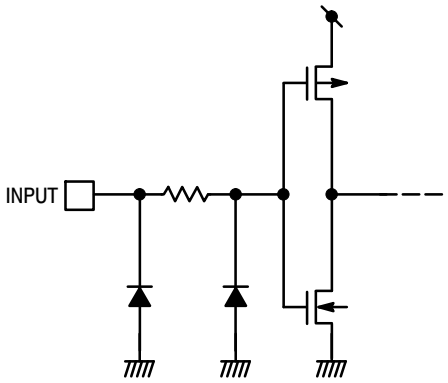


Figure 6. Input Equivalent Circuit

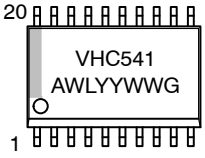
ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC541DWR2G	SOIC−20WB (Pb−Free)	1000 / Tape & Reel
MC74VHC541DTG	TSSOP−20 (Pb−Free)	75 Units / Rail
MC74VHC541DTR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel
MC74VHC541MELG	SOEIAJ−20 (Pb−Free)	2000 / Tape & Reel

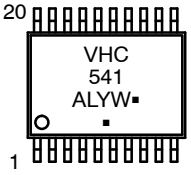
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

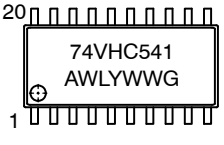
SOIC−20WB



TSSOP−20



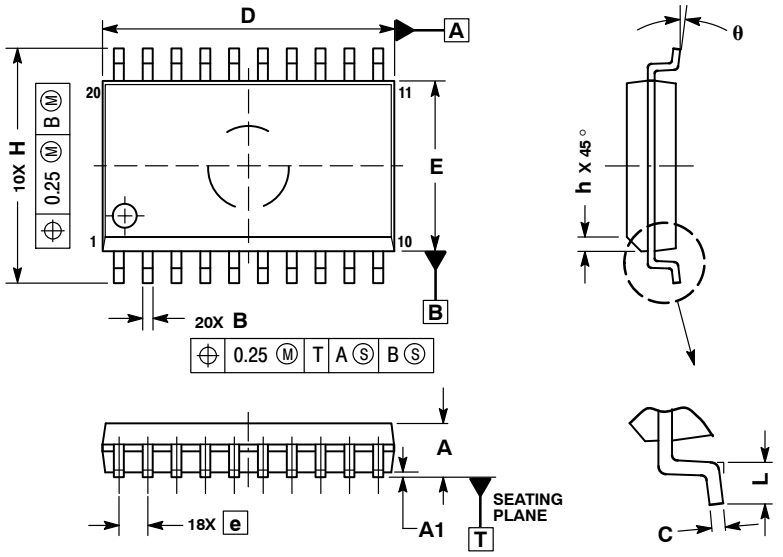
SOEIAJ−20



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

PACKAGE DIMENSIONS

SOIC−20 WB
DW SUFFIX
CASE 751D−05
ISSUE G

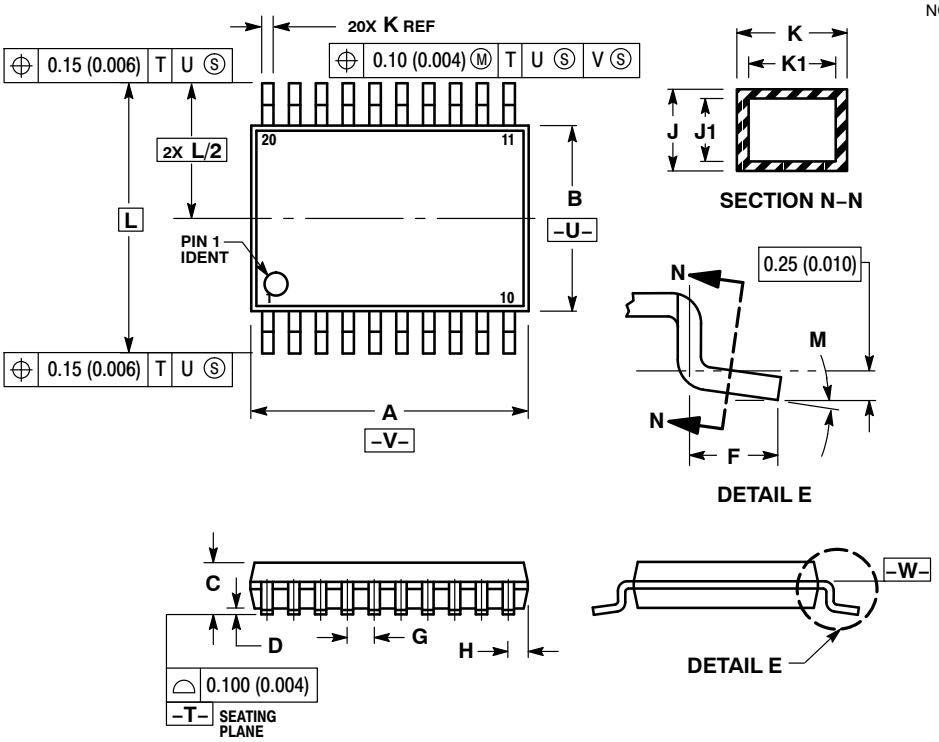


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

PACKAGE DIMENSIONS

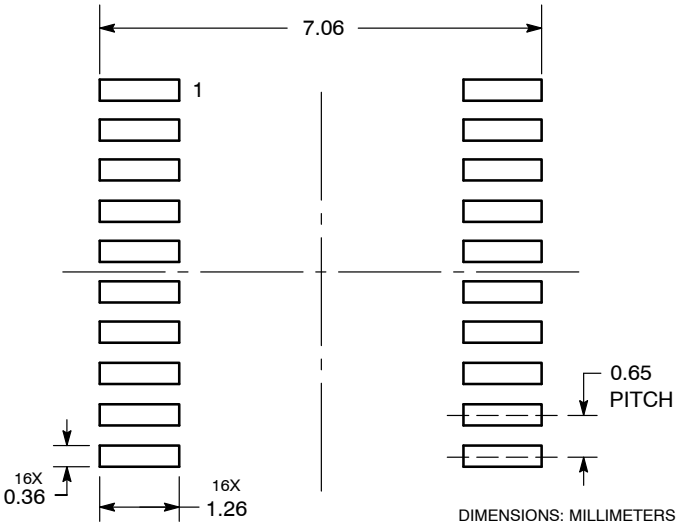
TSSOP−20
CASE 948E−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

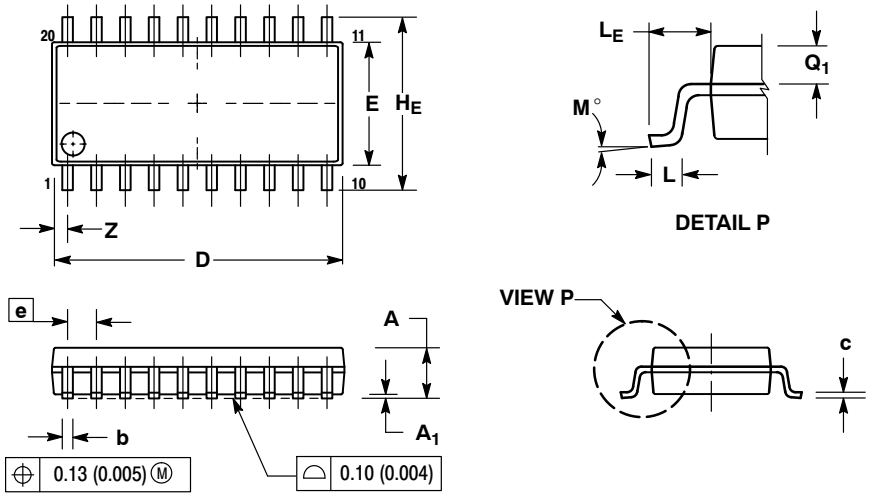
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

SOEIAJ–20
M SUFFIX
CASE 967
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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