# Low-Voltage CMOS Octal Transceiver/Registered Transceiver

## With 5 V–Tolerant Inputs and Outputs (3–State, Non–Inverting)

The MC74LCX646 is a high performance, non–inverting octal transceiver/registered transceiver operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $V_I$ specification of 5.5 V allows MC74LCX646 inputs to be safely driven from 5 V devices. The MC74LCX646 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

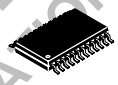
Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW–to–HIGH logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBA, SAB) can multiplex stored and real–time (transparent mode) data. The direction control (DIR) determines which bus will receive data when the enable $\overline{OE}$ is active LOW. In the isolation mode ($\overline{OE}$ HIGH), A data may be stored in the B register or B data may be stored in the A register. Only one of the two buses, A or B, may be driven at one time.

- Designed for 2.3 to 3.6 V $V_{CC}$ Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$ Specification Guarantees High Impedance When $V_{CC}$ = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V

**MC74LCX646**

**LCX**

**LOW–VOLTAGE CMOS OCTAL TRANSCEIVER/ REGISTERED TRANSCEIVER**



**DT SUFFIX**
24–LEAD PLASTIC TSSOP PACKAGE
CASE 948H

**DW SUFFIX**
24–LEAD PLASTIC SOIC PACKAGE
CASE 751E

**PIN NAMES**

| Pins | Function |
|---|---|
| A0–A7 | Side A Inputs/Outputs |
| B0–B7 | Side B Inputs/Outputs |
| CAB, CBA | Clock Pulse Inputs |
| SAB, SBA | Select Control Inputs |
| DIR, $\overline{OE}$ | Output Enable Inputs |

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June, 2006 – Rev. 5
Publication Order Number:
MC74LCX646/D

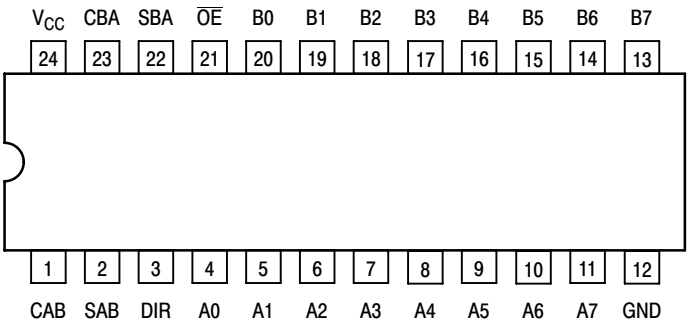


**Figure 1. Pinout: 24−Lead Package** (Top View)

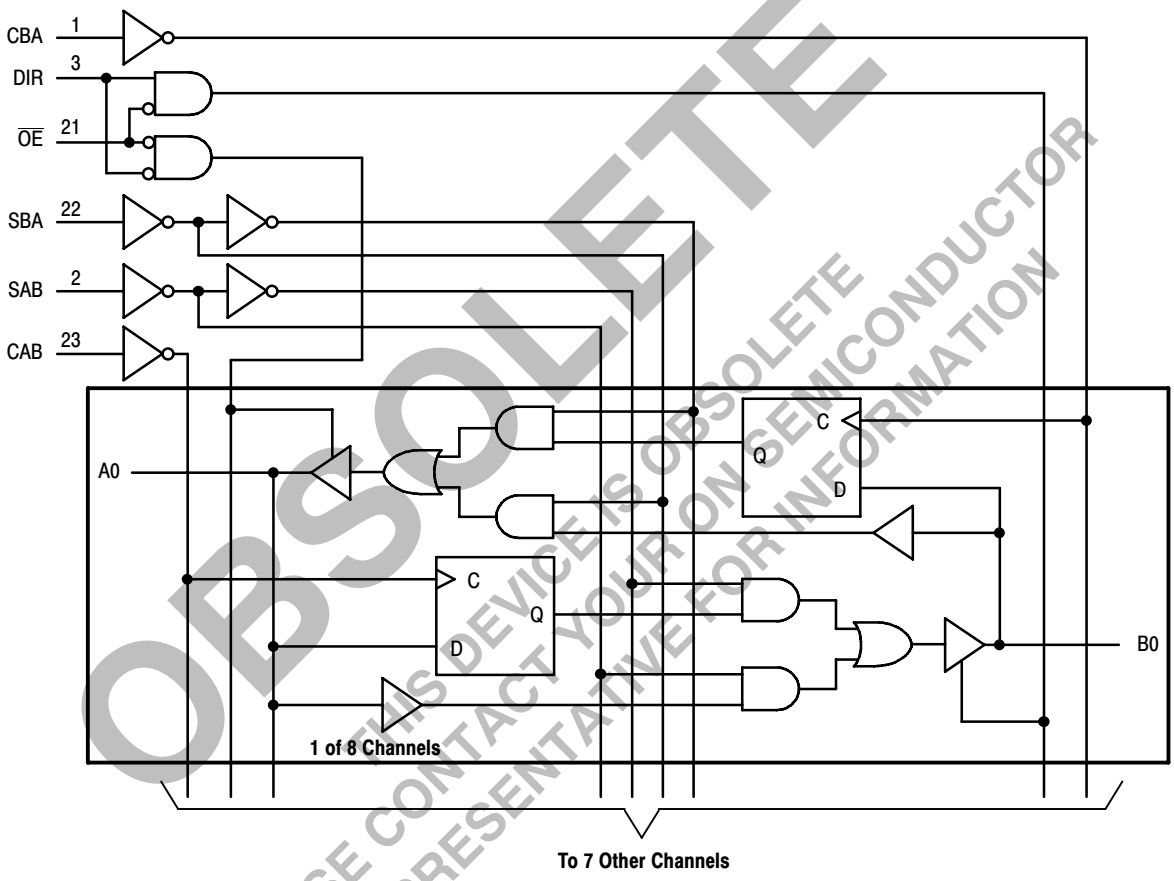


**Figure 2. LOGIC DIAGRAM**

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**TRUTH TABLE**

| Inputs | | | | | | Data Ports | | Operating Mode |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CAB | CBA | SAB | SBA | An | Bn | |
| H | X | | | | | **Input** | **Input** | |
| | | ↑ | ↑ | X | X | X | X | Isolation, Hold Storage |
| | | ↑ | ↑ | X | X | l<br>h<br>X<br>X | X<br>X<br>l<br>h | Store A and/or B Data |
| L | H | | | | | **Input** | **Output** | |
| | | ↑ | X* | L | X | L<br>H | L<br>H | Real Time A Data to B Bus |
| | | | | H | X | X | QA | Stored A Data to B Bus |
| | | ↑ | X* | L | X | l<br>h | L<br>H | Real Time A Data to B Bus; Store A Data |
| | | | | H | X | L<br>H | QA<br>QA | Clock A Data to B Bus; Store A Data |
| L | L | | | | | **Output** | **Input** | |
| | | X* | ↑ | X | L | L<br>H | L<br>H | Real Time B Data to A Bus |
| | | | | X | H | QB | X | Stored B Data to A Bus |
| | | X* | ↑ | X | L | L<br>H | l<br>h | Real Time B Data to A Bus; Store B Data |
| | | | | X | H | QB<br>QB | L<br>H | Clock B Data to A Bus; Store B Data |

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low−to−High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low−to−High Clock Transition
X = Don't Care
↑ = Low−to−High Clock Transition
↑ = NOT Low−to−High Clock Transition
QA = A input storage register
QB = B input storage register
* = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For $I_{CC}$ reasons, Do Not Float Inputs.

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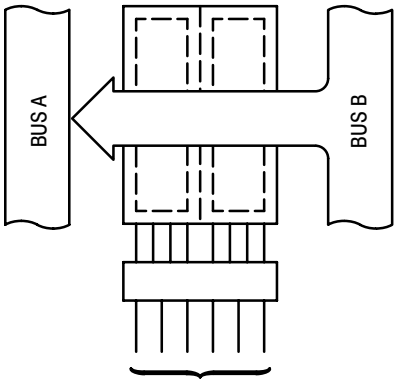
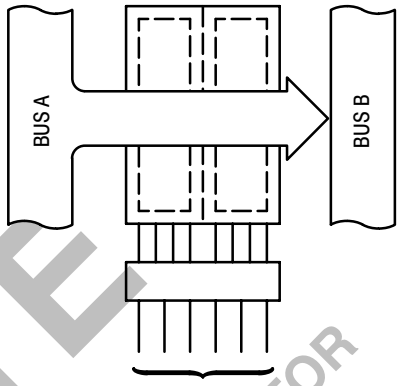
## BUS APPLICATIONS

**Real Time Transfer – Bus B to Bus A**



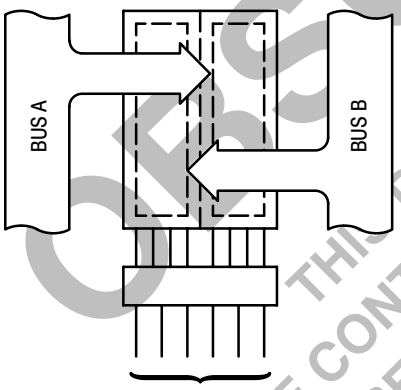

| $\overline{OE}$ | DIR | CAB | CBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**Real Time Transfer – Bus A to Bus B**



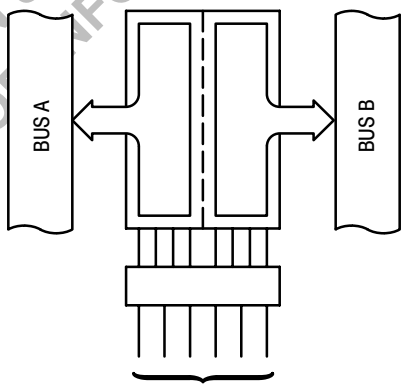

| $\overline{OE}$ | DIR | CAB | CBA | SAB | SBA |
|---|---|---|---|---|---|
| L | H | X | X | L | X |

**Store Data from Bus A, Bus B or Busses A and B**




| $\overline{OE}$ | DIR | CAB | CBA | SAB | SBA |
|---|---|---|---|---|---|
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**Transfer Storage Data to Bus A or Bus B**




| $\overline{OE}$ | DIR | CAB | CBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | H or L | X | H |
| L | H | H or L | X | H | X |

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## MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | −0.5 to +7.0 | | V |
| $V_I$ | DC Input Voltage | $-0.5 \le V_I \le +7.0$ | | V |
| $V_O$ | DC Output Voltage | $-0.5 \le V_O \le +7.0$ | Output in 3−State | V |
| | | $-0.5 \le V_O \le V_{CC} + 0.5$ | Note 1. | V |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I < GND$ | mA |
| $I_{OK}$ | DC Output Diode Current | −50 | $V_O < GND$ | mA |
| | | +50 | $V_O > V_{CC}$ | mA |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current Per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current Per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature Range | −65 to +150 | | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Output in HIGH or LOW State. $I_O$ absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating<br>Data Retention Only | 2.0<br>1.5 | 3.3<br>3.3 | 3.6<br>3.6 | V |
| $V_I$ | Input Voltage | | 0 | | 5.5 | V |
| $V_O$ | Output Voltage | (HIGH or LOW State)<br>(3−State) | 0<br>0 | | $V_{CC}$<br>5.5 | V |
| $I_{OH}$ | HIGH Level Output Current, $V_{CC}$ = 3.0 V − 3.6 V | | | | −24 | mA |
| $I_{OL}$ | LOW Level Output Current, $V_{CC}$ = 3.0 V − 3.6 V | | | | 24 | mA |
| $I_{OH}$ | HIGH Level Output Current, $V_{CC}$ = 2.7 V − 3.0 V | | | | −12 | mA |
| $I_{OL}$ | LOW Level Output Current, $V_{CC}$ = 2.7 V − 3.0 V | | | | 12 | mA |
| $T_A$ | Operating Free−Air Temperature | | −40 | | +85 | °C |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC}$ = 3.0 V | | 0 | | 10 | ns/V |

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## DC ELECTRICAL CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A$ = −40°C to +85°C | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage (Note 2.) | $2.7 V \le V_{CC} \le 3.6 V$ | 2.0 | | V |
| $V_{IL}$ | LOW Level Input Voltage (Note 2.) | $2.7 V \le V_{CC} \le 3.6 V$ | | 0.8 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $2.7 V \le V_{CC} \le 3.6 V$; $I_{OH}$ = −100 μA | $V_{CC}$ − 0.2 | | V |
| | | $V_{CC}$ = 2.7 V; $I_{OH}$ = −12 mA | 2.2 | | |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −18 mA | 2.4 | | |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −24 mA | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | $2.7 V \le V_{CC} \le 3.6 V$; $I_{OL}$ = 100 μA | | 0.2 | V |
| | | $V_{CC}$ = 2.7 V; $I_{OL}$= 12 mA | | 0.4 | |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 16 mA | | 0.4 | |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 24 mA | | 0.55 | |

2. These values of $V_I$ are used to test DC electrical characteristics only.

**DC ELECTRICAL CHARACTERISTICS** (Continued)

| Symbol | Characteristic | Condition | $T_A$ = −40°C to +85°C | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_I$ | Input Leakage Current | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V; 0 V ≤ $V_I$ ≤ 5.5 V | | ±5.0 | μA |
| $I_{OZ}$ | 3−State Output Current | 2.7 ≤ $V_{CC}$ ≤ 3.6 V; 0 V ≤ $V_O$ ≤ 5.5 V; $V_I$ = $V_{IH}$ or $V_{IL}$ | | ±5.0 | μA |
| $I_{OFF}$ | Power−Off Leakage Current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 5.5 V | | 10 | μA |
| $I_{CC}$ | Quiescent Supply Current | 2.7 ≤ $V_{CC}$ ≤ 3.6 V; $V_I$ = GND or $V_{CC}$ | | 10 | μA |
| | | 2.7 ≤ $V_{CC}$ ≤ 3.6 V; 3.6 ≤ $V_I$ or $V_O$ ≤ 5.5 V | | ±10 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | 2.7 ≤ $V_{CC}$ ≤ 3.6 V; $V_{IH}$ = $V_{CC}$ − 0.6 V | | 500 | μA |

**AC CHARACTERISTICS** ($t_R$ = $t_F$ = 2.5 ns; $C_L$ = 50 pF; $R_L$ = 500 Ω)

| Symbol | Parameter | Waveform | Limits | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = −40°C to +85°C | | | | |
| | | | $V_{CC}$ = 3.0 V to 3.6 V | | $V_{CC}$ = 2.7 V | | |
| | | | Min | Max | Min | Max | |
| $f_{max}$ | Clock Pulse Frequency | 3 | 150 | | | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Input to Output | 1 | 1.5<br>1.5 | 7.0<br>7.0 | 1.5<br>1.5 | 8.0<br>8.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Clock to Output | 3 | 1.5<br>1.5 | 8.5<br>8.5 | 1.5<br>1.5 | 9.5<br>9.5 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Select to Output | 1 | 1.5<br>1.5 | 8.5<br>8.5 | 1.5<br>1.5 | 9.5<br>9.5 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time to<br>High and Low Level | 2 | 1.5<br>1.5 | 8.5<br>8.5 | 1.5<br>1.5 | 9.5<br>9.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time From<br>High and Low Level | 2 | 1.5<br>1.5 | 8.5<br>8.5 | 1.5<br>1.5 | 9.5<br>9.5 | ns |
| $t_s$ | Setup Time, HIGH or LOW Data to Clock | 3 | 2.5 | | 2.5 | | ns |
| $t_h$ | Hold Time, HIGH or LOW Data to Clock | 3 | 1.5 | | 1.5 | | ns |
| $t_w$ | Clock Pulse Width, HIGH or LOW | 3 | 3.3 | | 3.3 | | ns |
| $t_{OSHL}$<br>$t_{OSLH}$ | Output−to−Output Skew<br>(Note 3.) | | | 1.0<br>1.0 | | | ns |

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW ($t_{OSHL}$) or LOW−to−HIGH ($t_{OSLH}$); parameter guaranteed by design.

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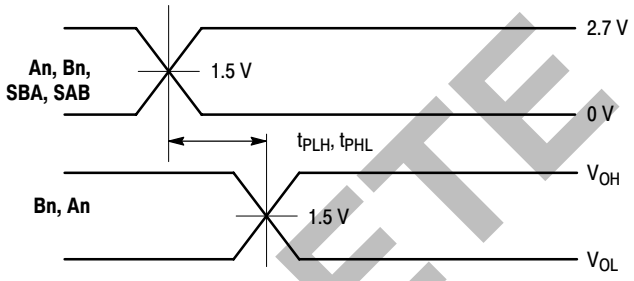
**DYNAMIC SWITCHING CHARACTERISTICS**

| Symbol | Characteristic | Condition | $T_A$ = +25°C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 4.) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V | | 0.8 | | V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 4.) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V | | 0.8 | | V |

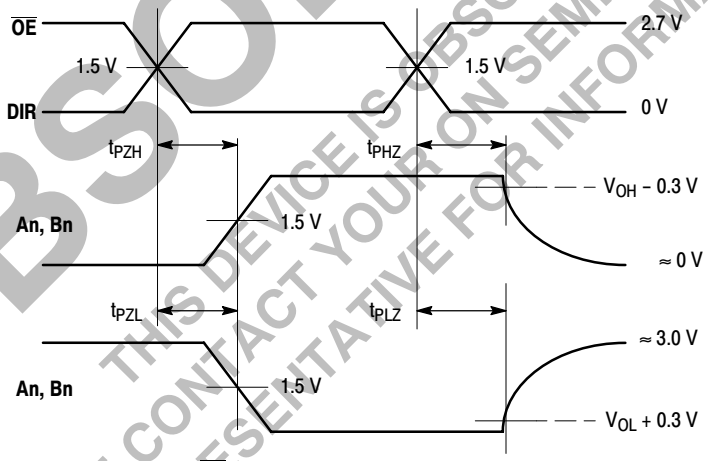
4. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

**CAPACITIVE CHARACTERISTICS**

| Symbol | Parameter | Condition | Typical | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 7 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | 10MHz, $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 25 | pF |




**WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns




**WAVEFORM 2 – OE/DIR to An/Bn OUTPUT ENABLE AND DISABLE TIMES**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns

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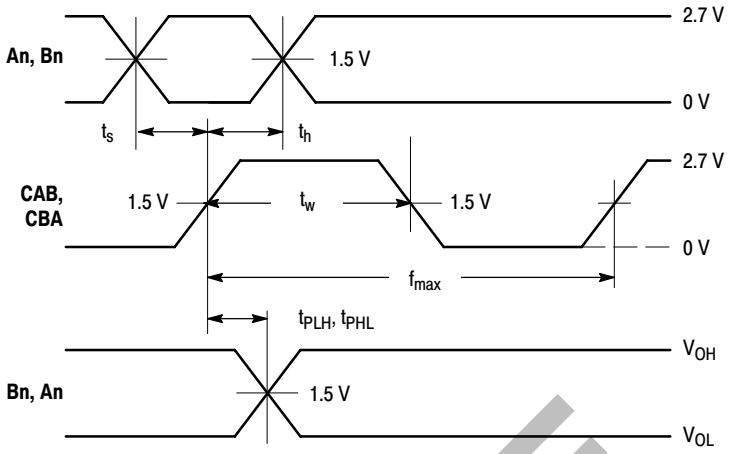
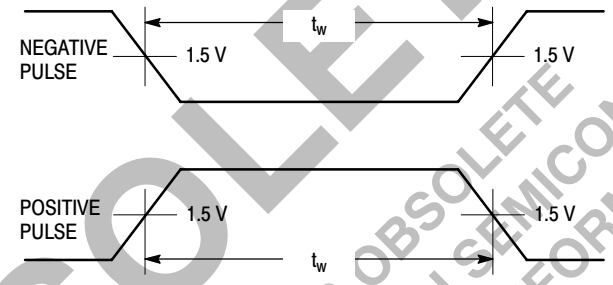
**Figure 3. AC Waveforms**




**WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES**

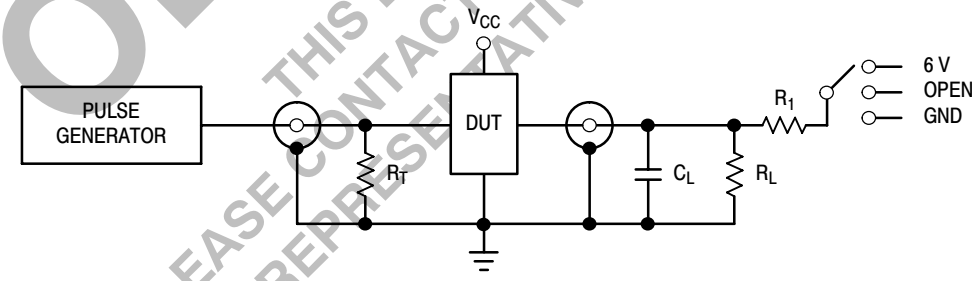
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns except when noted




**WAVEFORM 4 – INPUT PULSE DEFINITION**

$t_R = t_F$ = 2.5 ns, 10% to 90% of 0 V to 2.7 V

**Figure 4. AC Waveforms**




| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6 V |
| Open Collector/Drain $t_{PLH}$ and $t_{PHL}$ | 6 V |
| $t_{PZH}$, $t_{PHZ}$ | GND |

$C_L$ = 50 pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500 Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

**Figure 5. Test Circuit**

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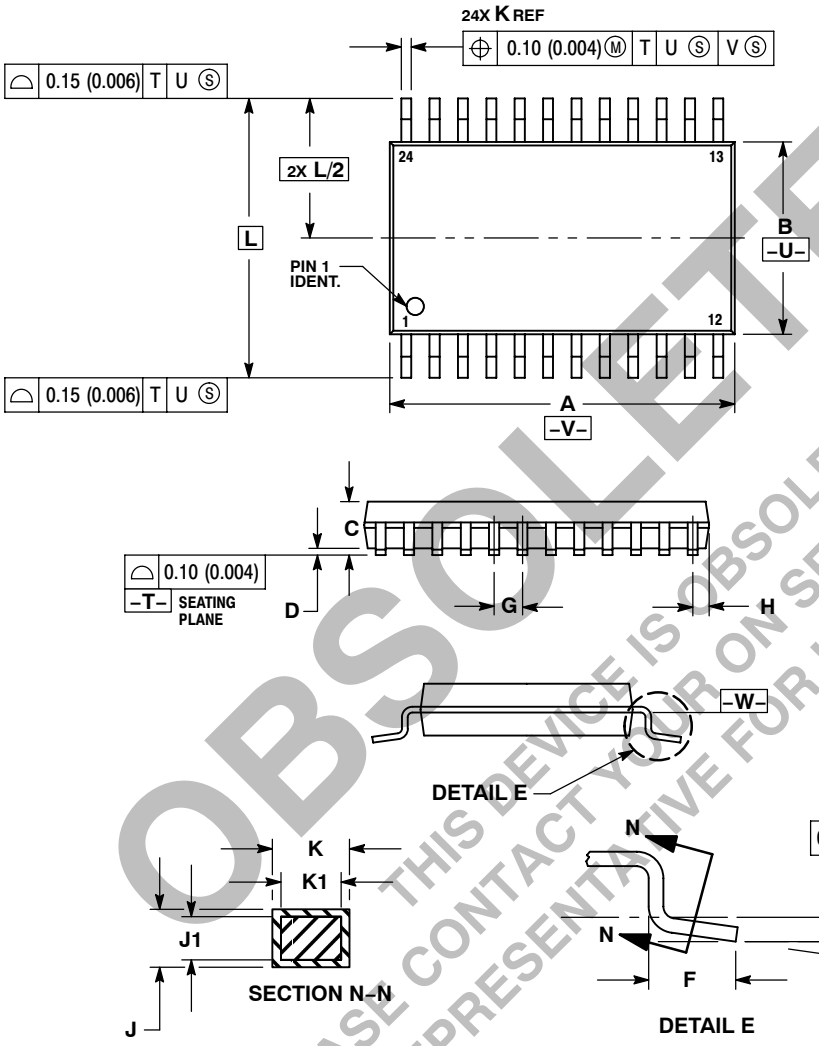
## PACKAGE DIMENSIONS

**DT SUFFIX**
PLASTIC TSSOP PACKAGE
CASE 948H–01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.70 | 7.90 | 0.303 | 0.311 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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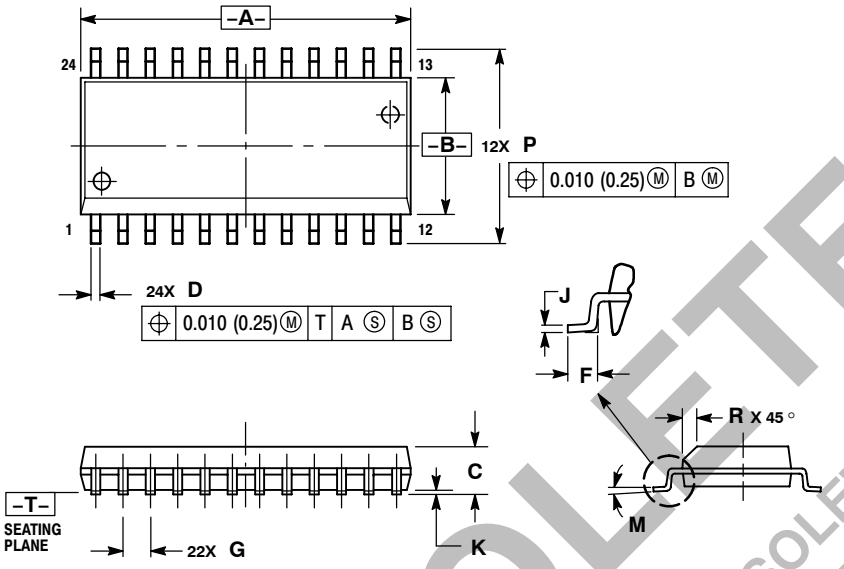
## PACKAGE DIMENSIONS

**DW SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 15.25 | 15.54 | 0.601 | 0.612 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.41 | 0.90 | 0.016 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.23 | 0.32 | 0.009 | 0.013 |
| K | 0.13 | 0.29 | 0.005 | 0.011 |
| M | 0° | 8° | 0° | 8° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

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