Device Errata

MC68360 QUICC

Revision B.2. Masks 2C69T, 0F35G, 1F35G, 0F34G, and 1F34G.

January 26, 1996

These errata items are valid on B.2 silicon. Please note that any errata listed in this document also applies to older revisions, unless otherwise stated. I n this document, mention is made of Revision C which is an all-layers revision and is currently shipping in volume.

Revision B.1 was the first silicon available of revision B but was not generally sampled. (Revision B.0 does not exist). Revision B.2 has ceased volume production. Revision B.3 was not generally sampled. Revision B.4 has ceased volume production.

Revision C.2 mentioned in earlier sheets has been renamed E.1 Revision E.1 is mentioned in this document but is not sampling at the time of writing. Revision D and Revision E.0 do not exist.

NOTE

This errata sheet is no longer being updated. Any errata that exists on future revisions of the device should be assumed to also exist on Revision B.2 unless specifically stated in the errata item.

CPU32+ Errata

1. CPU corrupting DMA cycles

If the CPU executes the TAS instruction after an unaligned access or split bus access (long access to 8/16-bit port), and a DMA device on the IMB requests the bus during the unaligned access, the TAS bus cycle and the DMA bus cycle will be corrupted. The workaround is to add 2 ‘NOP’ instructions before the TAS instruction. This will be fixed in Rev. C.

2. RMC pin asserting early

If the CPU executes the TAS instruction after an unaligned access or split bus access (long access to 8/16-bit port), the RMC signal will be active for the last bus cycle of the unaligned access (or split bus access). This may lead to confusion when observing bus signals but should not affect operation of the CPU. This will be fixed in Rev. C.

3. BDM DSI Timing Problem

The DSI setup and hold time (specs 80 and 81) are defined to be from the falling edge of CLK01. However, the QUICC currently samples this signal on the rising edge of clock. This will be fixed in Rev

C.1.

SIM60 Errata

1. Synchronous Bus Mode

If synchronous timing on bus signals is used (BSTM in the MCR register = 1) and an external master asserts $\overline{AS}$ while CLK01 is high, the 68360 bus controller will ignore the cycle. The work-around is to synchronize $\overline{AS}$ assertion with CLK01 low. This bug did NOT exist in revision A silicon. This will be fixed in Rev B.3.

NOTE

This only affects masters using 68000-bus timing. 68020/030-type masters assert $\overline{AS}$ on CLK01 low and thus are not affected by this errata.

2. PIT Timer and Software Watchdog Timer skipping interrupts

If the multiplication factor in the PLLCR register is greater than 1, an interrupt generated by the PIT timer or by the software watchdog timer (or reset generated by the software watchdog) may occasionally be skipped. This low-probability occurrence is dependent upon EXTAL frequency , MF value, and process variation and thus cannot be predicted. This bug usually shows up at high temperature or low voltage. This will be fixed in Rev B.4.

NOTE

Even if your system did not exhibit this problem using Rev. A silicon, you should verify that this bug does not appear when using Rev. B parts. It is possible for Rev. B parts to show the problem when Rev. A parts did not.

3. 040 Companion Mode Interrupts, Dual Port RAM Corruption, or Parity Errors

If an interrupt is generated by the PIT or the Software Watchdog, and the BSTM bit in the MCR register is set to **1**, the QUICC will not respond to the IACK cycle and thus a spurious interrupt error will occur when the bus monitor times out.

If an interrupt is generated by the PIT, or the Software Watchdog, and the BSTM bit in the MCR register is set to **0**, the first access to Dual-Port RAM or the QUICC's internal registers will be corrupted if that access is a write. In addition, the parity of all the accesses after the 040 IACK cycle (including the fetch from the vector table) will be calculated with incorrect data, and therefore will generate an improper parity result (possibly resulting in a parity error).

Workaround:
1) Set BSTM to zero. (Note that the BSTM setting should not be relevant in 040 companion mode)
2) Perform a read from an internal register during the interrupt service routine (before any writes to the QUICC's internal memory space if necessary).

NOTE

The work around only fixes the parity calculation after the 040 to Internal read access is performed. Any read accesses prior to that read will result in improper parity calculations and possibly generate parity errors. The vector table can be placed in internal QUICC DPRAM to eliminate the problem.

This will be fixed in Rev. C.

4. Inadvertent Burst-Cycle Assertion after Reset

If the QUICC is in 040-companion mode and the device is above room temperature, the TA* assertion from the QUICC for the first bus cycle may be held for 4 clocks (as if it were a burst-cycle) when the QUICC comes out of Reset. This will not result in any operational failures since the MC68040 inserts three idle clocks between SP fetch and PC fetch. However, this will affect an MC68060 master which has fewer idle clocks. This will be fixed in Rev B.4.

5. Bus Controller Lock in slave mode

If the QUICC is in slave mode with the config pins set to 110 (Slave mode with no global chip select and MBAR at $3FF04), and the device is above room temperature, and an MC68040 is attempting to access that QUICC for the first time, the TA* signal will not be generated from the QUICC and the bus controller will lock (thus it will not accept any further accesses). This will be fixed in Rev B.4.

6. AMUX and/or RAS Assertion Failure

If the memory controller has a DRAM bank programmed to page mode, and a master accesses the DRAM bank followed by an SRAM bank followed by a page-hit to the DRAM bank, AMUX or RAS may not re-assert for that cycle if the chip is above room temperature. This occurs if the master is an internal master or if the SYNC bit (in the GMR register) is set to 1 and the access is by an external master. The workaround is to disable page mode. This will be fixed in Rev. C for 25Mhz operation. This will be fixed in Rev C.1 for 33Mhz, extended termperature, or 3.3V operation.

7. Faulty Chip-Select Address Decoding

An access to the memory range $3FF00 - $3FF0F immediately following an bus cycle which had FC3-0 = ‘0111’ will result in the chip select corresponding to that memory device not asserting for that specific access. For example, if the stack pointer points to an address in the range $3FF00 - $3FF0F and an interrupt occurs, the chip select corresponding to that memory device will not assert on the first access of the stack frame push. Another situation would be an SDMA access to that memory immediately following an interrupt acknoweldge cycle. The workaround is to not place any memory in this addressing range. This will be fixed in Rev. C.1.

8. Corrupt access after DMA bus error

The address of a bus cycle can be corrupted if the following circumstances occur:

A DMA bus cycle (from either IDMA unit or any of the SDMA channels) is terminated by BERR* and the following cycle from the CPU is a non-aligned access (and thus takes two bus cycles to complete).

If this sequence of events occurs, the address of the second CPU bus cycle will be corrupted (it will be the address of the second CPU bus cycle logically ANDed with the address of the first bus cycle).

Work-arounds:
* Use 16-bit mode of the IDMA rather than 32-bit mode. (This will not work-around the SDMA case. However, SDMA bus errors typically do not occur in properly performing systems)
OR
* Don’t use the QUICC bus monitor. Use external circuitry to implement the bus monitor. If the bus cycle to be terminated is a CPU cycle (FC(3)=0), the circuitry should assert BERR*. If the bus cycle to be terminated is a DMA cycle (FC(3)=1), generate DSACK* and assert BERR* on the clock following DSACK* negation.
OR
* Set the SHEN bits in the MCR register to ‘1x’ (show cycles) and have external circuitry assert BR* with the following formula: BR* = !(FC(3) & !AS*). This will generate a one clock idle on the internal bus and avoid the problem.

This item will be fixed in Rev. E.1.

9. PIT and Software Watchdog not deterministic

The prescalers in the periodic interrupt timer (PIT) and the software watchdog (SWT) are not affected by a chip reset. Therefore, the first PIT interrupt or the SWT timeout could occur up to 512 system clocks early if the part has undergone a reset other than power-up. This will be fixed in Rev E.1.

10. Parallel I/O pins are not three-stated immediately after Reset

When the QUICC is reset, the parallel I/O pins (Port A, B, and C) are not three stated until the PLL locks. Thus, any port pins that are programmed as outputs may continue driving until the PLL re-locks after reset. This problem will also occur during power-up reset. In this case, the parallel I/O pins will be in an indeterminate state until the PLL locks. The fix for this has not yet been scheduled.

11.Hardware Breakpoint Generation Error

The hardware breakpoint logic will not detect/generate a breakpoint on any address in an 8-bit or 16-bit memory device. The fix has not yet been scheduled.

CPM Errata

1. Transmit On Demand and HDLC/Local Talk

The TOD command (issued in the TOD Register) is not always executed properly. This may cause excessive flags to be transmitted in HDLC or Local Talk. This will be fixed in Rev B.3.

2. Transparent SCC Bit Reversal

If you are running an SCC in transparent mode AND you have the REVD bit in the GSMR set to 1 AND you are transmitting data from a Buffer Descriptor that has its TC bit set to 0 AND its L bit set to 1, the bytes from the last long word will not be reversed. The workaround is to add the value $FFFFFFFF (which is the same as an idle pattern) to the end of the buffer and to increase the data count by 4. Alternately, the user could manually reverse the data in the last longword rather than padding the buffer. This will be fixed in Rev. E.1.

3. Cannot avoid transmitting BREAK characters in SMC UART

If the SMC port is in UART mode and the STOP TRANSMIT command is executed and the value of the BRKCR register is zero, the SMC UART transmitter will transmit 65536 break characters instead of transmitting no break characters. This will be fixed in Rev E.1. A microcode patch is available that will fix the problem on earlier revisions of silicon.

3. SMC UART Short Start Bit Recognition

If an SMC is being used in UART mode and the received character has a start bit that is shorter than 15/16ths of a bit time, the character will not be received. The limit for start bit recognition will be changed to 9/16ths in Rev E.1.

4. Timer Inaccurate

If timer2 is programmed to be a free-run timer and the user turns timer 1 on and off repeatedly, timer 2 will not increment properly and will count more slowly. This phenomenon will also occur if timer 4 is programmed to be a free-run timer and the user turns timer 3 on and off repeatedly. The work around is to place the free running timers on one pair of timers (1 and 2) and place the timers that are manipulated frequently onto the other pair of timers.(3 and 4). This will be fixed in Rev E.1.

JTAG Errata

1. JTAG PRELOAD Bug

The PRELOAD command cannot be used for two reasons:
a) Pins that default to input can be programmed by the PRELOAD command but cannot be changed to output via the PRELOA command.
b) Pins that default to output cannot be programmed using the PRELOAD command.
Thus standard BSDL files for JTAG are unusable. This bug will be fixed in Rev C.