

Advance Information
FLEX™ DECODER IC

The MC68177 FLEX™ IC simplifies implementation of a FLEX paging device by interfacing with any of several off-the-shelf paging receivers and any of several off-the-shelf host microcontroller/microprocessors. Its primary function is to process information received and demodulated from a FLEX radio paging channel, select messages addressed to the paging device, and communicate the message information to the host. The MC68177 also operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low-power mode when monitoring a single channel for message information.

The block diagram shown below illustrates the major components and functions of the MC68177 IC.

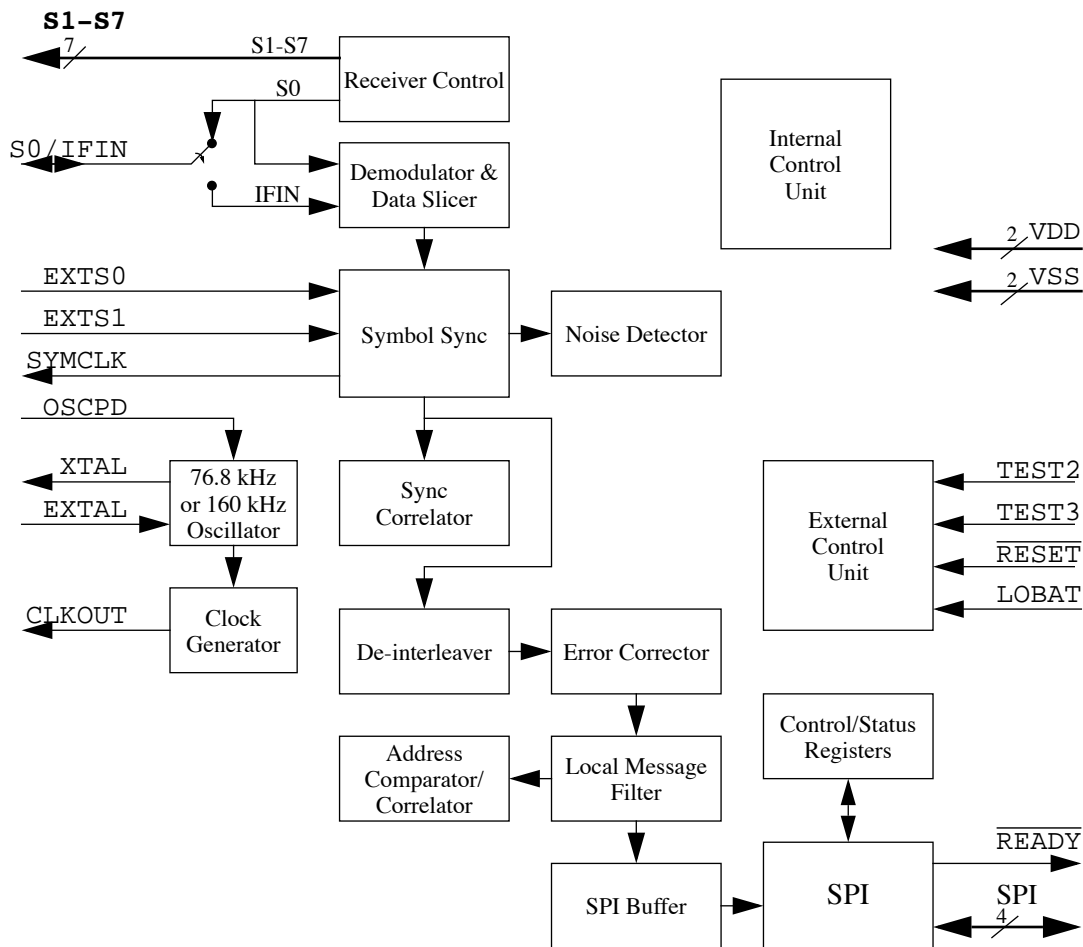


Figure 1 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PRELIMINARY

FEATURES

- FLEX paging protocol signal processor
- 16 programmable user address words
- 16 fixed temporary addresses
- 16 operator messaging addresses
- 1600, 3200, and 6400 bits per second decoding
- Any-phase or single-phase decoding
- Uses standard serial peripheral interface (SPI) in slave mode
- Allows low current STOP mode operation of host processor
- Highly programmable receiver control
- Realtime clock time base
- FLEX fragmentation and group messaging support
- Realtime clock over-the-air update support
- Compatible with synthesized receivers
- Low battery indication (External detector)
- 32-pin QFP package
- Backward compatible to the MC68175 FLEX decoder IC
- Internal demodulator and data slicer
- Improved battery savings via partial correlation and intermittent receiver clock
- Full support for revision 1.9 of the FLEX protocol

PIN DESCRIPTION

Table 1MC68177 Pin Description

Symbol	I/O	32-pin QFP Pin #	Description
VDD (2 pins)	—	3, 13	Power
VSS (2 pins)	—	7, 29	Ground
OSCPD	INPUT	2	Internal oscillator power down. Connected to VSS when using internal oscillator. Connected to VDD when using an external source.
TEST2	INPUT	4	IC manufacturing test mode pin. Normally connected to VSS.
TEST3	INPUT	8	IC manufacturing test mode pin. Normally connected to VSS.
RESET	INPUT	24	Active low reset to the FLEX decoder IC
EXTS1	INPUT	11	MSb of the symbol currently being decoded
EXTS0	INPUT	12	LSb of the symbol currently being decoded
LOBAT	INPUT	10	Low battery detect input
SS	INPUT	27	Slave select for SPI communications
SCK	INPUT	28	Serial clock for SPI communications
MOSI	INPUT	30	Data input for SPI communications
MISO	OUTPUT	31	Three-state data output for SPI communications
READY	OUTPUT	26	Driven low when the IC is ready for an SPI packet
CLKOUT	OUTPUT	32	38.4 kHz or 40 kHz clock output (derived from oscillator)
SYMCLK	OUTPUT	14	Recovered symbol clock
EXTAL	INPUT	6	76.8 kHz crystal input or external input
XTAL	OUTPUT	5	76.8 kHz clock output
S0 / IFIN	OUTPUT/ INPUT	23	Receiver control output when using external demodulator Limited IF input when using internal demodulator
S1 - S7	OUTPUT	22, 21, 20, 19, 18, 16, 15	Eight three-state receiver control ports

PRELIMINARY

APPLICATION EXAMPLES

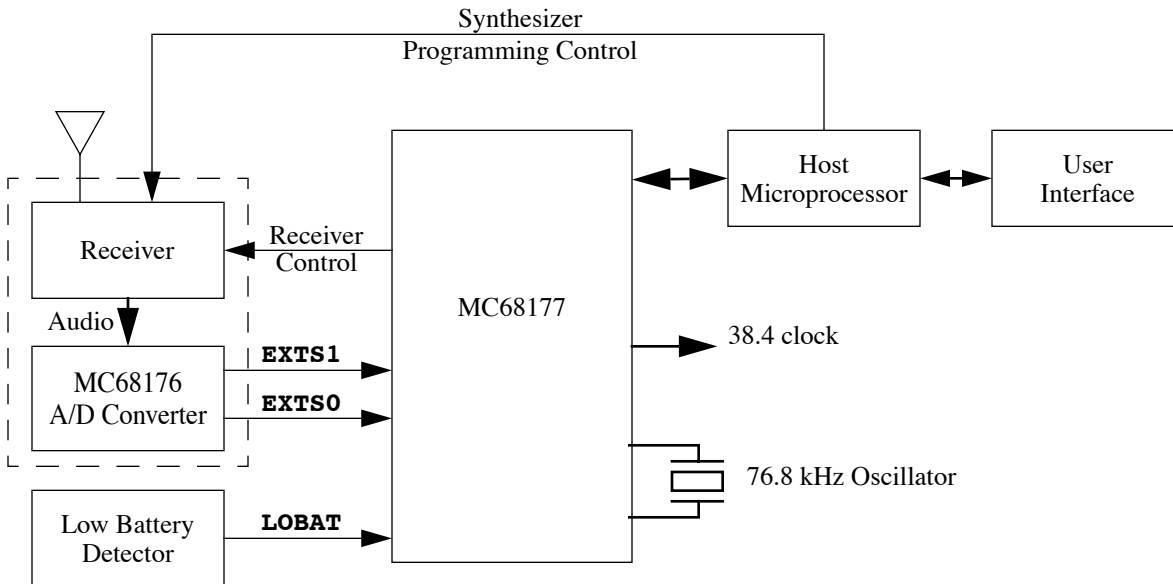


Figure 2 Example Block Diagram Using External Demodulator

The MC68177 IC connects to a receiver capable of converting a 4 level audio signal into a 2-bit digital signal. The FLEX decoder IC has eight receiver control lines used for warming up and shutting down a receiver in stages. The FLEX decoder IC has dual bandwidth control signals for two post detection filter bandwidths for receiving the two symbol rates of the FLEX signal. The FLEX decoder IC has the ability to detect a low battery signal during the receiver control sequences. It interfaces to a host MCU through a standard SPI. It has a 38.4 kHz clock output capable of driving other devices. It has a one minute timer that offers low-power support for a time-of-day function on the host.

APPLICATION EXAMPLES

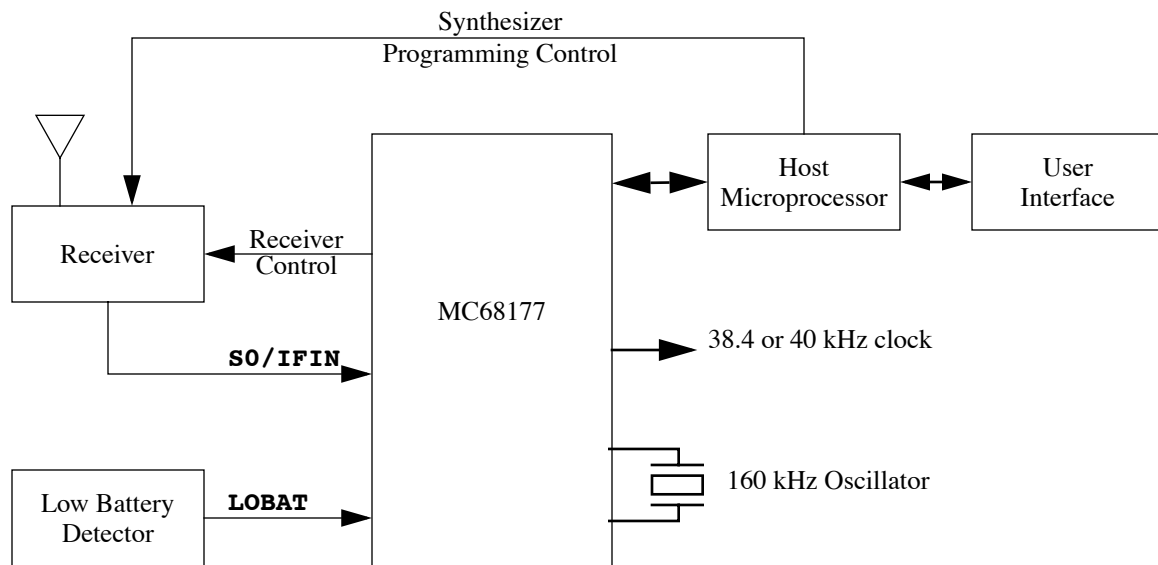



Figure 3 Example Block Diagram Using Internal Demodulator

The MC68177 chip also has an internal demodulator. When using the internal demodulator, a limited (i.e. 1-bit digitized) 455 kHz or 140 kHz IF signal is fed from the receiver into the FLEX decoder IC via the **SO/IFIN** pin. When using the internal demodulator, the oscillator frequency (or external clock) must be 160 kHz. The **CLKOUT** signal can be programmed to be either a 38.4 kHz signal created by fractionally dividing the oscillator clock, or a 40 kHz signal creating by dividing the oscillator clock by 4.

Further information about SPS's Wireless Products is available at <http://www.mot.com/SPS/WIRELESS>. Information on FLEX technology is available on Motorola's Web site at <http://www.motorola.com/FLEX>.

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