Freescale Semiconductor
Product Brief

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MC56F8006/MC56F8002 Digital Signal Controller Product Brief

1 Introduction

1.1 Overview

This document provides an overview of the major features and functional components of the MC56F8006/MC56F8002 series of digital signal controllers (DSCs).

The devices in the MC56F8006/MC56F8002 series combine, on a single chip, the processing power of a digital signal processor (DSP) and the functionality of a microcontroller unit (MCU) with a flexible set of peripherals to create an extremely cost-effective solution.

The MC56F8006/MC56F8002 uses the 56800E core, which is based on a dual Harvard-style architecture consisting of three execution units operating in parallel. This allows as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward

Contents

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generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

A full set of programmable peripherals supports various applications. Any signal pin associated with these peripherals can also be used for general-purpose input/output (GPIO). Power-saving features include an extremely low-power mode and the ability to shut down each peripheral independently.

1.2 Application Examples

Because of its low cost, configuration flexibility, and compact program code, the MC56F8006/MC56F8002 is well-suited for many applications. The MC56F8006/MC56F8002 includes many peripherals that are especially useful for cost-sensitive applications, including:

- Switched-mode, power supply, and power management
- Industrial control
- Home appliances
- Smart sensors
- Fire and security systems
- Power metering
- Motor controls (ACIM, BLDC, PMSM, SR, and Stepper)
- Handheld power tools
- Arc detection
- Medical device/equipment
- Instrumentations
- Lighting ballast

The next sections present two application scenarios that demonstrate how various features of the MC56F8006/MC56F8002 might be used within a product.

1.2.1 Pulse Oximeter

Figure 1 shows a portable, battery-powered pulse oximeter, a medical device that indirectly measures the oxygen saturation of a patient's blood. The MC56F8006/MC56F8002 controls the device. This application requires low-power standby mode and dynamic operation frequency to extend battery life. The high-speed timer module helps to sample in real time the two-wavelength digital light-signal pulses that pass through the detector.

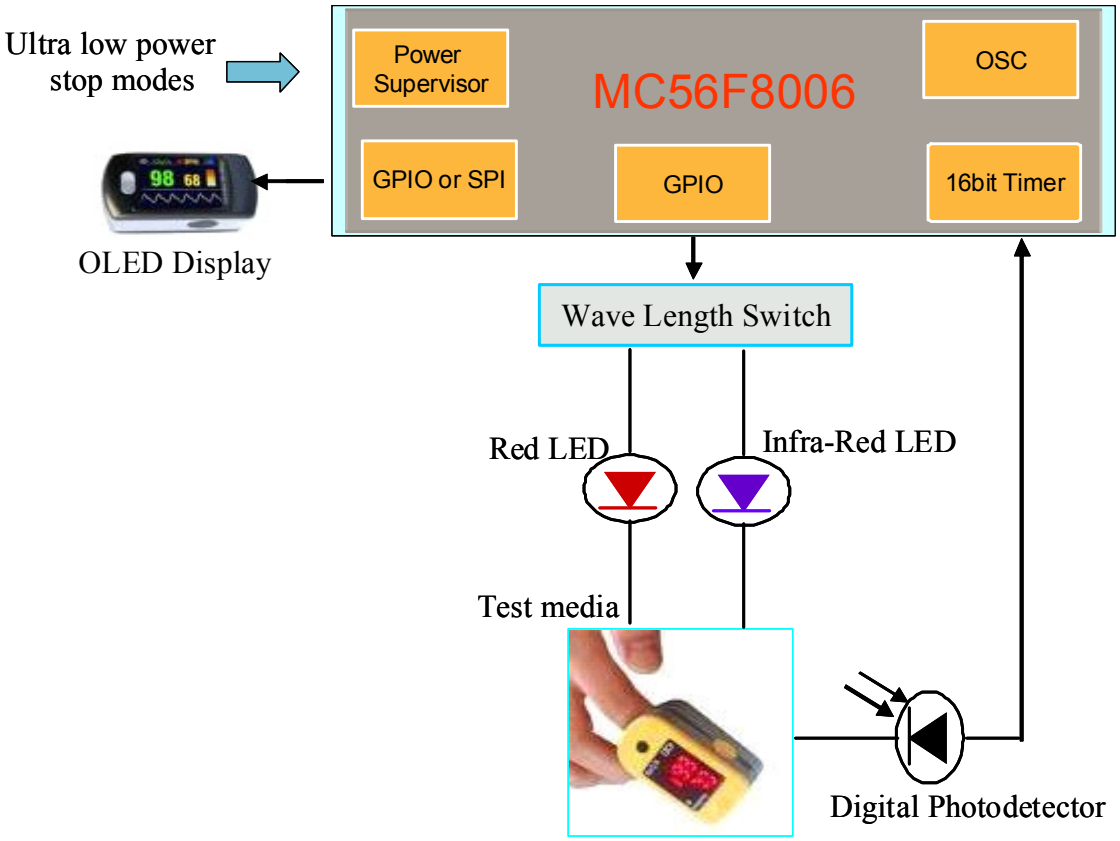

Figure 1. Pulse Oximeter

1.2.2 PWM with Single Shunt Resistor as Feedback Sensor

Figure 2 shows the PWM outputs of the MC56F8006/MC56F8002 that control three half H-bridge circuits driving a three-phase AC motor with an R_{Sense} current shunt in series with the negative power connection. R_{Sense} is normally a low-valued resistor (0.01–0.1 Ω) used to convert the motor currents into a voltage that can be measured for feedback purposes.

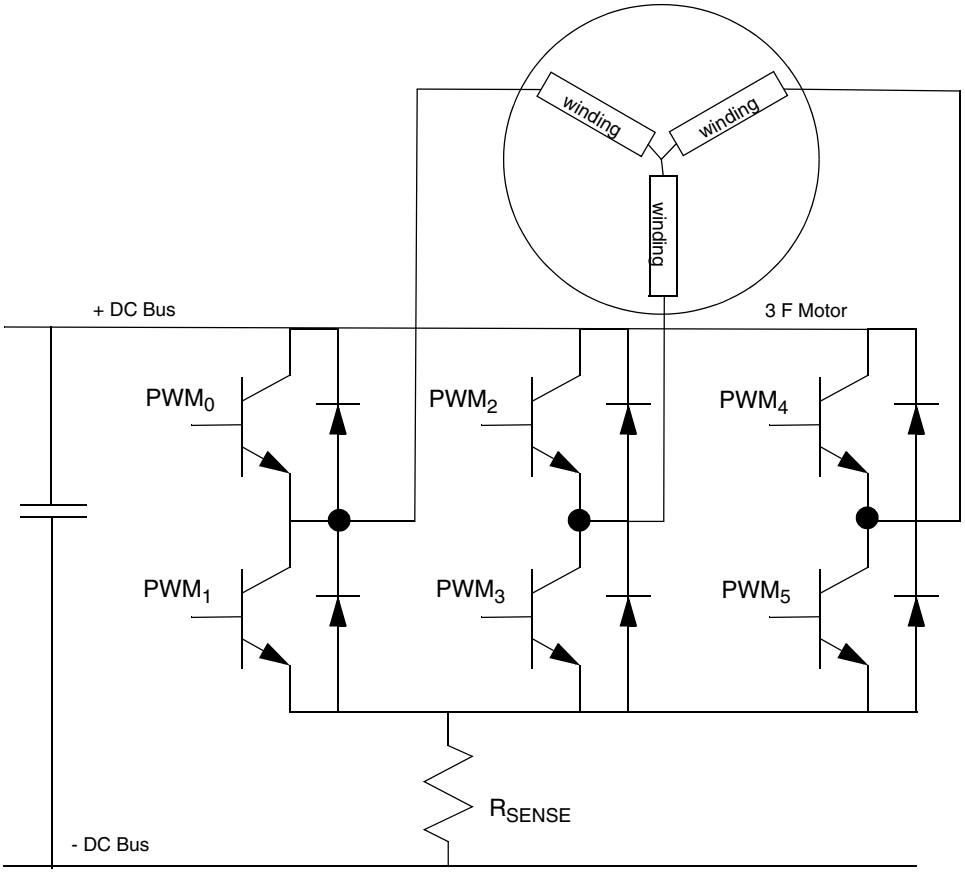

Figure 2. PWM/Shunt Resistor Connections for Three-Phase Motor

Figure 3 illustrates one PWM period for this scenario. The beginning of the period is identified via a PWM reload event, which triggers the programmable delay block (PDB) to begin counting. The PDB is configured in two-shot mode to time the phase A and phase C current measurements from the same trigger event.

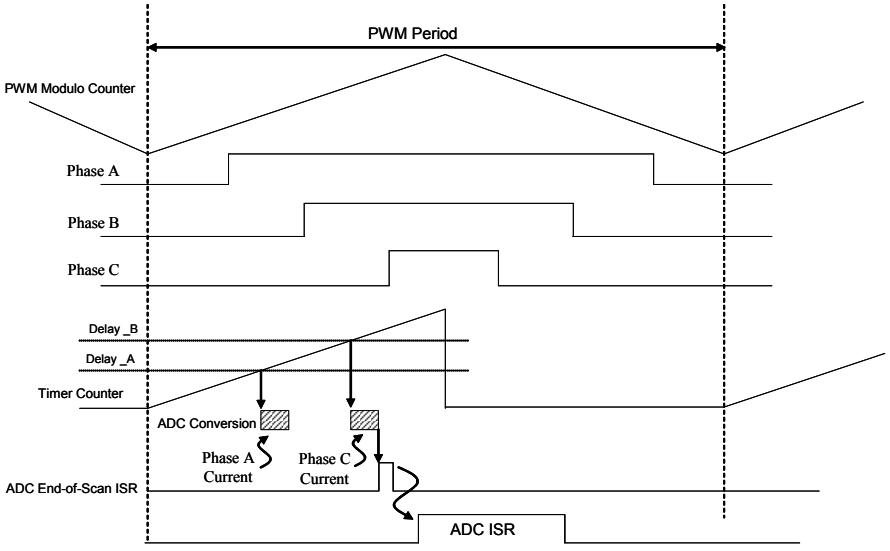

Figure 3. Current Reconstruction Timing Diagram

By precisely synchronizing the PWM and ADC sample point via PDB, the MC56F8006/MC56F8002 PGA/ADC accurately centers its sample in the PWM pulse shown in Figure 4.

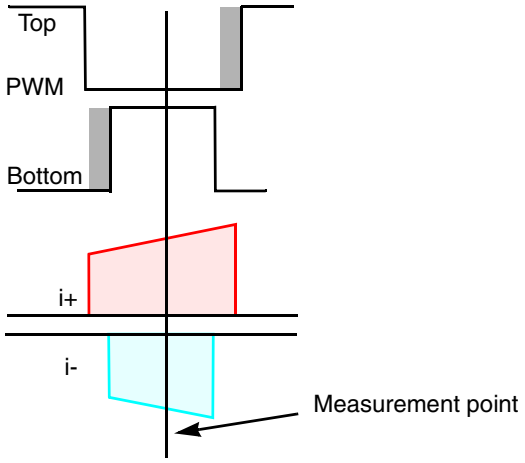

Figure 4. Motor Currents vs. PWM Signals and Measurement Window

1.2.3 Sensorless BLDC

Figure 5 illustrates the use of the comparator sampling mode for sensorless BLDC applications. In this application, comparators detect the zero-crossing of Back EMF generating in motor winding. To avoid false zero-crossing detection due to noise or changes of Back EMF reference, synchronize the PWM pulse and comparator output. In this case, the comparator can be programmed to send its output to the CPU when the comparator comparing window is opened, which is triggered by the PWM module.

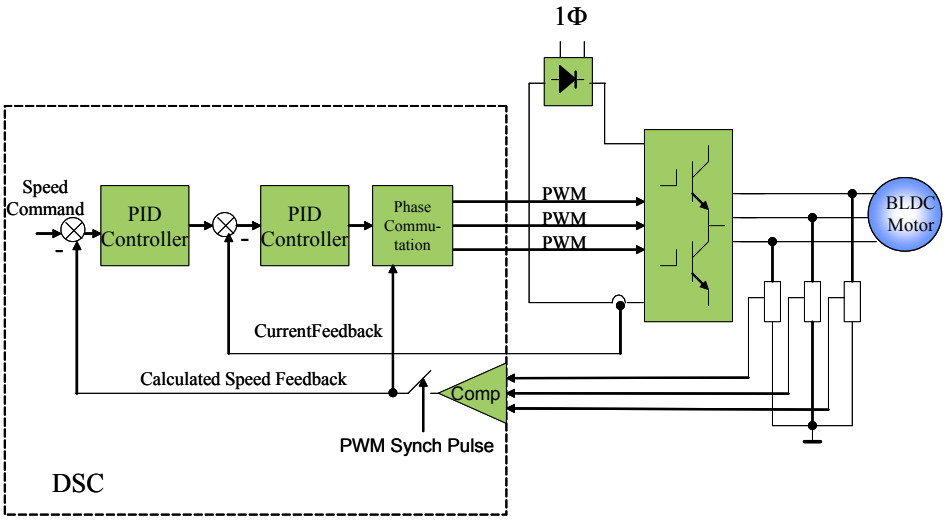

Figure 5. Use of Comparator Sampling Mode in a Sensorless BLDC Application

2 Block Diagram

Figure 6 shows a top-level block diagram for the MC56F8006/MC56F8002 series.

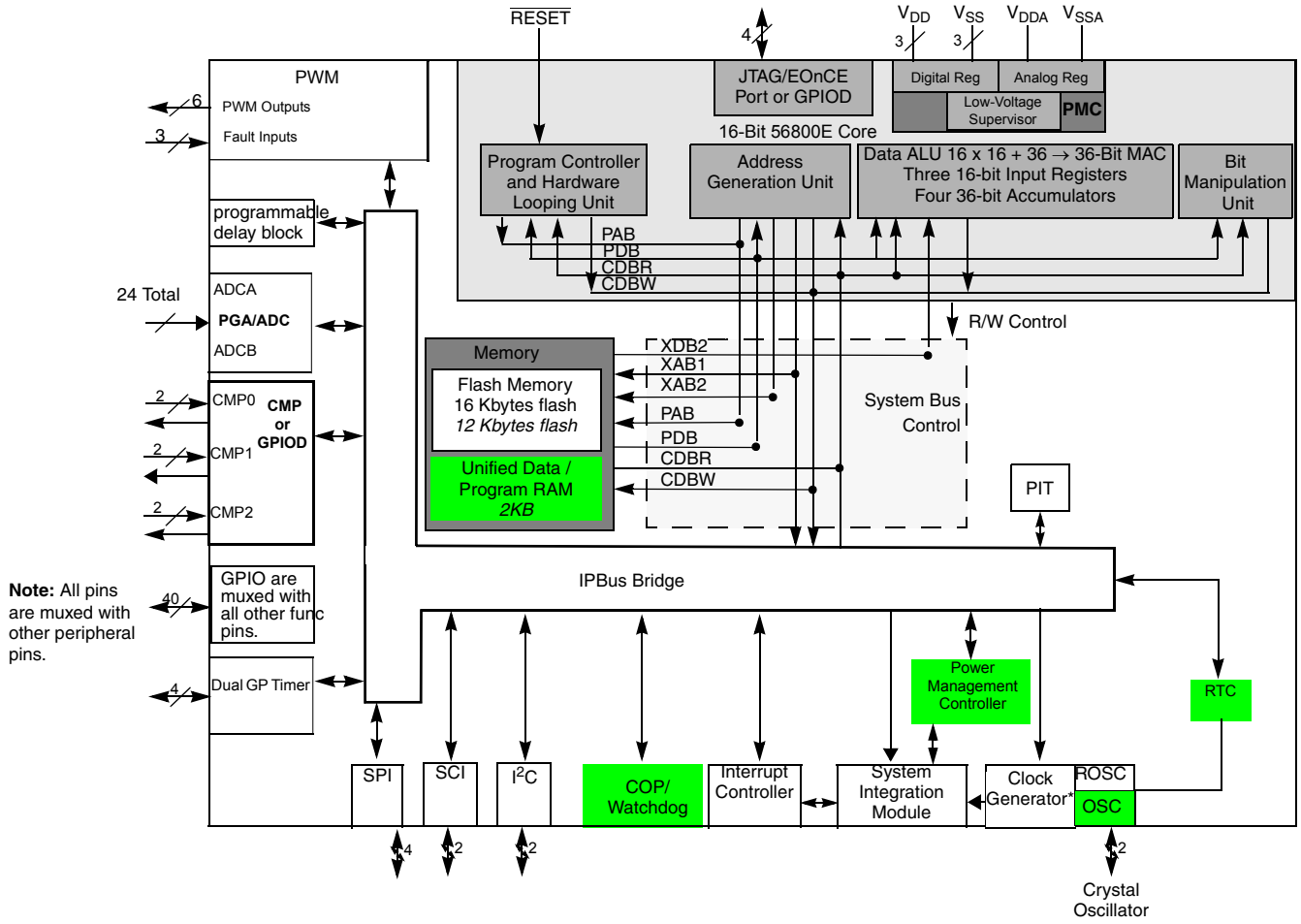

Figure 6. MC56F8006/MC56F8002 Top-Level Block Diagram

3 Device Comparison

Table 1. MC56F8006 Series Device Comparison

Feature	MC56F8006			MC56F8002
	28-pin	32-pin	48-pin	28-pin
Flash memory size (Kbytes)	16			12
RAM size (Kbytes)	2			
High-Speed comparators (HSCMP)	3	3	3	3
Analog-to-digital converters (ADC)	2			
Unshielded ADC inputs	6	7	7	6
Shielded ADC inputs	9	11	17	9
Total number of ADC input pins	15	18	24	15
Programmable gain amplifiers (PGA)	2			
Pulse-width modulator (PWM) outputs	6			
PWM fault inputs	3	4	4	3
Inter-integrated circuit (IIC)	1			
Serial peripheral interface (SPI)	1			
High-speed Serial communications interface (SCI)	1			
Programmable interrupt timer (PIT)	1			
Programmable delay block (PDB)	1			
16-bit Multi-purpose timers (TMR)	2			
Real-time counter (RTC)	1			
Computer operating properly (COP) timer	Yes			
Phase-locked loop (PLL)	Yes			
8 MHz (400 kHz at standby mode) on-chip Relaxation Oscillator (ROSC)	Yes			
1 kHz on-chip oscillator	Yes			
Crystal oscillator	Yes			
Power management controller (PMC)	Yes			
IEEE 1149.1 Joint Test Action Group (JTAG) interface	Yes			
Enhanced On-Chip Emulator (EOnCE)	Yes			

3.1 Features

3.2 High Performance Core

- Efficient 16-bit 56800E family Digital Signal Controller (DSC) engine with dual Harvard architecture

- Up to 32 Million Instructions Per Second (MIPS) at 32 MHz core frequency
- 155 Basic Instructions in conjunction with up to 20 address modes
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging

3.3 Operation Range

- From power-on-reset: Approximately 1.9 V to 3.6 V
- Operating: 1.8 V to 3.6 V (power supplies and input/output)
- Ambient temperature operating range: -40 °C to 105 °C

3.4 Memory Configuration

- Up to 16 Kbytes program flash memory with flash security protection
- 2 Kbytes unified program/data RAM

3.5 Module Configuration

- One 6-channel PWM module
  - — Up to 96 MHz PWM operating clock
  - — 15 bits of resolution
  - — Center-Aligned and edge-aligned PWM signal mode
  - — Four programmable fault inputs with programmable digital filter
  - — Double-Buffered PWM registers
- Dual 12-bit SAR analog-to-digital converters (ADC)
- 3.042 µSec for first ADC conversion, 2.125 µSec for subsequent
- Linear successive approximation algorithm with 12-bit resolution
- Up to 24 analog inputs
- Output formatted in 12-, 10-, or 8-bit right-justified unsigned format

- Single or continuous conversion (automatic return to idle after single conversion)
- Configurable sample time and conversion speed/power
- Conversion complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in wait or stop3 modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value
- Temperature sensor
- Two differential programmable gain amplifiers (PGA)
  - Sampled PGA architecture
  - Common mode noise and offset are automatically cancelled out (2–4 consecutive samples required for noise/offset cancellation)
  - Sample may be synchronized with PWM operation using the PWM sync output and programmable delay block
  - Sampling time can be precisely controlled (to less than 0.1 μs)
  - Several programmable gains (1×, 2×, 4×, 8×, 16×, and 32×)
  - 0.14 MSPS maximum
  - Selectable tradeoff for slower/low power versus faster/more power
  - Rail-to-rail input voltage range
  - Single-ended output routed directly to on-chip ADCs
- One high-speed serial communication interface (SCI) with LIN slave functionality
  - Max baud rate of 6 Mbps when using 3× IPBus at 96 MHz.
  - Full-duplex or single-wire operation
  - Two receiver wake-up methods:
    - Idle line
    - Address mark
- One serial peripheral interface (SPI)
  - Full-duplex operation
  - Master and slave modes
  - Programmable Length Transactions (2 to 16 bits)
- Dual 16-bit general-purpose timers (GPT)
  - Up to 96 MHz operating clock
  - Eight independent 16-bit counter/timers with cascading capability
  - Each timer has capture and compare capability
  - Up to 12 operating modes
- One programmable interval timer (PIT)
  - 16-bit counter/timer

  - Programmable count modulo
- Real-time counter (RTC) which can be used to implement a real-time clock
  - 8-Bit up-counter
  - Three software selectable clock sources for input to prescaler with selectable binary-based and decimal-Based divider values
    - 1 kHz internal oscillator
    - External clock
    - 32 kHz internal clock
- One programmable delay block (also known as a sync timer) for coordination of the ADC, PGA, or comparator samples with PWM
- One inter-integrated circuit (I^2C) port
  - Operates up to 400 kbps
  - Supports both master and slave operation
  - Supports both 10-bit address mode and broadcasting mode
  - System Management Bus Specification (SMBus) Version 2 support
- Computer operating properly (COP)/watchdog timer with independent 1 kHz on-chip oscillator
  - Integrated 1 KHz oscillator
  - Programmable timeout period
  - Programmable wait and stop and partial powerdown mode operation
  - Choice of clock sources for counter
  - Support for switched power modes
- Clock sources
  - On-chip 8 Mhz relaxation oscillator
  - On-chip 1 Khz clock
  - External clock (32 Khz or 8 Mhz): Crystal oscillator, ceramic resonator, and external clock source
- Integrated phase-locked loop (PLL)
- Three on-chip comparators
  - Selectable input source from external pins
  - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
  - Programmable output polarity
  - Comparator output may be:
    - Sampled
    - Windowed (ideal for certain PWM zero-crossing-detection applications)
    - Digitally Filtered
    - Filter can be bypassed
    - Clocked via external SAMPLE signal or scaled peripheral clock

- JTAG/Enhanced On-Chip Emulation (EOnCE™) for unobtrusive, real-time debugging
- Up to 40 general-purpose input/output (GPIO) lines
  - Programmable output drive level, slew-rate control, and optional input low-pass filters
  - Individual control for each pin to be in either Peripheral or GPIO mode
  - Individual Input/Output direction control for each pin in GPIO mode
  - Individual Pull-Up Enable Control for each input pin in either Peripheral or GPIO mode
  - 15 mA sink/source current

3.6 Power Management

- On-chip regulator for digital and analog circuitry to lower cost and reduce noise
- Integrated power-on reset
- Low-voltage interrupt with a user-selectable trip voltage of 1.86 or 2.33 V
- User selectable brown-out reset
- RUN, WAIT, and STOP modes
- Low-power RUN, WAIT, and STOP modes
- Partial Power Down mode
  - RAM, PMC, and COP remain powered
  - Rest of the chip is shut down for extreme power savings
- Each peripheral can be individually disabled to save power

4 Part Numbers

Table 2. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MC56F8006VLF	MC56F8006 DSC	16 / 2	48 LQFP	–40 °C to 105 °C
MC56F8006VLC	MC56F8006 DSC	16 / 2	32 LQFP	–40 °C to 105 °C
MC56F8006VWL	MC56F8006 DSC	16 / 2	28 SOIC	–40 °C to 105 °C
MC56F8002VWL	MC56F8002 DSC	12 / 2	28 SOIC	–40 °C to 105 °C

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