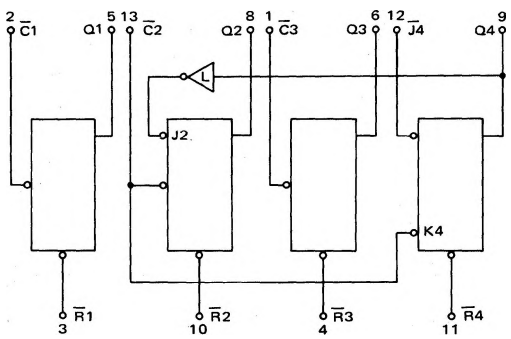
4-BIT UNIVERSAL COUNTER

MC4023F, L, P*

ADVANCE INFORMATION/NEW PRODUCT



V_{CC} = Pin 14
GND = Pin 7

Input Loading Factor:
J̄ = 1
C̄1, C̄3 = 2
C̄2, R̄ = 3

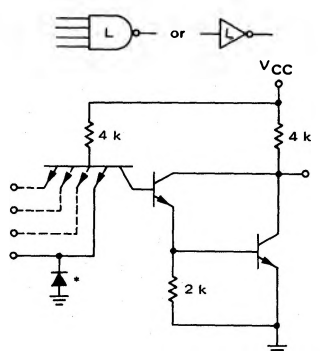
Output Loading Factor = 10

Total Power Dissipation = 200 mW typ/pkg
Propagation Delay Time = 16 ns typ/bit
Operating Frequency = 30 MHz typ

This device is a 4-bit counter with internally connected feedback. Inputs and outputs can be connected to count to any number between two and twelve except seven and eleven. Reset inputs are provided on each flip-flop to allow direct setting of the Q outputs to zero any time during the counting cycle.

Each flip-flop in the counter is built from high and low-level gates as shown by the logic diagram. The flip-flops and the feedback inverter are connected as shown by the block diagram to provide minimum power dissipation and maximum drive capability.

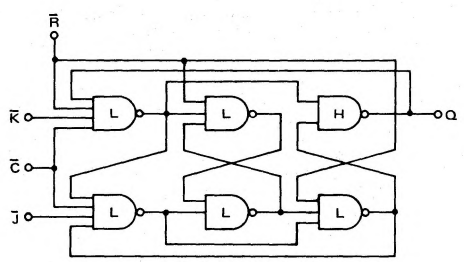
LOW-LEVEL GATE



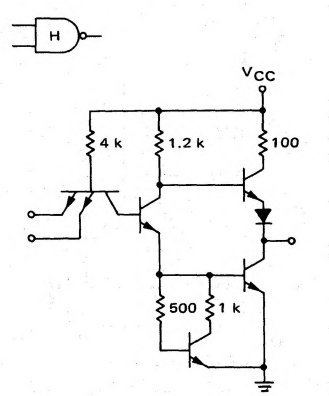
*Diode used only when input is connected to external point.

LOGIC DIAGRAM

One flip-flop shown. Only inputs shown on block diagram are present.



HIGH-LEVEL GATE



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

INPUT LOADING and OUTPUT DRIVING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4000 INPUT LOADING FACTOR	MC4000 OUTPUT DRIVE FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15**	12

Note: Differences in MC4000 series loading factors result from differences in specifications for each family

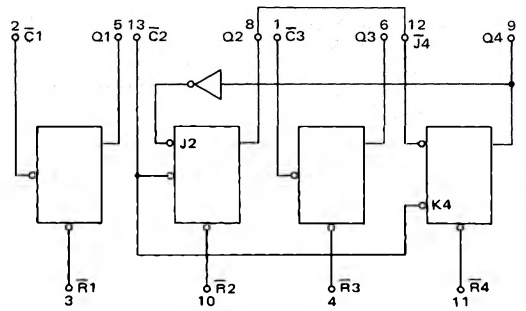
**Applies only when input is being driven by MDTL gate with 2.0 k ohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 k ohm pullup resistors reduce drive capability to fan-out of 3.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 75°C)

Characteristic	Symbol	Value	Conditions
Input			
Forward Current – J	I_{F1}	-1.6 mAdc max	
C1, C3		-3.2 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.25 Vdc
C2, R		-4.8 mAdc max	
J	I_{F2}	-1.4 mAdc max	
C1, C3		-2.8 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 4.75 Vdc
C2, R		-4.2 mAdc max	
Leakage Current – J	I_R	40 μAdc max	
C1, C3		80 μAdc max	V_{in} = 2.5 Vdc, V_{CC} = 5.25 Vdc
C2, R		120 μAdc max	
Breakdown Voltage	BV_{in}	5.5 Vdc max	I_{in} = 1.0 mAdc, V_{CC} = 5.25 Vdc, T_A = 25°C
Clamp Voltage	V_D	-1.5 Vdc max	I_D = -10 mAdc, V_{CC} = 4.75 Vdc, T_A = 25°C
Threshold Voltage	V_{th} "1"	2.0 Vdc	T_A = 0°C
		1.8 Vdc	T_A = +25°C, or T_A = 75°C
	V_{th} "0"	1.1 Vdc	T_A = 0°C, or T_A = +25°C
		0.9 Vdc	T_A = +75°C
Output			
Output Voltage	V_{OL}	0.4 Vdc max	I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
		0.4 Vdc max	I_{OL} = 17.6 mAdc, V_{CC} = 5.25 Vdc
	V_{OH}	2.5 Vdc max	I_{OH} = -1.6 mAdc, V_{CC} = 4.75 Vdc
Short-Circuit Current	I_{SC}	-20 to -65 mAdc	V_{out} = 0 Vdc, V_{CC} = 5.0 Vdc

COUNTING SEQUENCES



DIVIDE BY 3

C̄2	Q2	Q4
0	0	0
1	1	0
2	0	1

DIVIDE BY 4

C̄1	Q1	Q3
0	0	0
1	1	0
2	0	1
3	1	1

DIVIDE BY 6

C̄1	Q1	Q2	Q4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1

DIVIDE BY 12

C̄3	Q3	Q1	Q2	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1

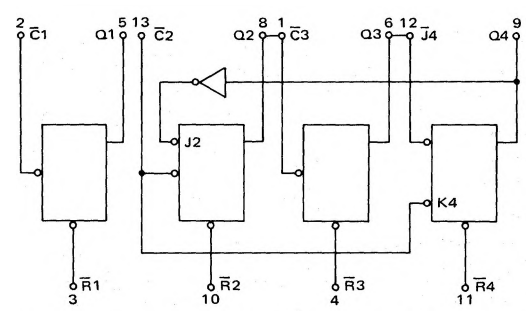
DIVIDE BY 2: Use flip-flop 1 or 3.

DIVIDE BY 3: Use flip-flops 2 and 4, connected as shown. The input signal is applied to C̄2; the output is taken from Q4.

DIVIDE BY 4: Use flip-flops 1 and 3; connect Q1 to C̄3. Apply the input signal to C̄1.

DIVIDE BY 6: In addition to the connection for divide by 3, connect Q1 to C̄2. Apply the input signal to C̄1.

DIVIDE BY 12: In addition to the connections for divide by 6, connect Q3 to C̄1. Apply the input signal to C̄3.



DIVIDE BY 5

C̄2	Q2	Q3	Q4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1

DIVIDE BY 8

C̄1	Q1	Q2	Q3
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

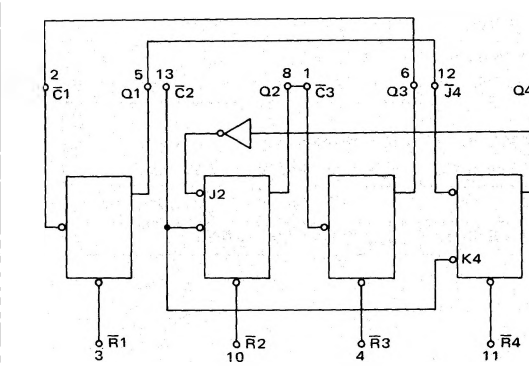
DIVIDE BY 10

C̄1	Q1	Q2	Q3	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

DIVIDE BY 5: Connect flip-flops 2, 3, and 4 as shown. The input signal is applied to C̄2; the output is taken from Q4.

DIVIDE BY 8: Connect flip-flops 2 and 3 as shown for divide by 5, but do not connect Q3 to J̄4. Connect Q1 to C̄2. The input signal is applied to C̄1; the output is taken from Q3.

DIVIDE BY 10: In addition to the connections for divide by 5, connect Q1 to C̄2. Apply the input signal to C̄1.



DIVIDE BY 9

C̄2	Q2	Q3	Q1	Q4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1

DIVIDE BY 9: The input signal is applied to C̄2; the output is taken from Q4.