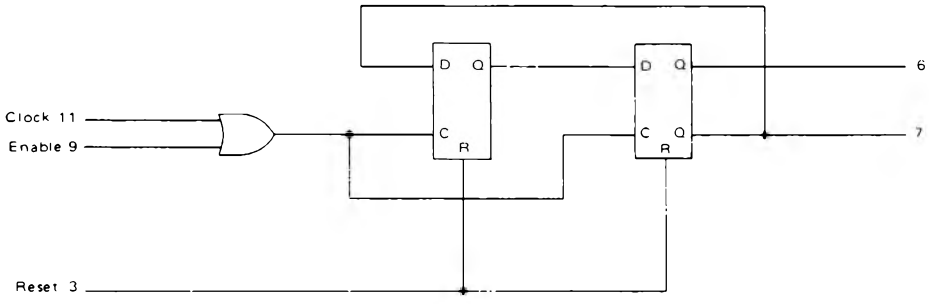
Divide-by-four Gigahertz Counter

The MC1699 is a divide-by-four gigahertz counter. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage.

The MC1699 includes clock enable and reset, which are both compatible with MECL III voltage levels. Reset operates only when either the clock or the enable is high.

Pin 13 is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.



f_{Tog} = 1.6 MHz typ
P_D = 320 mW Typ/Pkz
(No load −7.0 V supply)

V_{CC1} = Pin 4
V_{CC2} = Pin 5
V_{EE} = Pin 12
Bias Point = Pin 13