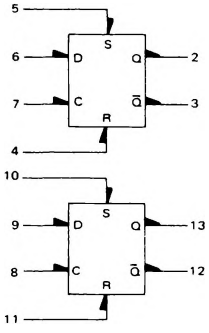

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	ϕ	ϕ	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	**
ϕ	ϕ	0	1	0
ϕ	ϕ	1	1	1

**Output state not defined ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)

Dual Clocked Latch

This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the data (D) input.