Freescale Semiconductor
Chip Errata

Document Number: MC13783CE
Rev. 4, 10/2011

MC13783

Power and Audio Management IC

This chip errata document applies to the MC13783 power management IC. Table 1 defines severity values for errata. Table 2 provides the known chip errata affecting the MC13783. Table 3, on page 3 summarizes the silicon waiver information.

Table 1. Definitions of Errata Severity

Severity	Errata Type	Meaning	Workaround
1	Critical	Failure mode that severely inhibits the use of the device for all or a majority of intended applications	Unavailable
2	High	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications	Generally available
3	Moderate	Unexpected behavior that does not cause significant problems for the intended applications of the device	Generally available

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Table 2. Chip Errata for MC13783

Severity	Erratum ID	Summary	Details
3	TLSbo92223	**Module Affected:** ADC **Title:** MC13783 ADC dual-SPI reading errors. ADA selection issue in dual SPI.	**Description:** Internal ADA selector is controlled by the SPI owner of last conversion. The address ports are controlled by the most recent SPI to begin a conversion. So if one SPI begins a conversion before the other SPI has read out, then the previous conversion results from the first set of results will be corrupted. Root cause identified. **Workaround:** A handshaking method using semaphore is one potential solution for workaround.
2	TLSbo92778	**Module Affected:** Control/SPI **Title:** MC13783 locked in power cut mode conditions.	**Description:** When the BP is between UVDET and BPON, Li cell is present and not empty. Power cut issue produces strange effects for turn on events: 1) Sometimes it delays the turn on of the charger insertion. 2) Sometimes it delays the M3 turn on upon battery insertion (B+ does not get voltage immediately). 3) Sometimes it prevents the MC13783 turn on by enabling a power supply when connected to the battery terminals. Root cause identified: • In power cut, user off and memory hold modes, the AC references are off ≥ BP regulator cannot turn on correctly. • During extended power cut, the MEMTMR and PCT stop counts when the BP is between UVDET and BPON. **Workaround:** Disable power cut mode (by setting PCEN = 0) when BP is below BPON.
2	TLSbo94499	**Module Affected:** Connectivity/USB Interface **Title:** USB crossover voltage could be degraded when USBVCC is connected to 1.8 V.	**Description:** The USB crossover voltage could be degraded when the USBVCC is connected to 1.8 V. Conditions: USBVCC set to 1.8 V. **Fix Plan/Status:** • Supply to the USBVCC with 2.775 V.

Table 3. Silicon Waivers to the MC13783

Severity	Erratum ID	Summary	Details
3	–	**Title:** Vvib load regulation exceeds the ±3% accuracy.	**Description:** When the regulator is loaded with full load, the output voltage is not in the ±3% range. The regulator drop is below the -3%. Output voltage accuracy relaxes from ±3% to: • For 1.3 V set point 1.23 V min. - 1.34 V max. • For 1.8 V set point 1.72 V min. - 1.85 V max. • For 2.0 V set point 1.91 V min. - 2.06 V max. • For 3.0 V set point 2.88 V min. - 3.09 V max.
3	–	**Module Affected:** Audio **Title:** Audio SPI Issue	**Description:** Depending on SPI clock speed and main audio clock (CLI) speed, sometimes the Audio Codec or the Stereo DAC does not start when it is programmed to do so. This is due to an internal clock timing issue related to the loading of audio converter SPI bits into the audio block. **Workaround:** • When using Audio Codec: do a second SPI write access to register 40 (Audio Codec) directly after the original write to register 40 with the exact same content. • When using Stereo DAC: do a second SPI write access to register 41 (STDAC) directly after the original write to register 41 with the exact same content.
3	–	**Module Affected:** Charger **Title:** Charger Separate Input, Dual Path configuration should not be used	**Description:** The Separate Input, Dual Path charger configuration should not be used as you may experience an oscillation issue when battery voltages are slightly above the CHGDETSEP threshold of 3.8V maximum and the charger is disconnected. Also, the CHRGRAW voltage must be greater than ~4.6V before the charger current can be programmed in this configuration. **Workaround:** Use Common Input, Dual Path Charger configuration instead.
3	–	**Module Affected:** Charger **Title:** Charger detection threshold in separate input dual path mode	**Description:** When in separate input charging configuration, detection of charger removal is based on CHGDETSEP and CHGCURR thresholds. • Rising detection threshold for CHGDETSEP is 3.8V max whereas it is specified at 4.65V max in the MC13783 User Guide. • Falling detection threshold for CHGDETSEP is 3.6V max whereas it is specified at 4.4V max in the MC13783 User Guide.
3	–	**Module Affected:** Charger **Title:** Standalone Trickle unavailable for Single path mode and SE1 = High	**Description:** When in single path charger configuration (CHRGMOD0 = OPEN), and SE1 signal is HIGH, standalone trickle mode is not available. Feature has been removed from IC. **Workaround:** SE1 signal should be set low in single path charger mode for standalone trickle charging to be operational.

Revision History

Table 4 summarizes revisions to this document since the release of the previous version (Rev. 3.3).

Table 4. Revision History

Location	Revision
Table 3, third row from bottom	**Added Silicon Waiver item titled:** Charger Separate Input, Dual Path configuration should not be used.
Table 3, second row from bottom	**Changed Silicon Waiver item titled:** Charger detection threshold in separate input dual path mode. Changed CHRGDETSEP to CHGDETSEP.

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