



CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	L	0
H	H	H

0 = Don't Care

C = $\overline{C_E} \cdot C_C$

A clock H is a clock transition from a low to a high state.

RS TRUTH TABLE

R	S	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

X = Not Defined

V_{CC1} = Pin 1

V_{CC2} = Pin 16

V_{EE} = Pin 8

P_D = 270 mW typ/pkg (No Load)

f_{Tog} = 225 MHz typ

High Speed Dual Type D Master-Slave Flip-Flop

The MC10231 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C_E}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pull-down resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times allow high frequency operation over 200 MHz.

MC10231

FLIP-FLOPS