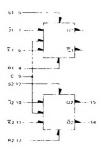
MC10135 FLIP-FLOPS

A-S TRUTH TABLE

N.D. Not Defined

0...



CLOCK J.K TRUTH TABLE

J	K	Qn. 1
t.		Q,
24	L	i i
L	н	+1
н :	-4	20

tive transition of clack to ... K input condition present

V<sub>CC1</sub> = Pin 1 V<sub>CC2</sub> = Pin 16 V<sub>FF</sub> = Pin 8

P<sub>D</sub> - 280 mW typ/pkg (No Load) f<sub>Tog</sub> = 140 MHz typ

## Dual J-K Master-Slave Flip-Flop

The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs overide the clock.

A common clock is provided with separate  $J\text{-}\overline{K}$  inputs. When the clock is static, the  $J\text{-}\overline{K}$  inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

Input pulldown resistors eliminate the need to tie unused inputs to  $V_{\text{EE}}$ . Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.