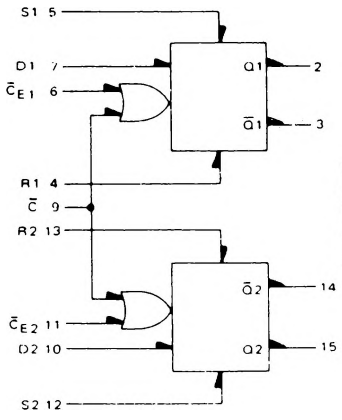

TRUTH TABLE

D	$\overline{C}$	$\overline{C}E$	Q_{n+1}
L	L	L	L
H	L	L	H
Φ	L	H	Q_n
Φ	H	L	Q_n
Φ	H	H	Q_n

Φ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 155 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

Dual Latch

The MC10130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

Output rise and fall times have been optimized to provide relaxation of system layout and design criteria.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{C}E$ or both are high.