5V Differential PECL to TTL Translator

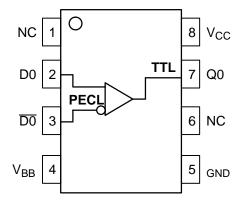
The MC10ELT/100ELT21 is a differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the single gate of the ELT21 makes it ideal for those applications where space, performance and low power are at a premium.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Output
- Flow Through Pinouts
- ESD Protection: >2 KV HBM
- Operating Range: V_{CC}= 4.75 V to 5.25 V with GND= 0 V
- Q Output Will Default High with Inputs Left Open or < 1.3 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
 For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 81 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q0 D0, D0 V _{BB} V _{CC} GND NC	TTL Output PECL Differential Inputs Reference Voltage Output Positive Supply Ground No Connect



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MARKING DIAGRAMS*



SO-8 D SUFFIX CASE 751



8 F F F F KLT21 ALYW



TSSOP-8 DT SUFFIX CASE 948R



 $\begin{array}{ll} H = MC10 & L = Wafer Lot \\ K = MC100 & Y = Year \\ A = Assembly Location & W = Work Week \end{array}$

ORDERING INFORMATION

Device	Package	Shipping						
MC10ELT21D	SO-8	98 Units/Rail						
MC10ELT21DR2	SO-8	2500 Tape & Reel						
MC100ELT21D	SO-8	98 Units/Rail						
MC100ELT21DR2	SO-8	2500 Tape & Reel						
MC10ELT21DT	TSSOP-8	98 Units/Rail						
MC10ELT21DTR2	TSSOP-8	2500 Tape & Reel						
MC100ELT21DT	TSSOP-8	98 Units/Rail						
MC100ELT21DTR2	TSSOP-8	2500 Tape & Reel						

^{*}For additional information, see Application Note AND8002/D

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Power Supply	GND = 0 V		7	V
V _{IN}	PECL Input Voltage	GND = 0 V	$V_1 \leq V_{CC}$	0 to 6	٧
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
$\theta_{\sf JA}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W
θJC	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

^{1.} Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES PECL INPUT DC CHARACTERISTICS V_{CC} = 5.0 V; GND= 0.0 V (Note 1.)

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V _{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3930		4265	mV
V _{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	2.2		5.0	2.2		5.0	2.2		5.0	٧
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.3			μΑ

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

100ELT SERIES PECL INPUT DC CHARACTERISTICS V_{CC} = 5.0 V; GND= 0.0 V (Note 1.)

			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V _{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V _{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V _{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.745	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	2.2		5.0	2.2		5.0	2.2		5.0	V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

^{1.} Input parameters vary 1:1 with V_{CC}. V_{CC} can vary \pm 0.25 V. 2. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

^{1.} Input parameters vary 1:1 with $V_{CC}.\ V_{CC}$ can vary \pm 0.25 V.

^{2.} V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC} .

TTL OUTPUT DC CHARACTERISTICS V_{CC}= 4.75 V to 5.25 V; T_A= -40° C to 85° C)

Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V _{OH}	Output HIGH Voltage	$I_{OH} = -3.0 \text{mA}$	2.4		(Note 1.)	V
V _{OL}	Output LOW Voltage	I _{OL} = 24mA			0.5	V
I _{CCH}	Power Supply Current			20	29	mA
I _{CCL}	Power Supply Current			22	32	mA
Ios	Output Short Circuit Current		-150		-60	mA

^{1.} Max level is V_{CC}-0.7 by design.

AC CHARACTERISTICS $\rm V_{CC^{=}}~4.75~V$ to $\rm 5.25~V;~GND=0.0~V$

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Toggle Frequency		TBD			100			TBD		MHz
t _{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t _{PLH}	Propagation Delay @ 1.5 V C _L = 20pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
t _{PHL}	Propagation Delay @ 1.5 V C _L = 20pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
V_{PP}	Input Swing (Note 1.)	200		1000	200		1000	200		1000	mV
t _r /t _f	Output Rise/Fall Time C _L = 20pF (10–90%)					750					ps

^{1.} V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

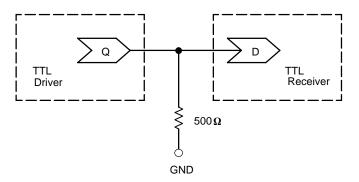


Figure 1. TTL Output Termination

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 - ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire-OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

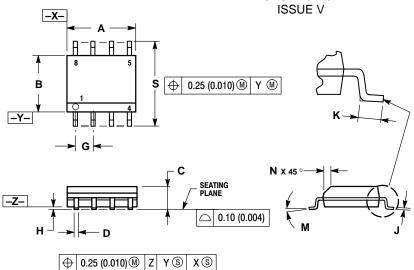
AND8001 - Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 - Termination of ECL Logic Devices

PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07

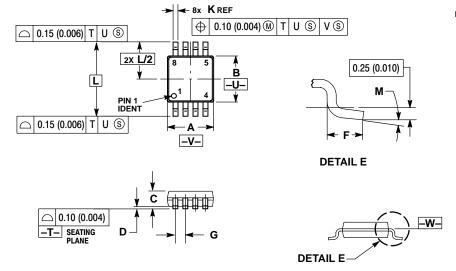


NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
Α	4.80	5.00	0.189	0.197		
В	3.80	4.00	0.150	0.157		
С	1.35	1.35 1.75		0.069		
D	0.33	0.51	0.013	0.020		
G	1.27	7 BSC	0.050 BSC			
Н	0.10	0.25	0.004	0.010		
J	0.19	0.25	0.007	0.010		
K	0.40	1.27	0.016	0.050		
M	0 ° 8		0 °	8 °		
N	0.25	0.50	0.010	0.020		
S	5.80	6.20	0.228	0.244		

TSSOP-8 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948R-02 **ISSUE A**



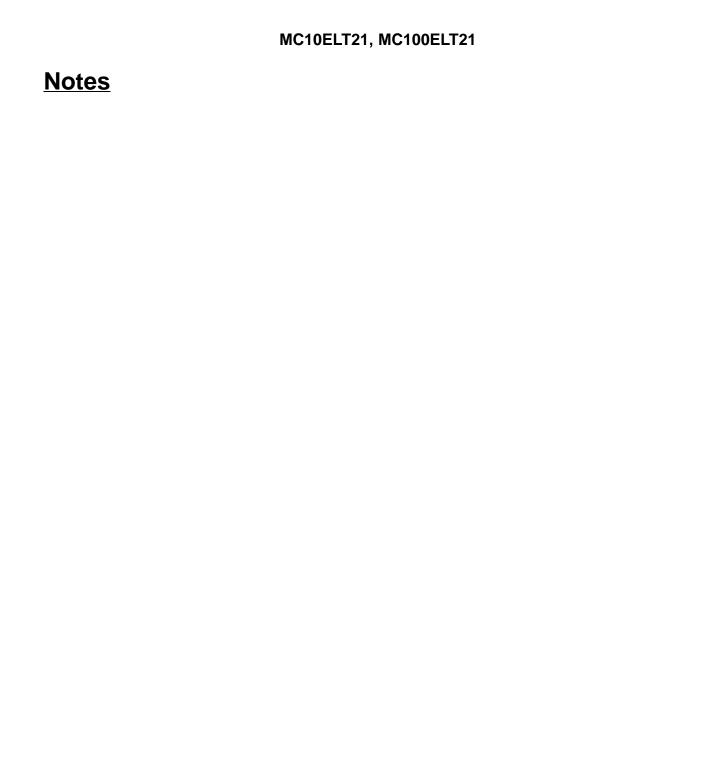
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- Y14.5M, 1982.

 CONTROLLING DIMENSION: MILLIMETER.

 DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 0.13 (0.00) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL NOT
 EXCEED 0.25 (0.010) PER SIDE.
- 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE
 DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES				
DIM	MIN	MAX	MIN	MAX			
Α	2.90	3.10	0.114	0.122			
В	2.90	3.10	0.114	0.122			
С	0.80	1.10	0.031	0.043			
D	0.05	0.15	0.002	0.006			
F	0.40	0.70	0.016	0.028			
G	0.65	BSC	0.026	BSC			
K	0.25	0.40	0.010	0.016			
L	4.90	4.90 BSC		BSC			
M	0°	6 °	0°	6°			





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