MC100EL17

5V ECL Quad Differential Receiver

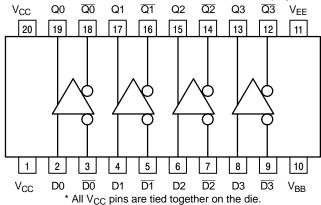
The MC100EL17 is a low-voltage, quad differential receiver. The device is functionally equivalent to the E116 device

Under open input conditions, the \overline{D} input will be biased at $V_{CC}/2$ and the D input will be pulled down to V_{EE} . This operation will force the Q output LOW and ensure stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 325 ps Propagation Delay
- ESD Protection: > 2 KV HBM, > 100 V MM
- The 100 series contains temperature compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -4.2 V to -5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
 For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 141 devices

LOGIC DIAGRAM AND PINOUT: 20-LEAD SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

T IN DESCRIPTION								
Pins	Function							
Dn, D n	ECL Differential Data Inputs							
Qn, Qn	ECL Differential Data Outputs							
V_{BB}	Reference Voltage Output							
V _{CC}	Positive Supply							
V _{EE}	Negative Supply							



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MARKING
DIAGRAM
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MC100EL17
AWLYYWW

SO-20 DW SUFFIX CASE 751D

A = Assembly Location

WL = Wafer Lot

YY = Year

WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL17DW	SO-20	38 Units/Rail
MC100EL17DWR2	SO-20	1000 Units/Reel

MC100FI 17

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0 V$		-8	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	$ \begin{array}{c} V_I \! \leq \! V_{CC} \\ V_I \! \geq \! V_{EE} \end{array} $	6 -6	V
l _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

^{1.} Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		26	31		26	31		27	33	mA
V _{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V _{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V _{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V _{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V _{IHCMR}	Common Mode Range (Differential) (Note 3.) $ \begin{array}{c} V_{PP} < 500 \text{ mV} \\ V_{PP} \geq 500 \text{ mV} \end{array} $	1.3 1.5		4.6 4.6	1.2 1.4		4.6 4.6	1.2 1.4		4.6 4.6	V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The

- circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

 1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / -0.5 V.

 2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.

 3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = -5.0 V (Note 1.)

		-40°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current		26	31		26	31		27	33	mA
V _{OH}	Output HIGH Voltage (Note 2.)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 2.)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V _{IH}	Input HIGH Voltage (Single Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V _{IL}	Input LOW Voltage (Single Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V _{IHCMR}	Common Mode Range (Differential) (Note 3.) $ V_{PP} < 500 \text{ mV} $ $ V_{PP} \geq 500 \text{ mV} $	-3.7 -3.5		-0.4 -0.4	-3.8 -3.6		-0.4 -0.4	-3.8 -3.6		-0.4 -0.4	V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current	0.5			0.5			0.5			μΑ

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

- 1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / -0.5 V. 2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.
- V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = -5.0 V (Note 1.)

			-40°C 25°C								
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t _{PLH} t _{PHL}	Propagation Delay Diff D to Q S.E.	330 280		530 580	350 300		550 600	360 310		560 610	ps
t _{SKEW}	Skew Output-to-Output (Note 2.) Part-to-Part (Diff) (Note 2.) Duty Cycle (Diff) (Note 3.)			75 200 25			75 200 25			75 200 25	ps
t _{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

- 1. V_{EE} can vary +0.8 V / -0.5 V.
- 2. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
- 3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
- V_{PP(}min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

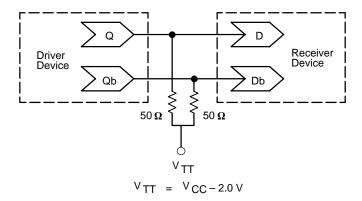


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 - ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire-OR Ties in ECLinPS Designs

AN1672 - The ECL Translator Guide

AND8001 - Odd Number Counters Design

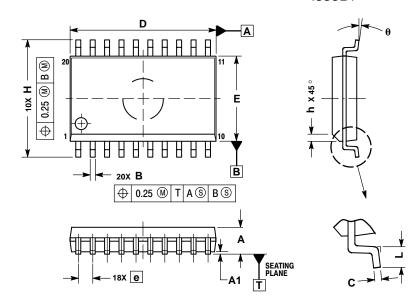
AND8002 – Marking and Date Codes

AND8020 - Termination of ECL Logic Devices

MC100EL17

PACKAGE DIMENSIONS

SOIC-20 **DW SUFFIX** PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



NOTES

- DIMENSIONS ARE IN MILLIMETERS. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0 15 PER SIDE
- DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS								
DIM	MIN	MAX							
Α	2.35	2.65							
A1	0.10	0.25							
В	0.35	0.49							
С	0.23	0.32							
D	12.65	12.95							
Е	7.40	7.60							
е	1.27	BSC							
Н	10.05	10.55							
h	0.25	0.75							
L	0.50	0.90							
θ	0 °	7°							

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