19-1082; Rev 0; 6/96

MAXIM

+5V, Serial-Input, Voltage-Output 16-Bit DAC

General Description

The MAX542 16-bit, serial-input, voltage-output, digital-to-analog converter (DAC) operates from a single +5V supply. It provides 16-bit performance (±1LSB INL and DNL) and a maximum offset error of 2LSBs over temperature without any adjustments. Kelvin-sense connections for the reference and analog ground pins improve the device's performance. The DAC output is unbuffered, resulting in a low, 0.3mA supply current.

The MAX542 allows unipolar or bipolar operation. For bipolar operation, internal scaling resistors are provided for use with an external precision op amp (such as the MAX400). These resistors are matched to provide a $\pm V_{REF}$ output swing at the external amplifier output in bipolar mode.

A 16-bit serial word loads data into the DAC latch. The 6.25MHz, 3-wire serial interface is compatible with SPI™/QSPI™ and Microwire™, and it also interfaces directly with optocouplers for applications that need isolation. A power-on reset circuit clears the DAC output to 0V (unipolar mode) when power is initially applied.

The 16-bit MAX542 is available in a small 14-pin DIP or SO package.

Applications

High-Resolution Offset and Gain Adjustment

Industrial Process Control

Automated Test Equipment

Data Acquisition Systems

Features

- **Full 16-Bit Performance Without Adjustments**
- **+5V Single-Supply Operation**
- **Low Power: 1.5mW**
- **1µs Settling Time**
- **Unbuffered Voltage Output Directly Drives 60kΩ Loads**
- **SPI/QSPI/Microwire-Compatible Serial Interface**
- **Power-On Reset Circuit Clears DAC Output to 0V (unipolar mode)**
- **Schmitt Trigger Inputs for Direct Optocoupler Interface**

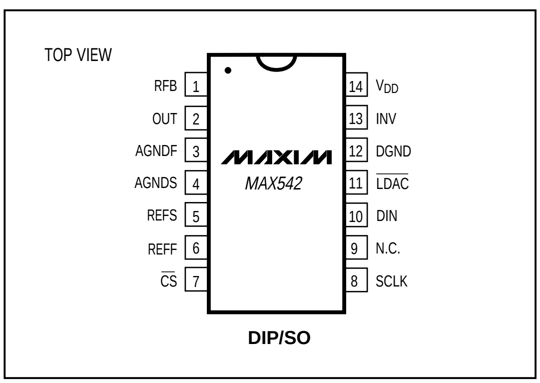
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX542ACPD	0°C to +70°C	14 Plastic DIP	±1
MAX542BCPD	0°C to +70°C	14 Plastic DIP	±2
MAX542CCPD	0°C to +70°C	14 Plastic DIP	±4
MAX542ACSD	0°C to +70°C	14 SO	±1
MAX542BCSD	0°C to +70°C	14 SO	±2
MAX542CCSD	0°C to +70°C	14 SO	±4
MAX542BC/D	0°C to +70°C	Dice*	±2

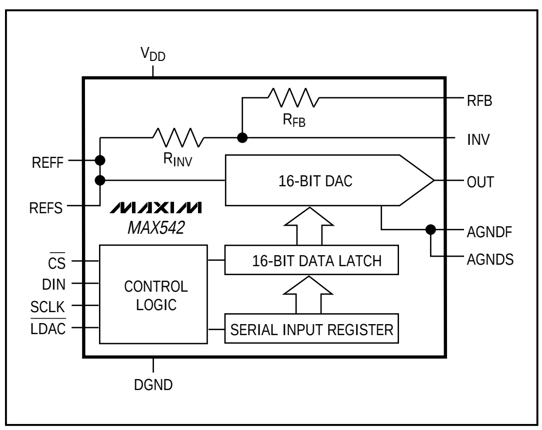
Ordering Information continued at end of data sheet.

** Dice are tested at T_A = +25°C only.*

Pin Configuration



Functional Diagram



SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

+5V, Serial-Input, Voltage-Output 16-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ....-0.3V to +6V
$\overline{CS}$, SCLK, DIN, $\overline{LDAC}$ to DGND ....-0.3V to +6V
REFF, REFS to AGND_ ....-0.3V, V_{DD} +0.3V
AGNDF, AGNDS to DGND ....-0.3V to +0.3V
OUT, INV to AGNDF, AGNDS, DGND......................-0.3V to V_{DD}
RFB to AGNDF, AGNDS, DGND ....-6V to +6V
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.33mW/°C above +70°C).........................667mW
Maximum Current into Any Pin...50mA
Operating Temperature Ranges
MAX542_C_D...0°C to +70°C
MAX542_E_D..-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, $V_{REF\_}$ = 2.5V, AGNDF = AGNDS = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION (R_L = ∞)							
Resolution	N			16			Bits
Integral Nonlinearity	INL	V_{DD} = 5V	MAX542A		±0.5	±1.0	LSB
			MAX542B		±0.5	±2.0	
			MAX542C		±0.5	±4.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±0.5	±1.0	LSB
Zero-Code Offset Error	ZSE	T_A = +25°C				±1	LSB
		T_A = T_{MIN} to T_{MAX}				±2	
Zero-Code Tempco	ZS_{TC}	T_A = T_{MIN} to T_{MAX}			±0.05		ppm/°C
Gain Error (Note 1)		T_A = +25°C				±5	LSB
		T_A = T_{MIN} to T_{MAX}				±10	
Gain-Error Tempco					±0.1		ppm/°C
DAC Output Resistance	R_{OUT}	(Note 2)			6.25		kΩ
Bipolar Resistor Matching		R_{FB}/R_{INV}			1.0		%
		Ratio error				±0.015	
Bipolar Zero Offset Error		T_A = +25°C				±10	LSB
		T_A = T_{MIN} to T_{MAX}				±20	
Bipolar Zero Tempco	BZS_{TC}				±0.5		ppm/°C
Power-Supply Rejection	PSR	4.75V ≤ V_{DD} ≤ 5.25V				±1.0	LSB
REFERENCE INPUT							
Reference Input Range	V_{REF}	(Note 3)		2.0		3.0	V
Reference Input Resistance (Note 4)	R_{REF}	Unipolar Mode		11.5			kΩ
		Bipolar Mode		9.0			
DYNAMIC PERFORMANCE—ANALOG SECTION (R_L = ∞, unipolar mode)							
Voltage-Output Slew Rate	SR	C_L = 10pF (Note 5)			25		V/µs
Output Settling Time		to ±$^1/_2$LSB of FS			1		µs
DAC Glitch Impulse		Major-carry transition			10		nV-s
Digital Feedthrough		Code = 0000H; $\overline{CS}$ = V_{DD}; $\overline{LDAC}$ = 0V; SCLK, DIN = 0V to V_{DD} levels			10		nV-s

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, $V_{REF\_}$ = 2.5V, AGNDF = AGNDS = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE—REFERENCE SECTION						
Reference -3dB Bandwidth	BW	Code = FFFF hex		1		MHz
Reference Feedthrough		Code = 0000 hex, V_{REF} = 1Vp-p at 100kHz		1		mVp-p
Signal-to-Noise Ratio	SNR			92		dB
Reference Input Capacitance	C_{IN}	Code = 0000 hex		75		pF
		Code = FFFF hex		120		
STATIC PERFORMANCE—DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	V_{IN} = 0V			±1	µA
Input Capacitance	C_{IN}	(Note 6)			10	pF
Hysteresis Voltage	V_H			0.40		V
POWER SUPPLY						
Positive Supply Range	V_{DD}		4.75		5.25	V
Positive Supply Current	I_{DD}			0.3	1.1	mA
Power Dissipation	PD			1.5		mW

TIMING CHARACTERISTICS

(V_{DD} = +5V ±5%, $V_{REF\_}$ = 2.5V, AGNDF = AGNDS = DGND = 0V, CMOS inputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

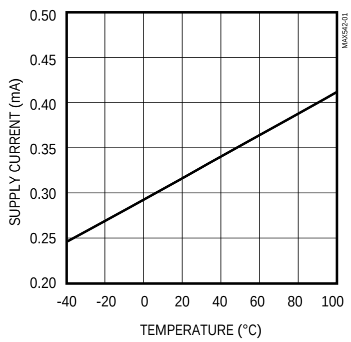
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{CLK}				6.25	MHz
SCLK Pulse Width High	t_{CH}		80			ns
SCLK Pulse Width Low	t_{CL}		80			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		50			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		50			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}	(Note 6)	30			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		80			ns
DIN to SCLK High Setup	t_{DS}		40			ns
DIN to SCLK High Hold	t_{DH}		0			ns
$\overline{LDAC}$ Pulse Width	$t_{\overline{LDAC}}$		50			ns
$\overline{CS}$ High to $\overline{LDAC}$ Low Setup	t_{LDACS}	(Note 6)	50			ns
V_{DD} High to $\overline{CS}$ Low (power-up delay)				20		µs

Note 1: Gain Error tested at V_{REF} = 2.0V, 2.5V, and 3.0V.
Note 2: R_{OUT} tolerance is typically ±20%.
Note 3: Min/max range guaranteed by gain-error test. Operation outside min/max limits will result in degraded performance.
Note 4: Reference input resistance is code dependent, minimum at 8555 hex.
Note 5: Slew-rate value is measured from 0% to 63%.
Note 6: Guaranteed by design. Not production tested.

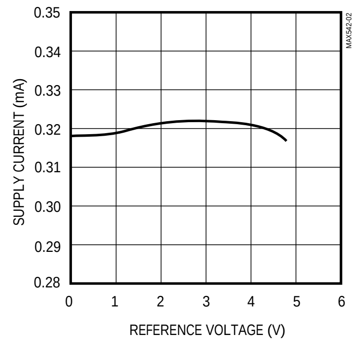
Typical Operating Characteristics

(V_{DD} = 5V ±5%, V_{REF} = 2.5V, T_A = +25°C, unless otherwise noted.)

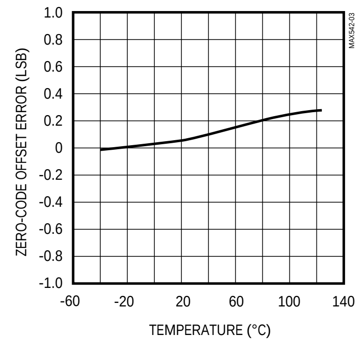
SUPPLY CURRENT vs. TEMPERATURE



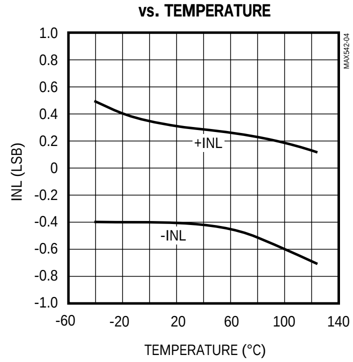
SUPPLY CURRENT vs. REFERENCE VOLTAGE



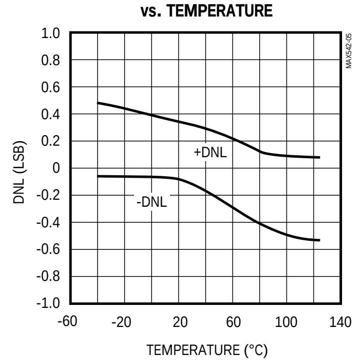
ZERO-CODE OFFSET ERROR vs. TEMPERATURE



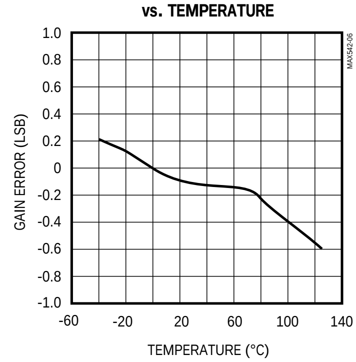
INTEGRAL NONLINEARITY vs. TEMPERATURE



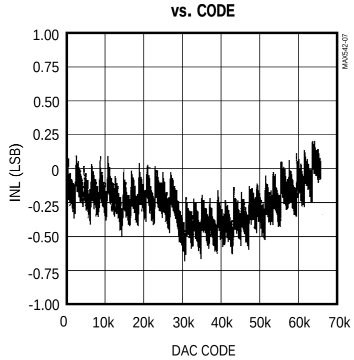
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



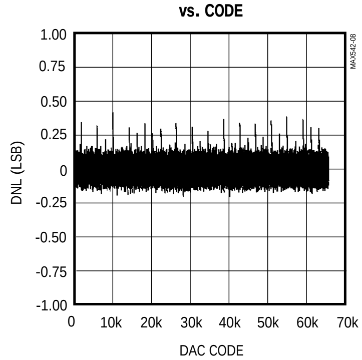
GAIN ERROR vs. TEMPERATURE



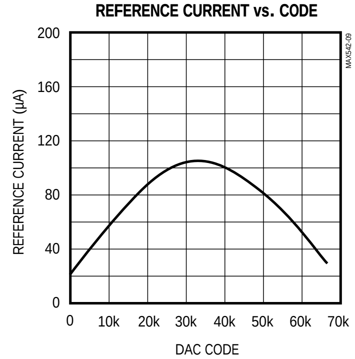
INTEGRAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. CODE



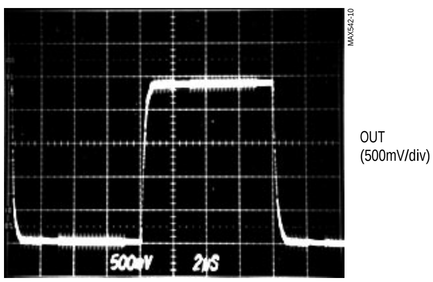
REFERENCE CURRENT vs. CODE



Typical Operating Characteristics (continued)

(V_{DD} = 5V ±5%, V_{REF} = 2.5V, T_A = +25°C, unless otherwise noted.)

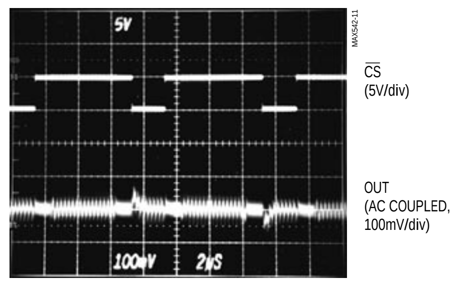
FULL-SCALE STEP RESPONSE



2µs/div

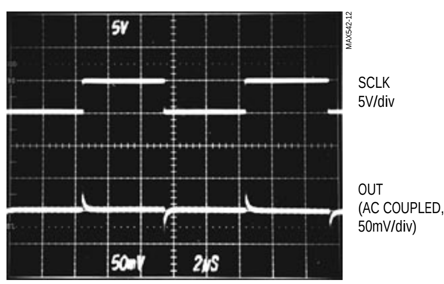
$R_L = \infty$, C_L = 10pF

MAJOR-CARRY OUTPUT GLITCH



2µs/div

DIGITAL FEEDTHROUGH



2µs/div

CODE = 0000 hex

Pin Description

PIN	NAME	FUNCTION
1	RFB	Feedback Resistor. Connect to external op amp's output in bipolar mode.
2	OUT	DAC Output Voltage
3	AGNDF	Analog Ground (force)
4	AGNDS	Analog Ground (sense)
5	REFS	Voltage Reference Input (sense). Connect to external 2.5V reference.
6	REFF	Voltage Reference Input (force). Connect to external 2.5V reference.
7	$\overline{CS}$	Chip-Select Input—active low
8	SCLK	Serial Clock Input. Duty cycle must be between 40% and 60%.
9	N.C.	No Connection. Not internally connected.
10	DIN	Serial Data Input
11	$\overline{LDAC}$	$\overline{LDAC}$ Input. A falling edge updates the internal DAC latch.
12	DGND	Digital Ground
13	INV	Junction of internal scaling resistors. Connect to external op amp's inverting input in bipolar mode.
14	V_{DD}	Supply Voltage

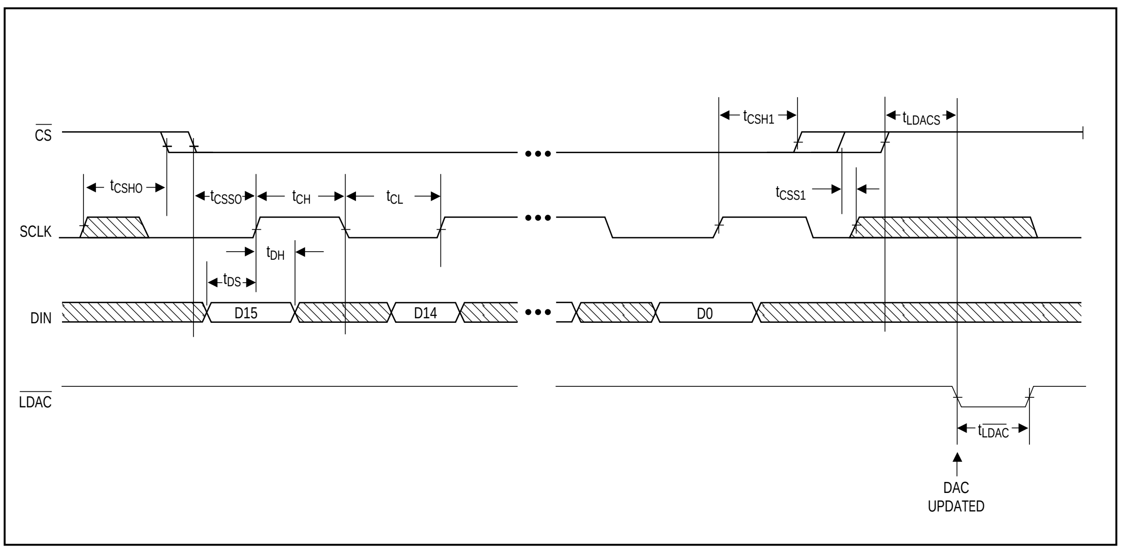


Figure 1. Timing Diagram

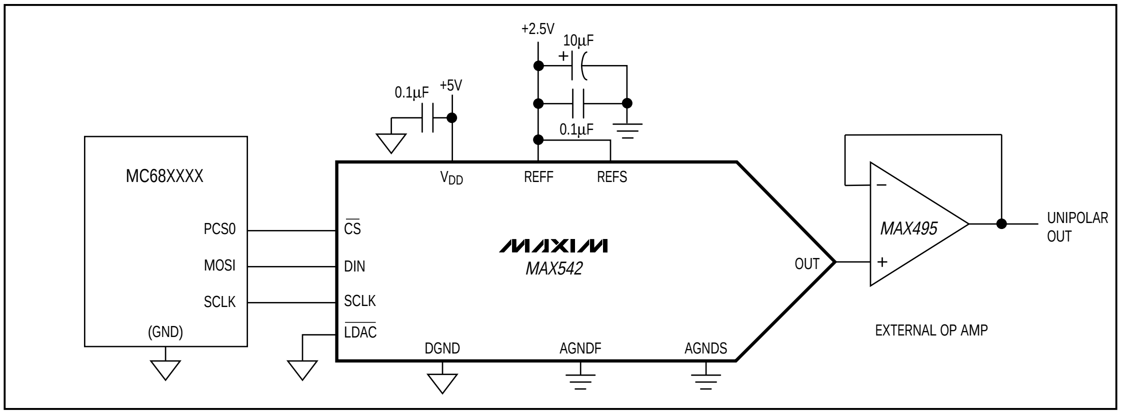


Figure 2a. Typical Operating Circuit—Unipolar Output

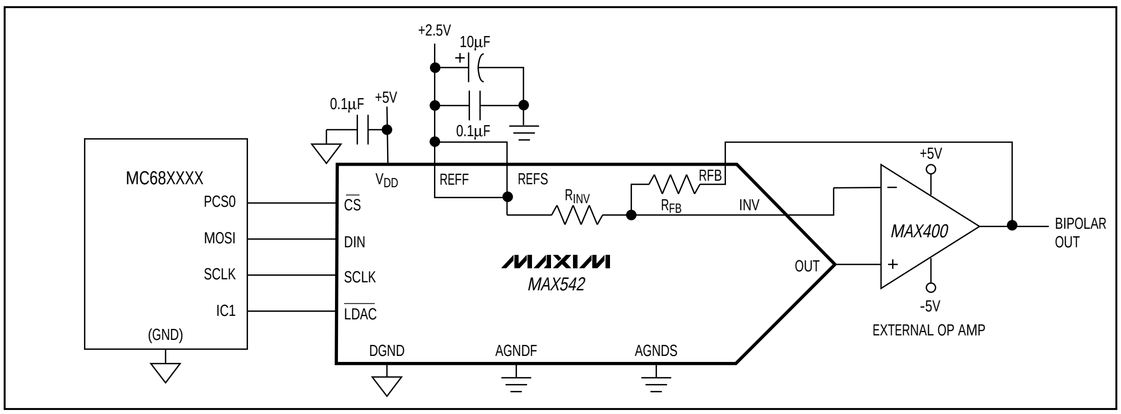


Figure 2b. Typical Operating Circuit—Bipolar Output

Detailed Description

The MAX542 16-bit voltage output, digital-to-analog converter (DAC) offers full 16-bit performance with less than 1LSB integral linearity error and less than 1LSB differential linearity error, thus ensuring monotonic performance. Serial data transfer minimizes the number of package pins required.

The MAX542 is composed of two matched DAC sections, with a 12-bit inverted R-2R DAC forming the 12 LSBs and the 4MSBs derived from 15 identically matched resistors. This architecture allows the lowest glitch energy to be transferred to the DAC output on major-carry transitions. It also lowers the DAC output impedance by a factor of eight compared to a standard R-2R ladder, allowing unbuffered operation in medium-load applications.

The MAX542 provides matched bipolar offset resistors, which connect to an external op amp to ensure accurate bipolar output swings (Figure 2b). For optimum performance, the MAX542 also provides a set of Kelvin connections to the voltage-reference and analog-ground inputs.

Digital Interface

The MAX542's digital interface is a standard 3-wire connection compatible with SPI™/QSPI™/Microwire™ interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at the data-input pin (DIN). Immediately following $\overline{CS}$'s high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial clock input (SCLK). After 16 data bits have been loaded into the serial input register, it transfers its contents to the DAC latch on $\overline{CS}$'s low-to-high transition if $\overline{LDAC}$ is tied low (Figure 3a). Note that if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word.

Alternatively, $\overline{LDAC}$ allows the DAC latch to update asynchronously by pulling $\overline{LDAC}$ low, independent of $\overline{CS}$ (Figure 3b). Hold $\overline{LDAC}$ high during the data-loading sequence.

External Reference

The MAX542 operates with external voltage references from 2V to 3V. The reference voltage determines the DAC's full-scale output voltage. Kelvin connections are provided for optimum performance. The 2.5V MAX873A, with ±15mV initial accuracy and a 7ppm/°C (max) temperature coefficient, is a good choice.

Power-On Reset

The MAX542 has a power-on reset circuit to set the DAC's output to 0V in unipolar mode when V_{DD} is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after a loss of power. In bipolar mode the DAC output is set to $-V_{REF}$.

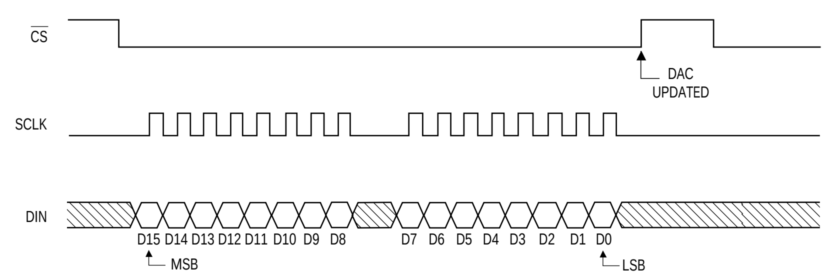


Figure 3a. 3-Wire Interface Timing Diagram ($\overline{LDAC}$ = DGND)

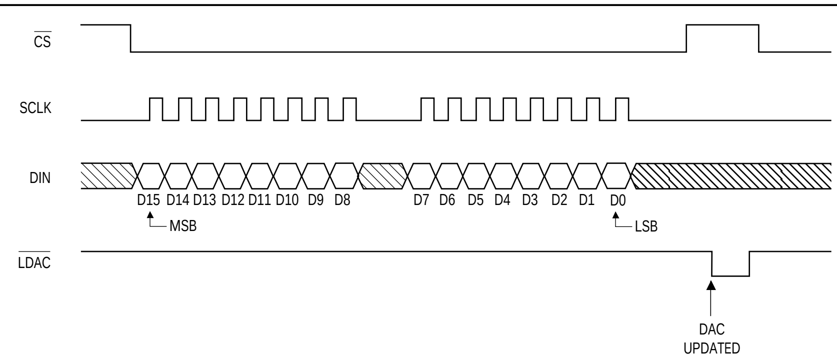


Figure 3b. 4-Wire Interface Timing Diagram

Applications Information

Reference and Analog Ground Inputs

The MAX542 operates with external voltage references from 2V to 3V, and maintains 16-bit performance if certain guidelines are followed when selecting and applying the reference. Ideally, the reference's temperature coefficient should be less than 0.4ppm/°C to maintain 16-bit accuracy to within 1LSB over the 0°C to +70°C commercial temperature range. Since this converter is designed as an inverted R-2R voltage-mode DAC, the input resistance seen by the voltage reference is code dependent. The worst-case input-resistance variation is from 11.5kΩ (at code 8555 hex) to 200kΩ (at code 0000 hex). The maximum change in load current for a 2.5V reference is 2.5V / 11.5kΩ = 217µA; therefore, the required load regulation is 7ppm/mA for a maximum error of 0.1LSB. This implies a reference output impedance of less than 18mΩ. In addition, the impedance of the signal path from the voltage reference to the reference input must be kept low because it contributes directly to the load-regulation error.

The requirement for a low-impedance voltage reference is met with capacitor bypassing at the REF_ inputs. A 0.1µF ceramic capacitor with short leads between REFF and AGNDF provides high-frequency bypassing. A surface-mount ceramic chip capacitor is preferred because it has the lowest inductance. An additional 10µF between REFF and AGNDF provides low-frequency bypassing. A low-ESR tantalum, film, or organic semiconductor capacitor works well. Leaded capacitors are acceptable because impedance is not as critical at lower frequencies. The circuit can benefit from even larger bypassing capacitors, depending on the stability of the external reference with capacitive loading. If separate force and sense lines are not used, tie the appropriate force and sense pins together close to the package.

AGND must also be low impedance, as load-regulation errors will be introduced by excessive AGND resistance. As in all high-resolution, high-accuracy applications, separate analog and digital ground planes yield the best results. Tie DGND to AGND at the AGND pin to form the "star" ground for the DAC system. Always refer remote DAC loads to this system ground for the best possible performance.

Unbuffered Operation

Unbuffered operation reduces power consumption as well as offset error contributed by the external output buffer. The R-2R DAC output is available directly at OUT, allowing 16-bit performance from $+V_{REF}$ to AGND without degradation at zero-scale. The DAC's output impedance is also low enough to drive medium loads (R_L > 60kΩ) without degradation of INL or DNL; only the gain error is increased by externally loading the DAC output.

External Output Buffer Amplifier

The requirements on the external output buffer amplifier change whether the DAC is used in the unipolar or bipolar mode of operation. In unipolar mode, the output amplifier is used in a voltage-follower connection. In bipolar mode, the amplifier operates with the internal scaling resistors (Figure 2b). In each mode, the DAC's output impedance is constant and is independent of input code; however, the output amplifier's input impedance should still be as high as possible to minimize gain errors. The DAC's output capacitance is also independent of input code, thus simplifying stability requirements on the external amplifier.

In bipolar mode, a precision amplifier operating with dual power supplies (such as the MAX400) provides the $\pm V_{REF}$ output range. In single-supply applications, precision amplifiers with input common-mode ranges including AGND are available; however, their output swings do not normally include the negative rail (AGND) without significant degradation of performance. A single-supply op amp, such as the MAX495, is suitable if the application does not use codes near zero.

Since the LSBs for a 16-bit DAC are extremely small (38.15µV for V_{REF} = 2.5V), pay close attention to the external amplifier's input specification. The input offset voltage can degrade the zero-scale error and might require an output offset trim to maintain full accuracy if the offset voltage is greater than 1/2LSB. Similarly, the input bias current multiplied by the DAC output resistance (typically 6.25kΩ) contributes to the zero-scale error. Temperature effects also must be taken into consideration. Over the 0°C to +70°C commercial temperature range, the offset voltage temperature coefficient (referenced to +25°C) must be less than 0.42µV/°C to add less than 1/2LSB of zero-scale error. The external amplifier's input resistance forms a resistive divider with the DAC output resistance, which results in a gain error. To contribute less than 1/2LSB of gain error, the input resistance typically must be greater than:

$$6.25k\Omega \div \frac{1}{2}\left[\frac{1}{2^{16}}\right] = 819M\Omega.$$

The setting time is affected by the buffer input capacitance, the DAC's output capacitance, and PC board capacitance. The typical DAC output voltage settling time is 1µs for a full-scale step. Settling time can be significantly less for smaller step changes. Assuming a single time-constant exponential settling response, a full-scale step takes 12 time constants to settle to within 1/2LSB of the final output voltage. The time constant is equal to the DAC output resistance multiplied by the total output capacitance. The DAC output capacitance is typically 10pF. Any additional output capacitance will increase the settling time.

The external buffer amplifier's gain-bandwidth product is important because it increases the settling time by adding another time constant to the output response. The effective time constant of two cascaded systems, each with a single time-constant response, is approximately the square root of the sum of the two time constants. The DAC output's time constant is 1µs / 12 = 83ns, ignoring the effect of additional capacitance. If the time constant of an external amplifier with 1MHz bandwidth is 1 / 2π (1MHz) = 159ns, then the effective time constant of the combined system is:

$$\sqrt{\left[(96ns)^2 + (159ns)^2\right]} = 186ns$$

This suggests that the settling time to within 1/2LSB of the final output voltage, including the external buffer amplifier, will be approximately 12 x 180ns = 2µs.

Digital Inputs and Interface Logic

The digital interface for the 16-bit DAC is based on a 3-wire standard that is compatible with SPI, QSPI, and Microwire interfaces. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input data serially into the DAC. $\overline{LDAC}$ updates the DAC output asynchronously.

All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX542 without additional external logic. The digital inputs are compatible with TTL/CMOS-logic levels.

Unipolar Configuration

Figure 2a shows the MAX542 configured for unipolar operation with an external op amp. The op amp is set for unity gain, and Table 1 shows the codes for this circuit.

Bipolar Configuration

Figure 2b shows the MAX542 configured for bipolar operation with an external op amp. The op amp is set for unity gain with an offset of $-1/2V_{REF}$. Table 2 shows the offset binary codes for this circuit.

Power-Supply Bypassing and Ground Management

For optimum system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND together at the IC. The best ground connection can be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass V_{DD} with a 0.1µF ceramic capacitor connected between V_{DD} and AGND. Mount it with short leads close to the device. Ferrite beads can also be used to further isolate the analog and digital power supplies.

Table 1. Unipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	V_{REF} x (65,535 / 65,536)
1000 0000 0000 0000	V_{REF} x (32,768 / 65,536) = $^1/_2 V_{REF}$
0000 0000 0000 0001	V_{REF} x (1 / 65,536)
0000 0000 0000 0000	0V

Table 2. Bipolar Code Table

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	$+V_{REF}$ x (32,767 / 32,768)
1000 0000 0000 0001	$+V_{REF}$ x (1 / 32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF}$ x (1 / 32,768)
0000 0000 0000 0000	$-V_{REF}$ x (32,768 / 32,768) = $-V_{REF}$

Ordering Information (continued)

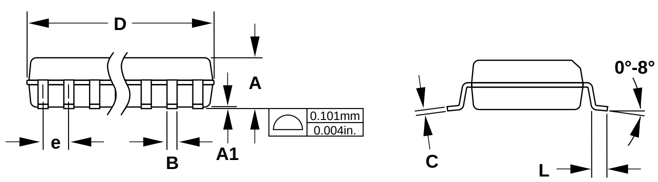
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX542AEPD	-40°C to +85°C	14 Plastic DIP	±1
MAX542BEPD	-40°C to +85°C	14 Plastic DIP	±2
MAX542CEPD	-40°C to +85°C	14 Plastic DIP	±4
MAX542AESD	-40°C to +85°C	14 SO	±1
MAX542BESD	-40°C to +85°C	14 SO	±2
MAX542CESD	-40°C to +85°C	14 SO	±4
MAX542CMJD	-55°C to +125°C	14 CERAMIC SB**	±4

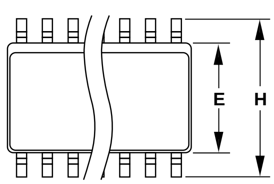
***Contact factory for availability.*

Chip Information

TRANSISTOR COUNT: 2209

Package Information





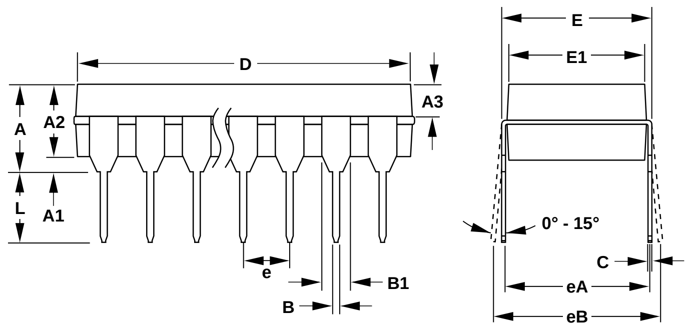
Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

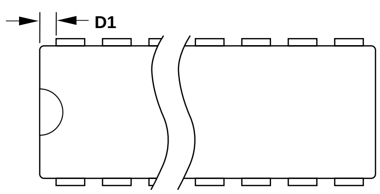
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

Package Information (continued)





Plastic DIP
PLASTIC DUAL-IN-LINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A