

PRELIMINARY
 Notice : This is not a final specification.
 some parametric limits are subject to change.

MITSUBISHI SOUND PROCESSOR

M62421SP/FP

SOUND CONTROLLER

Tone and Volume Controller with 2 Line Control

OUTLINE

M62421SP/FP is the tone and volume controller with 2 line control.
 This IC can apply the broad application because of low noise and distortion.

FEATURE

- TONE(Bass/Treble) control and 1dB step volume control are enabled .
- Low noise and low distortion .
 $V_{NO} = 4.5\mu V_{rms}$, THD=0.1% max
- Controlling by 2 Line serial data .

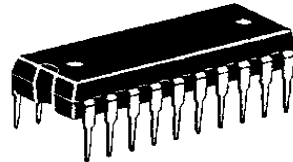
APPLICATION

- Mini-Stereo , etc

RECOMMENDED OPERATING CONDITION

- Supply voltage range 5.5~9.5V (analog) 4.5~5.5V (digital)
- Rated supply voltage 9V (analog) 5V (digital)

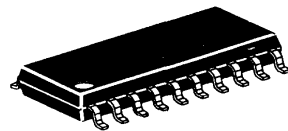
PACKAGE OUTLINE



20 P 4 B (SP)

PITCH : 1.78 mm

SIZE : 19.0 mm X 6.3 mm X 3.3 mm

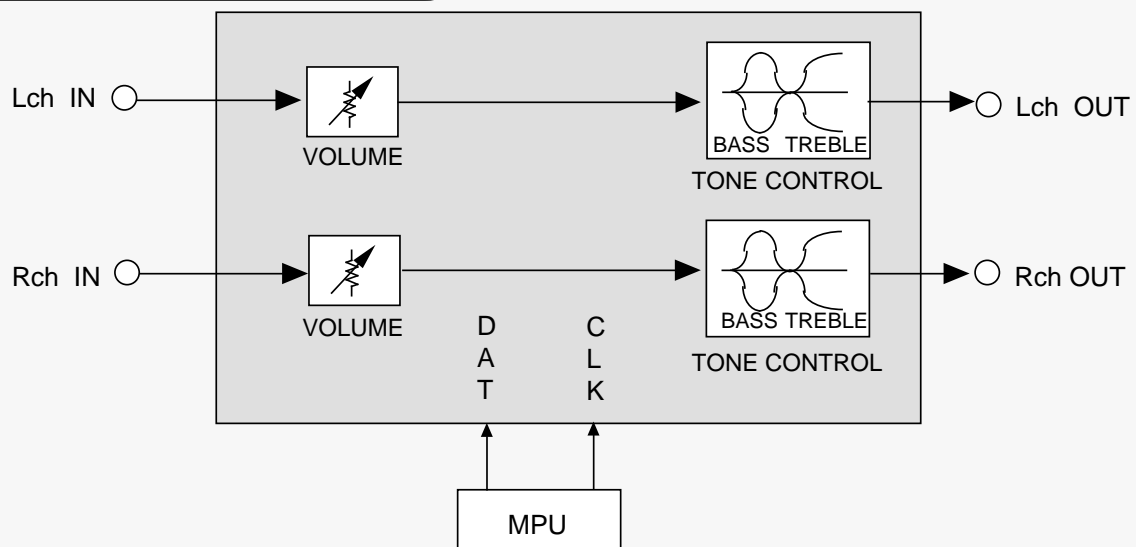


20 P 2 N (FP)

PITCH : 1.27 mm

SIZE : 5.3 mm X 12.6 mm X 1.8 mm

SYSTEM BLOCK DIAGRAM



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PIN DESCRIPTION

PIN No.	PIN NAME	I/O	DESCRIPTION
1	REF	I	Reference voltage terminal for analog
2	CH1 IN	I	Input terminal (ch1)
3	SIMIN 1	I	Pin for capacitor of simulated inductor 1
4	SIMOUT 1	O	Pin for capacitor of simulated inductor 1
5	BASS1	I	Pin for capacitor of ch1-side bass setting
6	TRE1	I	Pin for capacitor of ch1-side treble setting
7	OUT1	O	Output terminal (ch1)
8	DGND	—	Digital GND
9	DAT	I	I/O terminal of DATA 2 line bus format
10	CLK	I	Input terminal of CLOCK 2 line bus format
11	CS	I	Chip select terminal
12	DVDD	—	VDD for digital circuit
13	AGND	—	GND for analog circuit
14	OUT2	O	Output terminal (ch2)
15	TRE2	I	Pin for capacitor of ch2-side treble setting
16	BASS2	I	Pin for capacitor of ch2-side bass setting
17	SIMOUT2	O	Pin for capacitor of simulated inductor 2
18	SIMIN 2	I	Pin for capacitor of simulated inductor 2
19	CH2 IN	I	Input terminal (ch2)
20	AVDD	—	VCC for analog circuit

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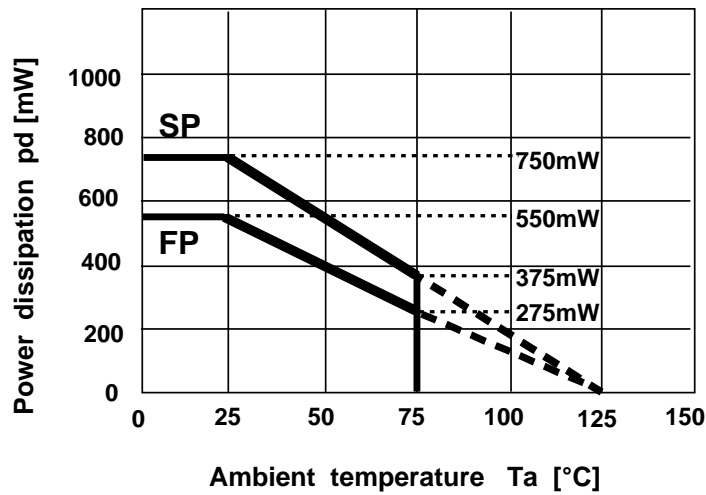
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SOUND CONTROLLER

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITION	LIMITS	UNIT
AVdd	Analog supply voltage		10.0	V
DVdd	Digital supply voltage		7.0	V
Pd	Power dissipation	Ta ≤ 25°C	750(SP) 550(FP)	mW
Kθ	Thermal Derating ratio	Ta > 25°C	7.5(SP) 5.5(FP)	mW/°C
Topr	Operating temperature		-20~+75	°C
Tstg	Storage temperature		-40~+125	°C

Thermal Derating



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RECOMMENDED OPERATING CONDITION

(Ta=25°C unless otherwise noted)

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Analog supply voltage	AVDD		5.5	9.0	9.5	V
Digital supply voltage	DVDD		4.5	5.0	5.5	V
H level input voltage (logic circuit)	VIH		0.7 DVDD	—	VDD	V
L level input voltage (logic circuit)	VIL		0	—	0.3 DVDD	V

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ELECTRIC CHARACTERISTICS

(Ta=25°C, AVDD=9V,DVDD=5V and bass and treble=0dB
 unless otherwise noted)

(1) SUPPLY VOLTAGE

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Analog supply current	Icc	•AVdd=9.0V •measure terminal=20 pin •no signal input	—	10	20	mA
Digital supply current	Idd	•DVdd= 5V •measure terminal=12 pin •no signal input	—	0	2	μA

(2) I / O CHARACTERISTICS

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Maximum input voltage	VIM	2,19pin input,7,14pin output RL=10K , THD=1%,f=1kHz ATT=-6dB	2.0	3.2	—	Vrms
Output voltage	Vodc	7pin,14pin, no signal	4.35	4.5	4.65	V
Gain	Gv	Vin=0dBm,FLAT,f=1kHz 2- 7PIN 19-14PIN gain	-2	0	2	dB
Output noise voltage	Vono	IHF-A filter no signal Rg=10K 7,14pin	—	4.5	10	μ Vrms
Total harmonic distortion	THD	7pin,14pin f=1kHz Vo=0.5Vrms , RL=10K LPF=30kHz	—	0.007	0.1	%
Channel separation	CT	RL=10K S:Vin=1Vrms,f=1kHz M:Rg=10k ,IHF-A filter	—	-100	-70	dB

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(3) TONE CHARACTERISTICS

ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Tone control gain (bass)	Gbassb	f=100Hz	9	12	15	dB
	Gbassc		-15	-12	-9	dB
Tone control gain (treble)	Gtrebb	f=10KHz	9	12	15	dB
	Gtrebc		-15	-12	-9	dB

(4) VOLUME CHARACTERISTICS

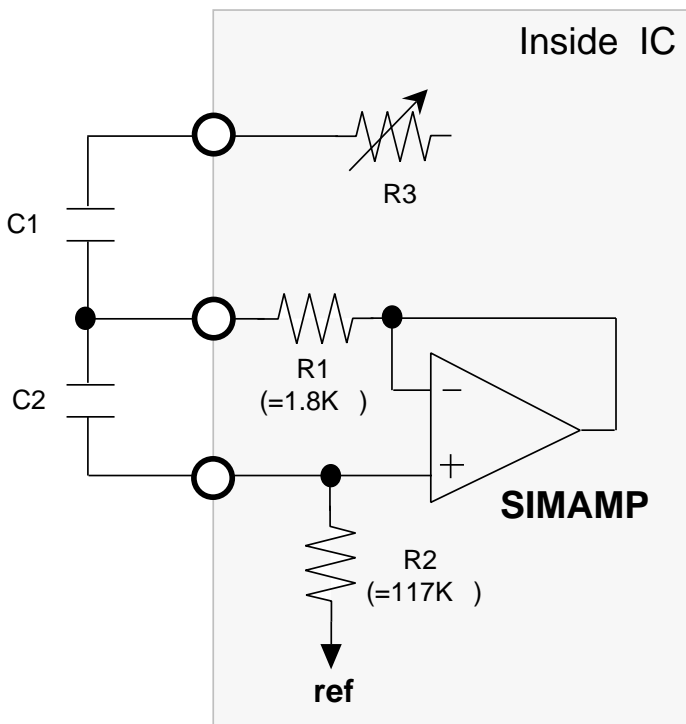
ITEM	SYMBOL	CONDITION	LIMIT			UNIT
			Min	typ	Max	
Maximum attenuation	ATTmax	f=1KHz, Vin=0dBm 2pin~7pin	-108	-100	-80	dB
Minimum attenuation	ATTmin	19pin~14pin gain IHF-A-filter	-1.5	0	1.5	dB

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FUNCTION EXPLANATION

(1) EQUIVALENT CIRCUIT OF TONE CONTROL

The resonance circuit is able to construct by using built-in amplifier for simulated inductor. (Shows the constant as follow)



Center frequency

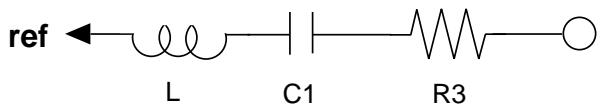
$$f_0 = 1 / 2 \sqrt{C1 \cdot C2 \cdot R1 \cdot R2} \text{ [Hz]}$$

$$Q = \sqrt{(C2 \cdot R2) / (C1 \cdot R1)}$$

(EX) BASS band ($f \approx 100\text{Hz}$)
 $R1=1.8\text{K}$, $R2=117\text{K}$
 $C1=0.47\mu$, $C2=0.022\mu$

FIG1. The circuit used simulated inductor.

FIG1 is equal to FIG2.
 The following relation is concluded.



$$L=C2 \cdot ER1 \cdot ER2$$

FIG2. The equivalent circuit used L.

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INPUT DATA FORMAT

← Input direction

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12
0/1	0/1	VOLUME						0/1	0	0	0/1	
	TREBLE	BASS				1	1	1	0			

0: BOTH
 1: ONLY 1CHANNEL

These functions are effective only VOLUME data.

0: 1ch
 1: 2ch

0:MUTE OFF
 1:MUTE ON

DATA SELECT
 0: VOLUME/MUTE
 1: BASS/TREBLE

If CS PIN(15 PIN) is "L" → 0,
 and if "H" → 1.

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(3) -1: volume control

VOLUME CODE

ATT	D2	D3	D4	D5	D6
0dB	H	L	H	L	H
-4dB	L	L	H	L	H
-8dB	H	H	L	L	H
-12dB	L	H	L	L	H
-16dB	H	L	L	L	H
-20dB	L	L	L	L	H
-24dB	H	H	H	H	L
-28dB	L	H	H	H	L
-32dB	H	L	H	H	L
-36dB	L	L	H	H	L
-40dB	H	H	L	H	L
-44dB	L	H	L	H	L
-48dB	H	L	L	H	L
-52dB	L	L	L	H	L
-56dB	H	H	H	L	L
-60dB	L	H	H	L	L
-64dB	H	L	H	L	L
-68dB	L	L	H	L	L
-72dB	H	H	L	L	L
-76dB	L	H	L	L	L
-80dB	H	L	L	L	L
- dB	L	L	L	L	L

ATT	D7	D8
0dB	H	H
-1dB	L	H
-2dB	H	L
-3dB	L	L

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(4) -2 : tone level control

TONE CODE

	BASS				TREBLE			
	D7	D6	D5	D4	D3	D2	D1	D0
12dB	L	H	H	L	L	H	H	L
10dB	L	H	L	H	L	H	L	H
8dB	L	H	L	L	L	H	L	L
6dB	L	L	H	H	L	L	H	H
4dB	L	L	H	L	L	L	H	L
2dB	L	L	L	H	L	L	L	H
0dB	L	L	L	L	L	L	L	L
-2dB	H	L	L	H	H	L	L	H
-4dB	H	L	H	L	H	L	H	L
-6dB	H	L	H	H	H	L	H	H
-8dB	H	H	L	L	H	H	L	L
-10dB	H	H	L	H	H	H	L	H
-12dB	H	H	H	L	H	H	H	L

NOT USED HHHH
 LHHH
 HLLL

(3) -3 : MUTE CONTROL

On condition D9=1,MUTE can be set up.
 In MUTE,VOLUME LEVEL is set up VOL=-
 automatically.

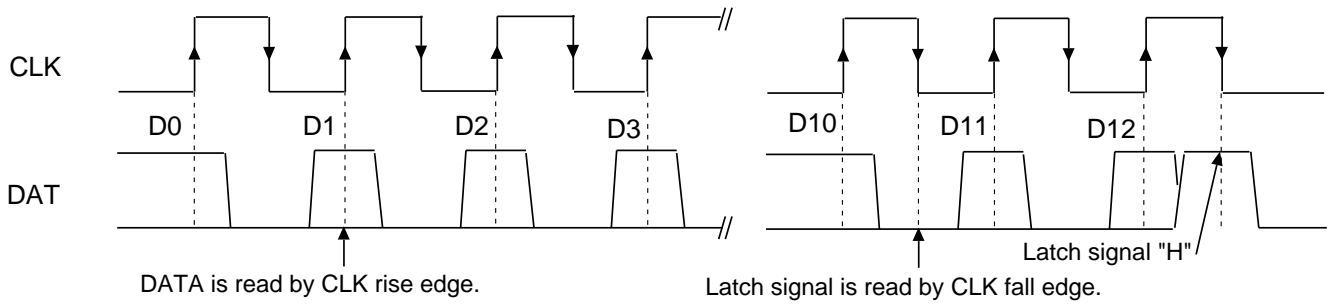
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DATA and CLOCK



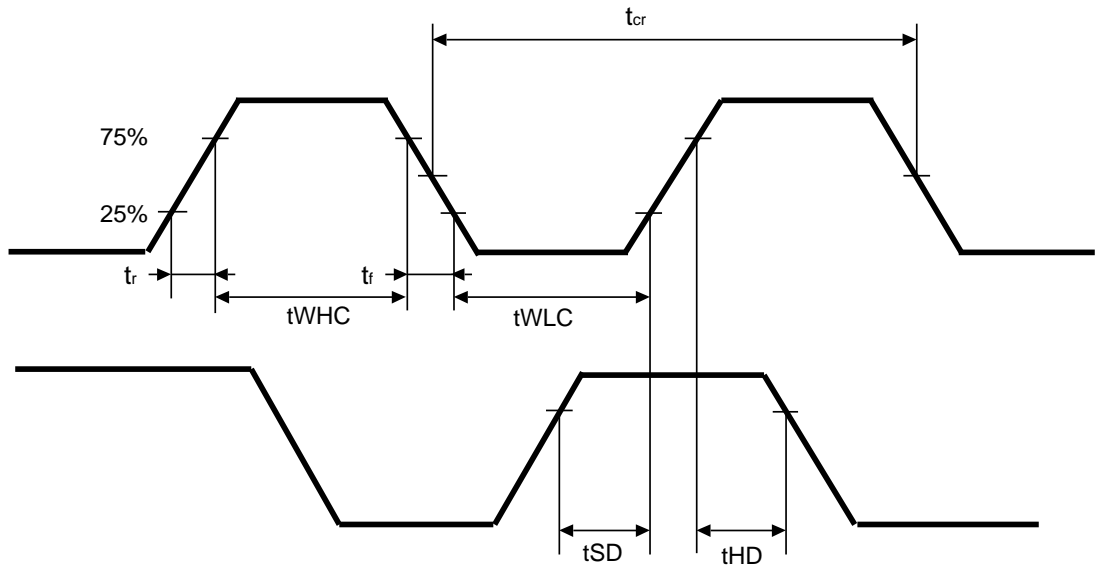
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BUS LINE TIMING SPECIFICATION



Parameter	Symbol	MIN	MAX	Units
CLK clock frequency	t_{cr}	4	-	μs
The HIGH period of the clock	t_{WHC}	1.6	-	μs
The LOW period of the clock	t_{WLC}	1.6	-	μs
Rise time of CLK line	t_r	-	0.4	μs
Fall time of CLK line	t_f	-	0.4	μs
Set-up time DATA	t_{SD}	0.8	-	μs
Hold time DATA	t_{HD}	0.8	-	μs

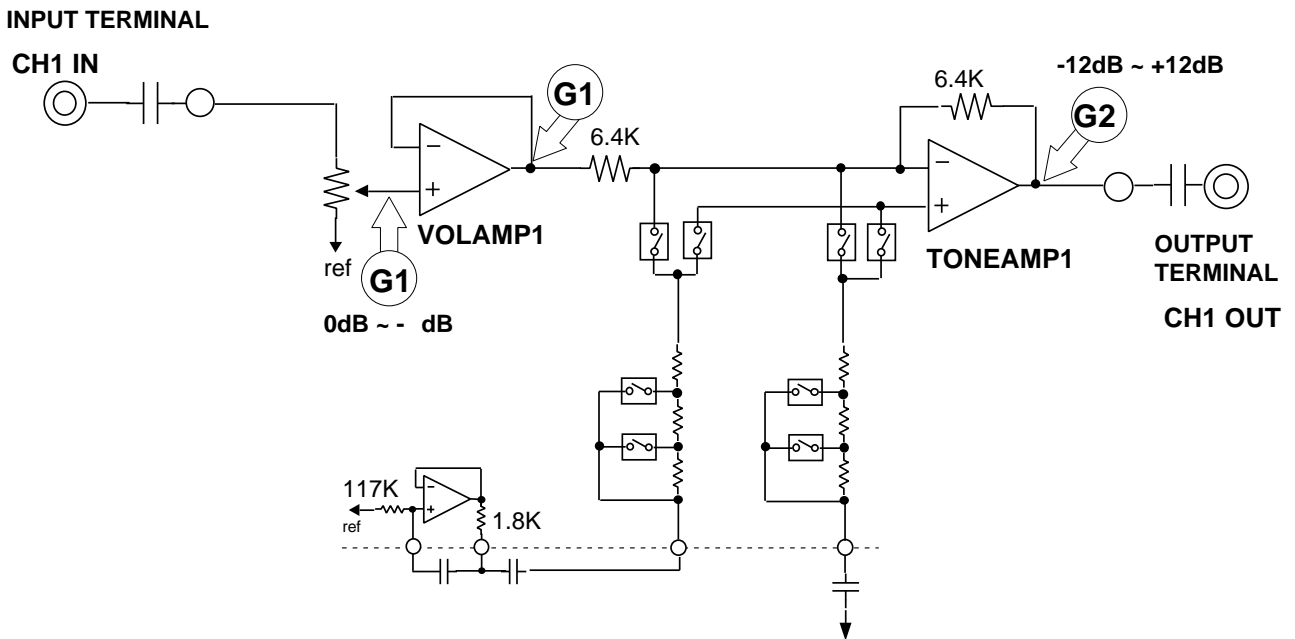
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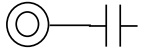
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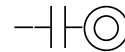
LEVEL DIAGRAM



INPUT TERMINAL
 CH2 IN



----- Same to CH 1 -----



OUTPUT TERMINAL
 CH2 OUT

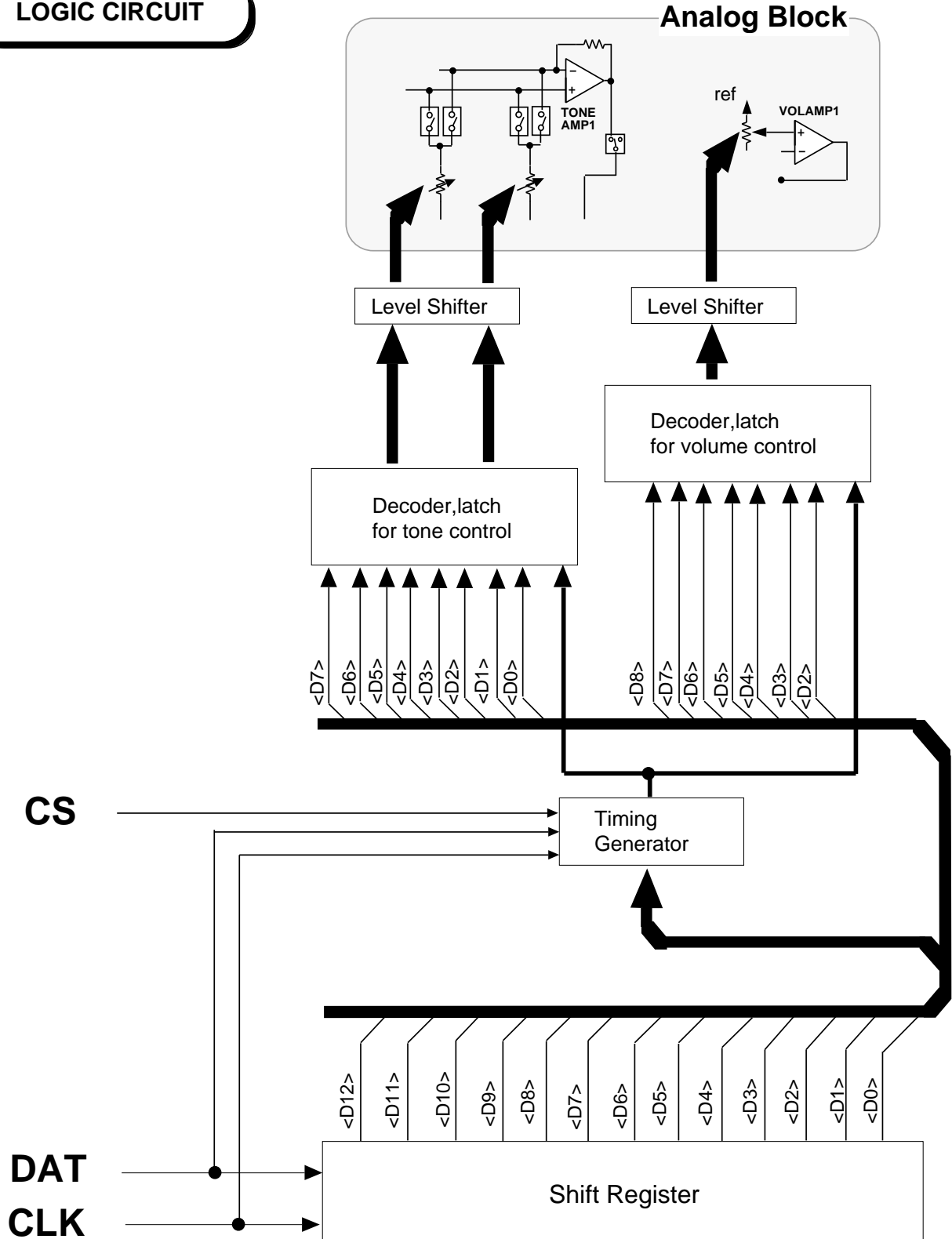
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LOGIC CIRCUIT



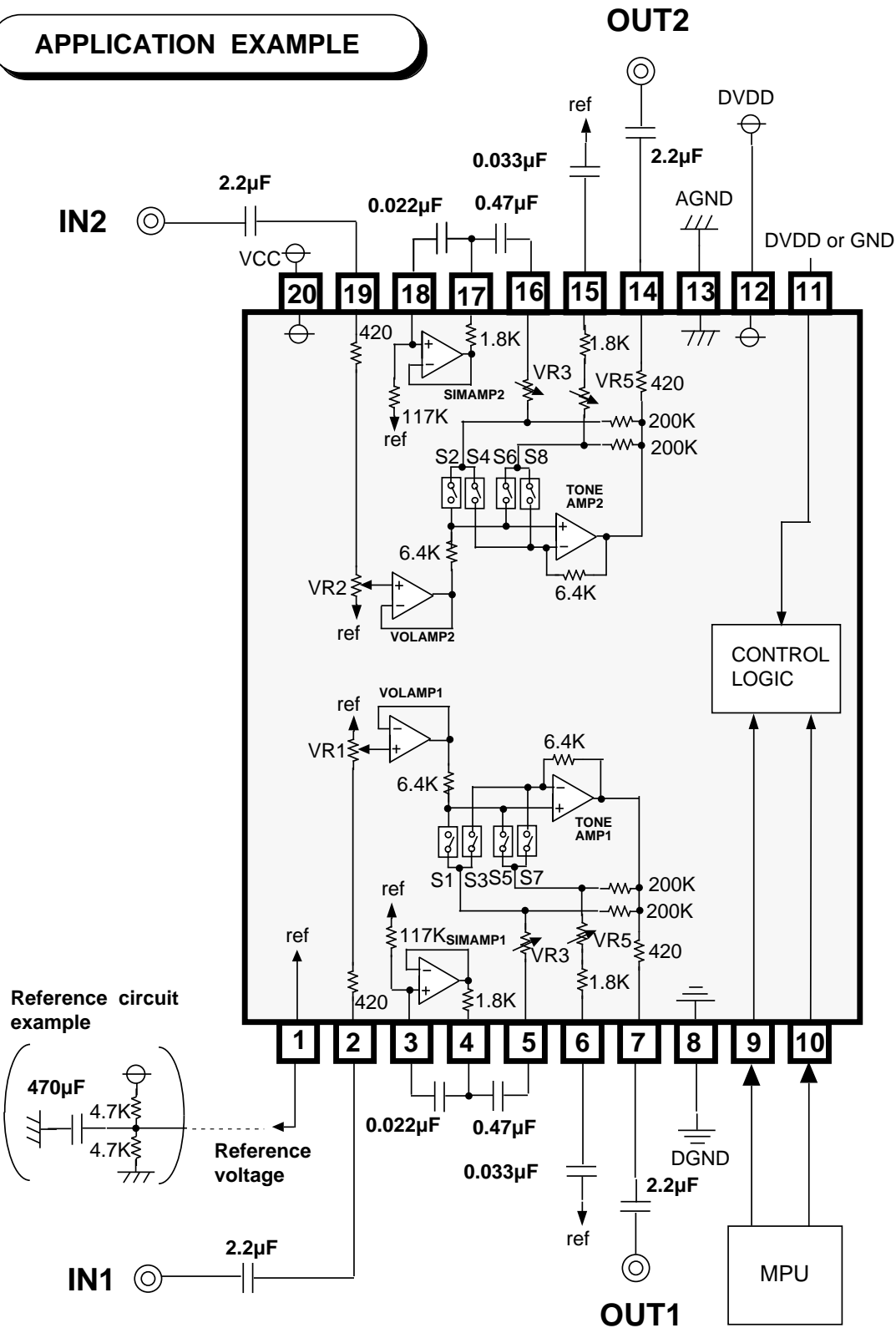
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APPLICATION EXAMPLE



Reference circuit example

