SGS-THOMSON MICROELECTRONICS

M54HC356
M74HC356

8-CHANNEL MULTIPLEXER/REGISTER WITH LATCHES (3-STATE)

- HIGH SPEED
  t_{PD} = 29 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS356

B1N
Plastic Package

F1
Ceramic Frit Seal Package

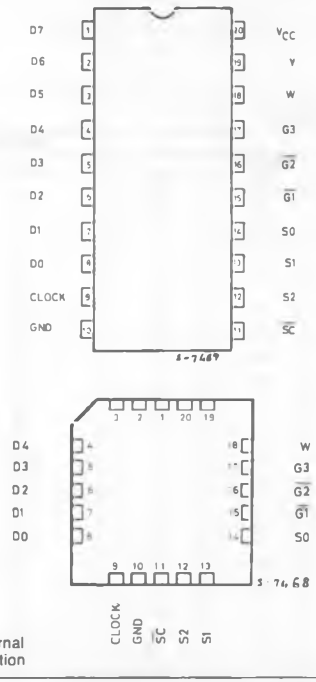
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC356 F1
M74HC356 B1N
M74HC356 F1
M74HC356 C1
M74HC356 M1

PIN CONNECTIONS (top view)



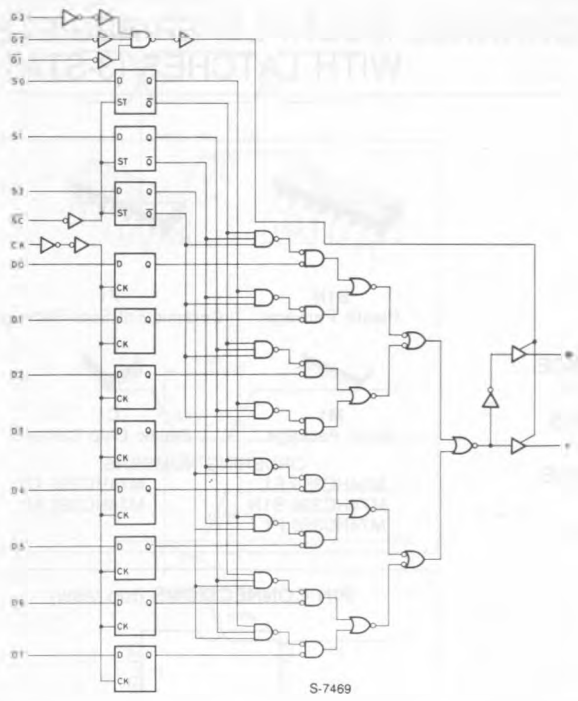
NC =
No Internal
Connection

DESCRIPTION

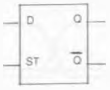
The M54/74HC356 is a high speed CMOS 8-CHANNEL MULTIPLEXER/REGISTER (3-State) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.
This device contains an 8 channel digital multiplexer with an 8-bit input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) is determineted by the address data.

The information at the data inputs (D0 to D7) is stored in the 8-bit flip-flop at the positive going edge of clock input (CLOCK). The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when input $\overline{G1}$ is held high, input $\overline{G2}$ is held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system. The M54/74HC356 is similar in function to the M54/74HC354, which has an 8-bit latch as the data register instead of an 8-bit flip-flop. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



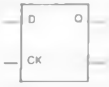
TRUTH TABLE OF INTERNAL LATCH



INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE — Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE

TRUTH TABLE OF INTERNAL LATCH (FLIP-FLOP)



D	CK	Q
L	↑	L
H	↑	H
X	↓	Qn

X: DON'T CARE
Qn: NO CHANGE

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT*			CLOCK	OUTPUT ENABLES				
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	↓	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	↓	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	↓	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	↓	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	↓	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	↓	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	↓	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	↓	L	L	H	$\overline{D7n}$	D7n

X: DON'T CARE - Z: HIGH IMPEDANCE *: This column shows the input address setup with SC Low.
D0.....D7: The level of steady-state inputs at input D0 through D7, respectively, at the time of the low-to-high transition of clock

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	DC Input Voltage	− 0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	− 65 to 150	°C

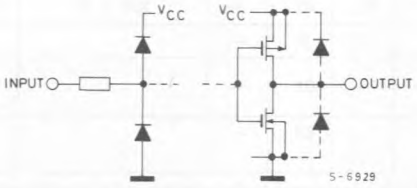
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	− 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		− 6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		7.8		− 7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	± 0.5	—	± 5		± 10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

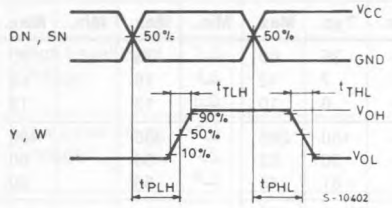
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Y, W)	2.0		—	150	265	—	330		400	ns
		4.5		—	36	53	—	66		80	
		6.0		—	31	45	—	56		60	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		—	160	285	—	355		430	ns
		4.5		—	40	57	—	71		86	
		6.0		—	34	48	—	60		73	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SC}$ - Y, W)	2.0		—	160	295	—	370		445	ns
		4.5		—	40	59	—	74		89	
		6.0		—	34	50	—	63		76	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{SC}$)	2.0		—	30	75	—	95		110	
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time (Sn)	2.0		—	25	75	—	95		110	
		4.5		—	5	15	—	19		22	
		6.0		—	4	13	—	16		19	
t_s	Minimum Set-up Time (Dn)	2.0		—	40	75	—	95	—	110	
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_h	Minimum Hold Time (Sn)	2.0		—	—	5	—	5	—	5	
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_h	Minimum Hold Time (Dn)	2.0		—	—	0	—	0	—	0	
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{PZL} t_{PZH}	Output Enable Time	2.0		—	68	125	—	155	—	190	
		4.5		—	17	25	—	31	—	38	
		6.0	$R_L = 1K\Omega$	—	15	21	—	26	—	22	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0		—	60	155	—	195	—	235	
		4.5		—	22	31	—	39	—	47	
		6.0	$R_L = 1K\Omega$	—	20	26	—	33		40	
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—			
C_{PD} (*)	Power Dissipation Capacitance			—	53	—	—	—			pF

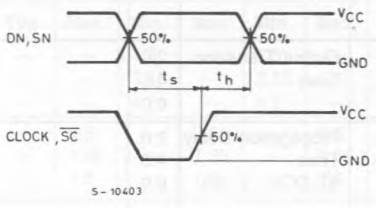
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

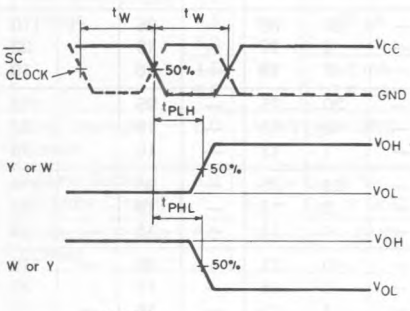
Average operating current can be obtained by the following equation.

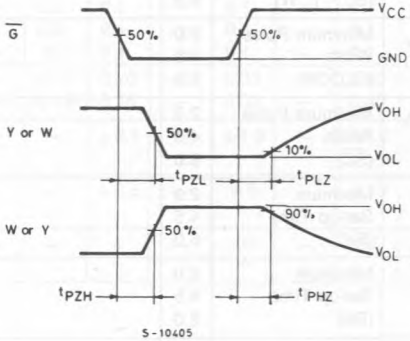
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM









TEST CIRCUIT WAVEFORM I_{CC} (Opr.)