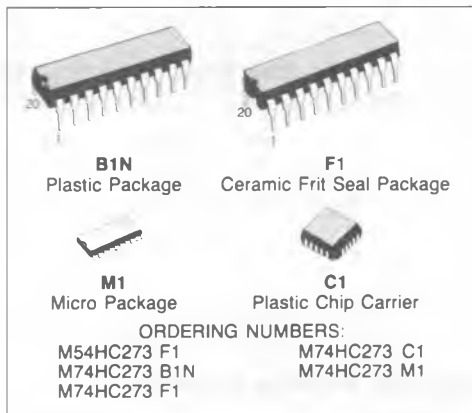


## OCTAL D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED  
 $f_{MAX} = 48 \text{ MHz (TYP.) at } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY  
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY  
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE  
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS  
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE  
 $V_{CC} \text{ (OPR)} = 2 \text{ V to } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE  
 WITH 54/74LS273



### DESCRIPTION




The M54/74HC273 is a high speed CMOS OCTAL D-TYPE FLIP FLOP WITH CLEAR fabricated in silicon gate C<sup>2</sup>MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

Information signals applied to D inputs are transferred to the Q outputs on the positive-going edge of the clock pulse.

When the CLEAR input is held low, the Q output are in the low logic level independent of the other inputs.

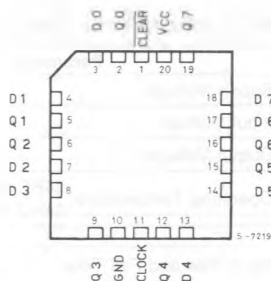
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
CLEAR	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q <sub>n</sub>	NO CHANGE

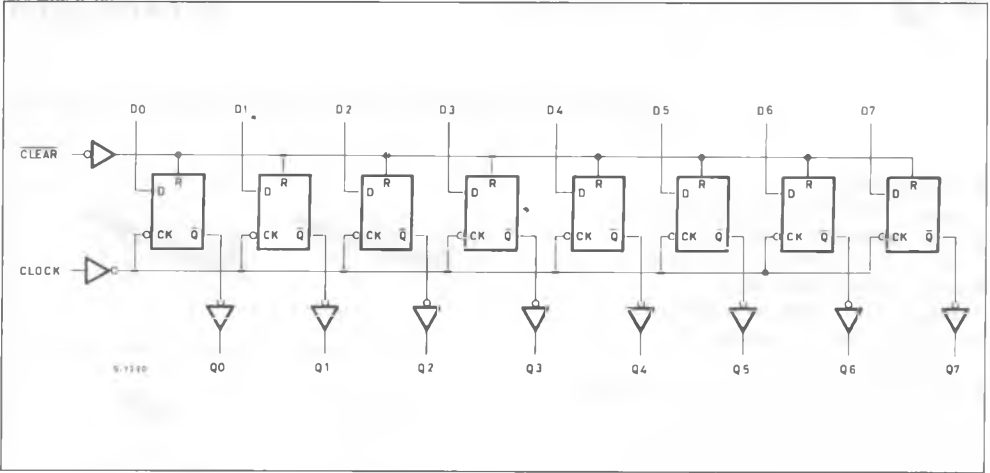
X: DON'T CARE

### PIN CONNECTIONS (top view)



NC =  
No Internal  
Connection

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to 7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Source Sink Current Per Output Pin	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
PD	Power Dissipation	500 (*)	mW
$T_{stg}$	Storage Temperature	-65 to 150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW:  $\cong$  65 $^{\circ}C$  derate to 300 mW by 10 mW/ $^{\circ}C$ : 65 $^{\circ}C$  to 85 $^{\circ}C$ .

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_A$	Operating Temperature	74HC Series 54HC Series	-40 to 85 -55 to 125	$^{\circ}C$
$t_r, t_f$	Input Rise and Fall Time	$V_{CC}$ { 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

## DC SPECIFICATIONS

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V <sub>IH</sub>	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V	
V <sub>IL</sub>	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V	
V <sub>OH</sub>	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V <sub>I</sub>	I <sub>O</sub>	1.9	2.0	—	1.9	—	1.9	—	V
			V <sub>IH</sub> or V <sub>IL</sub>	- 20 μA	4.4 5.9	4.5 6.0	— —	4.4 5.9	— —	4.4 5.9	— —	
				- 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
				- 5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V <sub>OL</sub>	Low Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	20 μA	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
				4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
				5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
					—			—				
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND	—	—	± 0.1	—	± 1.0	—	± 1.0	μA	
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND	—	—	4	—	40	—	80	μA	

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, C<sub>L</sub> = 15pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time	—	4	8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLOCK-Q)	—	20	31	ns
t <sub>PHL</sub>	Propagation Delay Time (CLEAR-Q)	—	19	30	ns
f <sub>MAX</sub>	Maximum Clock Frequency	30	48	—	MHz

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

Symbol	Parameter	$V_{CC}$	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			$-40$ to $85^\circ\text{C}$ 74HC		$-55$ to $125^\circ\text{C}$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{TLH}$ $t_{THL}$	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	9	15	—	19	—	22	
		6.0		—	8	13	—	16	—	19	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CLOCK - Q)	2.0		—	92	180	—	225	—	270	ns
		4.5		—	25	36	—	45	—	54	
		6.0		—	22	31	—	38	—	46	
$t_{PLH}$	Propagation Delay Time (CLEAR-Q)	2.0		—	92	175	—	220	—	265	ns
		4.5		—	25	35	—	44	—	53	
		6.0		—	22	30	—	37	—	45	
$f_{MAX}$	Maximum Clock Frequency	2.0		5.4	11	—	4.4	—	3.6	—	MHz
		4.5		27	44	—	22	—	18	—	
		6.0		32	52	—	26	—	21	—	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
$t_s$	Minimum Set-up Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	6	13	—	16	—	19	
$t_h$	Minimum Hold Time	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
$t_{REM}$	Minimum Removal Time CLEAR	2.0		—	18	75	—	95	—	110	ns
		4.5		—	5	15	—	19	—	22	
		6.0		—	4	13	—	16	—	19	
$C_{IN}$	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	53	—	—	—	—	—	pF

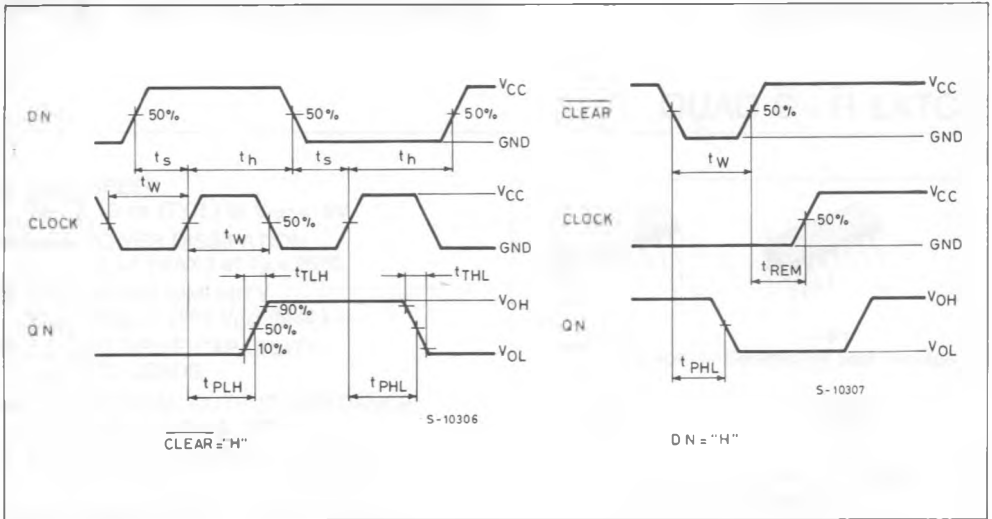
Note (\*)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current is:  $I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$  (per FF)

And the total  $C_{PD}$  when n pcs Flip Flop operate can be gained by the following equation.

$$C_{PD}(\text{total}) = 38 + 15 \cdot n$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT  $I_{CC}$  (Opr.)

