



M14C64 M14C32

Memory Card IC 64/32 Kbit Serial I²C Bus EEPROM

DATA BRIEFING

- Compatible with I²C Extended Addressing
- Two Wire I²C Serial Interface
Supports 400 kHz Protocol
- Single Supply Voltage (2.5 V to 5.5 V)
- Hardware Write Control
- BYTE and PAGE WRITE (up to 32 Bytes)
- BYTE, RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behaviour
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)
- 5 ms Programming Time (typical)

DESCRIPTION

Each device is an electrically erasable programmable memory (EEPROM) fabricated with STMicroelectronics's High Endurance, Single Polysilicon, CMOS technology. This guarantees an endurance typically well above one million Erase/Write cycles, with a data retention of 40 years. The memory operates with a power supply as low as 2.5 V for the M14Cxx-W version.

The M14C32 is available in wafer form (either sawn or unsawn) and in micromodule form (on film). The M14C64 is available in micro-module

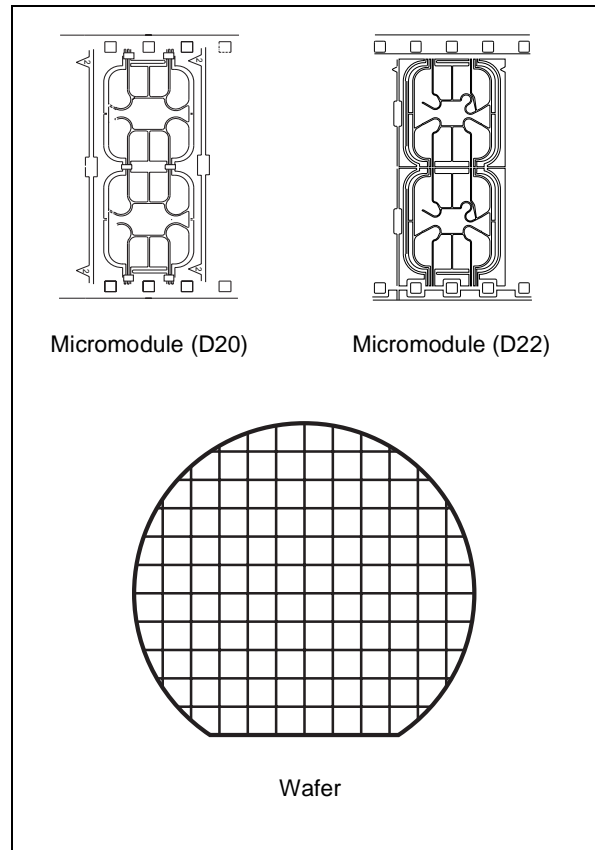


Figure 1. Logic Diagram

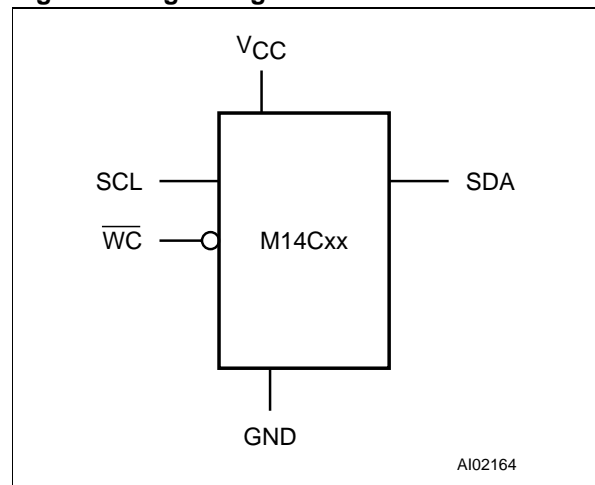


Table 1. Signal Names

SDA	Serial Data/Address Input/Output
SCL	Serial Clock
\overline{WC}	Write Control
VCC	Supply Voltage
GND	Ground

Figure 2. D20 Contact Connections

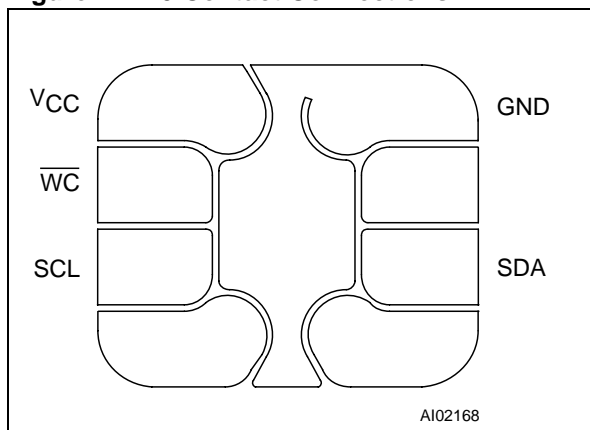
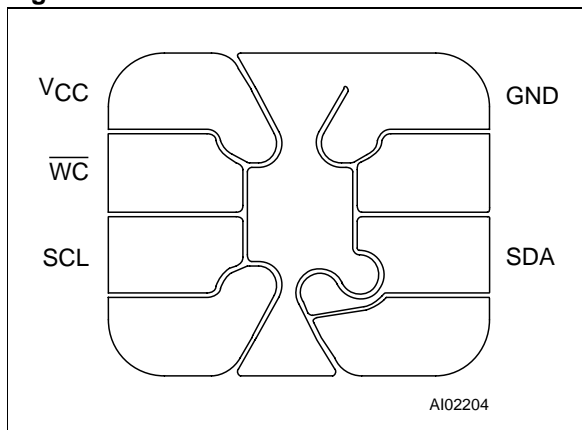


Figure 3. D22 Contact Connections



form only. For availability of the M14C64 in wafer form, please contact your ST sales office.

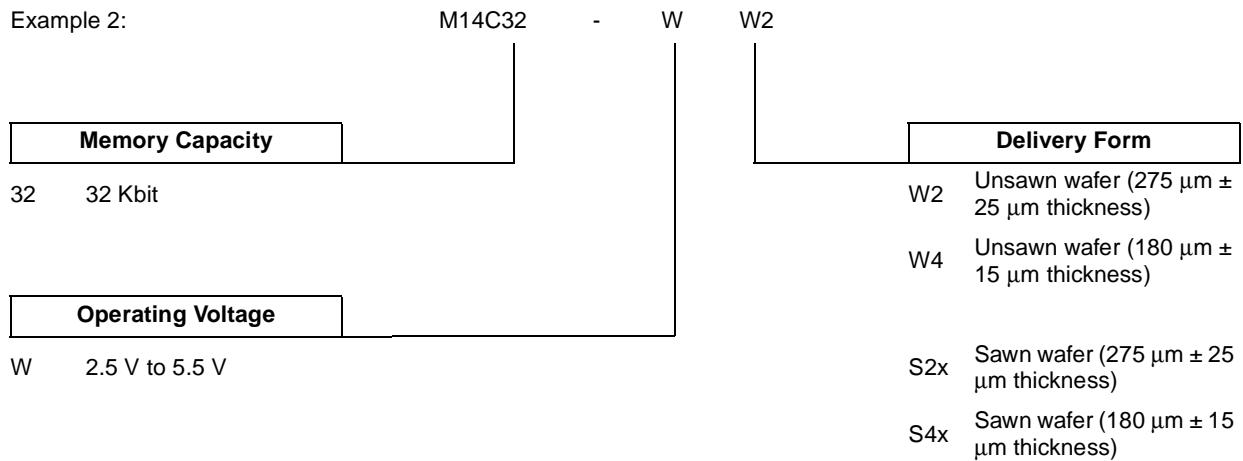
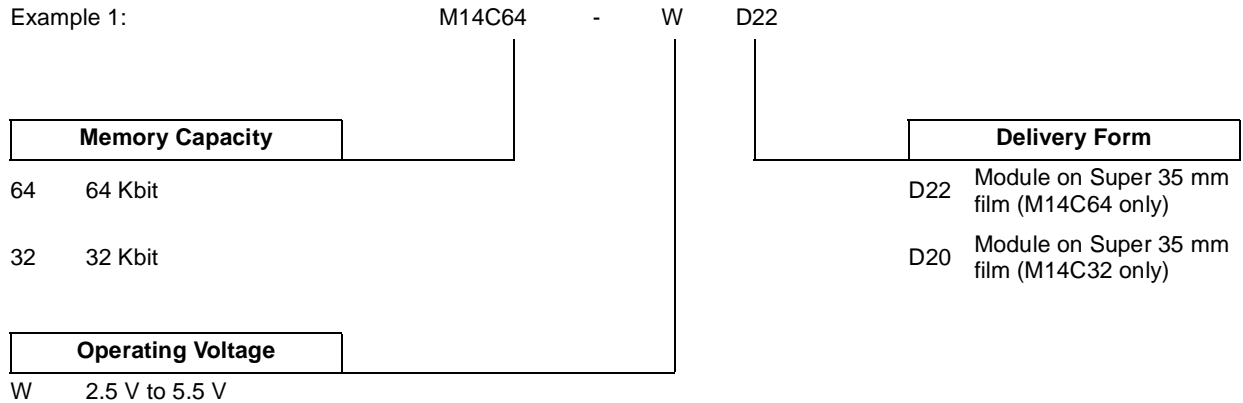
Each memory is compatible with the I²C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 7-bit unique Device Type Identifier code (1010000) in accordance with the I²C bus definition. Only one memory can be attached to each I²C bus.

The memory behaves as a slave device in the I²C protocol, with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition, generated by the

bus master. The START condition is followed by the Device Select Code which is composed of a stream of 7 bits (1010000), plus one read/write bit (R/W) and is terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Table 2. Ordering Information Scheme



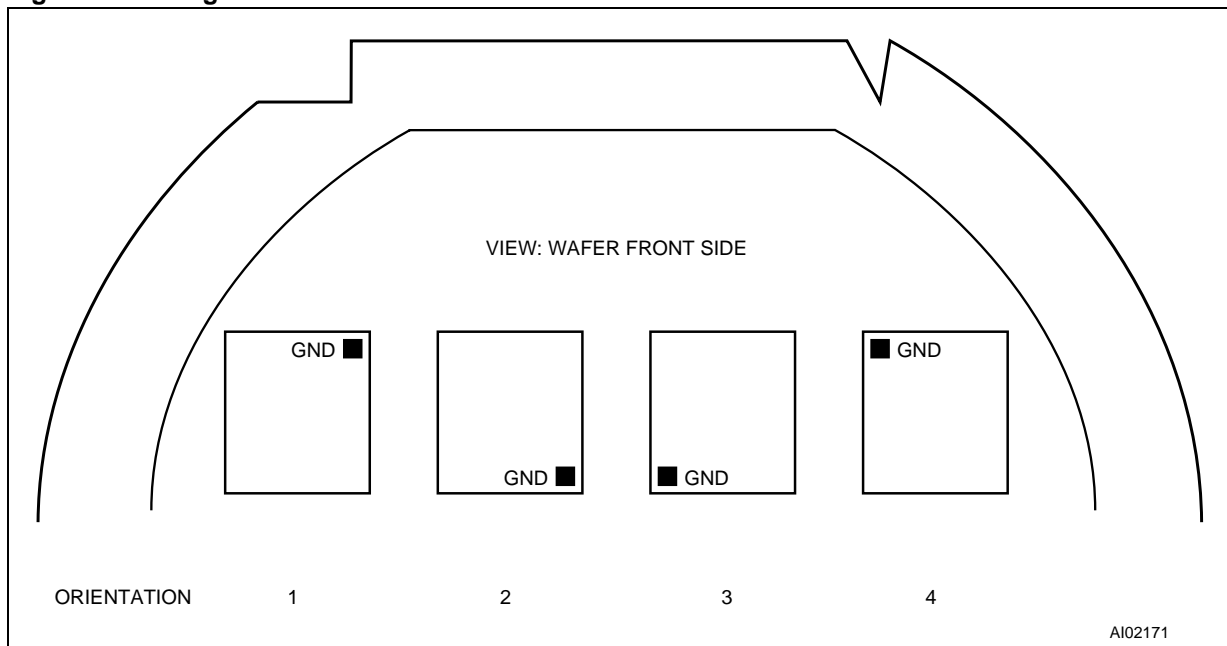
where "x" indicates the sawing orientation, as follows (and as shown in Figure 4)

- 1 GND at top right
- 2 GND at bottom right
- 3 GND at bottom left
- 4 GND at top left

Devices are shipped from the factory with the memory content set at all '1's (FFh).

For a list of available options (speed, package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Figure 4. Sawing Orientation



Sawn wafers are scribed and mounted in a frame on adhesive tape. The orientation is defined by the position of the GND pad on the die, viewed with active area of product visible, relative to the notches of the frame (as shown in Figure 4). The orientation of the die with respect to the plastic frame notches is specified by the Customer.

One further concern, when specifying devices to be delivered in this form, is that wafers mounted on adhesive tape must be used within a limited period from the mounting date:

- two months, if wafers are stored at 25°C, 55% relative humidity
- six months, if wafers are stored at 4°C, 55% relative humidity