KS88C0316 MICROCONTROLLER

The KS88C0316 single-chip CMOS microcontroller is designed for a wide range of electronics applications that require support for HDLC or SDLC data transfer standards. In addition to seven I/O ports, the KS88C0316 has an Advanced Data Link Control (ADLC) module, a full-duplex serial port with three UART modes, and programmable timers and timer/counters. There are 16 K bytes of on-chip program ROM. You can also choose to implement the chip in ROM-less mode to access external memory or other peripherals over the external bus interface. This powerful microcontroller is available in a 64-pin SDIP or 64-pin QFP package.

FEATURES

CPU

- SAM8 CPU core

Memory

- 272-byte general purpose register area
- 16-Kbyte internal program memory
- ROM-less operating mode

External Interface

- 64-Kbyte external data memory area
- 64-Kbyte external program memory area (ROM-less mode)

Instruction Set

- 79 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 600 ns at 20 MHz f_{OSC} (minimum)

Interrupts

- 21 interrupt sources
- 21 interrupt vectors
- Eight interrupt levels
- Fast interrupt processing

Timer/Counters

- Two 8-bit timers with interval timer and PWM modes
- Two 16-bit general-purpose timer/counters with four programmable operating modes

Backup Timer

- 16-bit backup timer with 15-bit prescaler

Advanced Data Link Control (ADLC) Block

- Full support for HDLC and SDLC protocols
- Digital PLL circuit for clock synchronization
- Address recognition circuit
- Automatic flag detection and synchronization
- Zero insert/delete, FCS, and abort features
- NRZ/NRZI data modes

General I/O

- Seven I/O ports (54 pins):
- Three nibble-programmable ports
- One bit-programmable port
- Two bit-programmable ports with external interrupt enable and pending control
- One n-channel, open-drain output port

UART Module

- One synchronous operating mode and three full-duplex asynchronous UART modes

Operating Temperature Range

- $-20^{\circ}C$ to $+85^{\circ}C$

Operating Voltage Range

- 4.5 V to 5.5 V

Package Types

- 64-pin SDIP, 64-pin QFP

BLOCK DIAGRAM

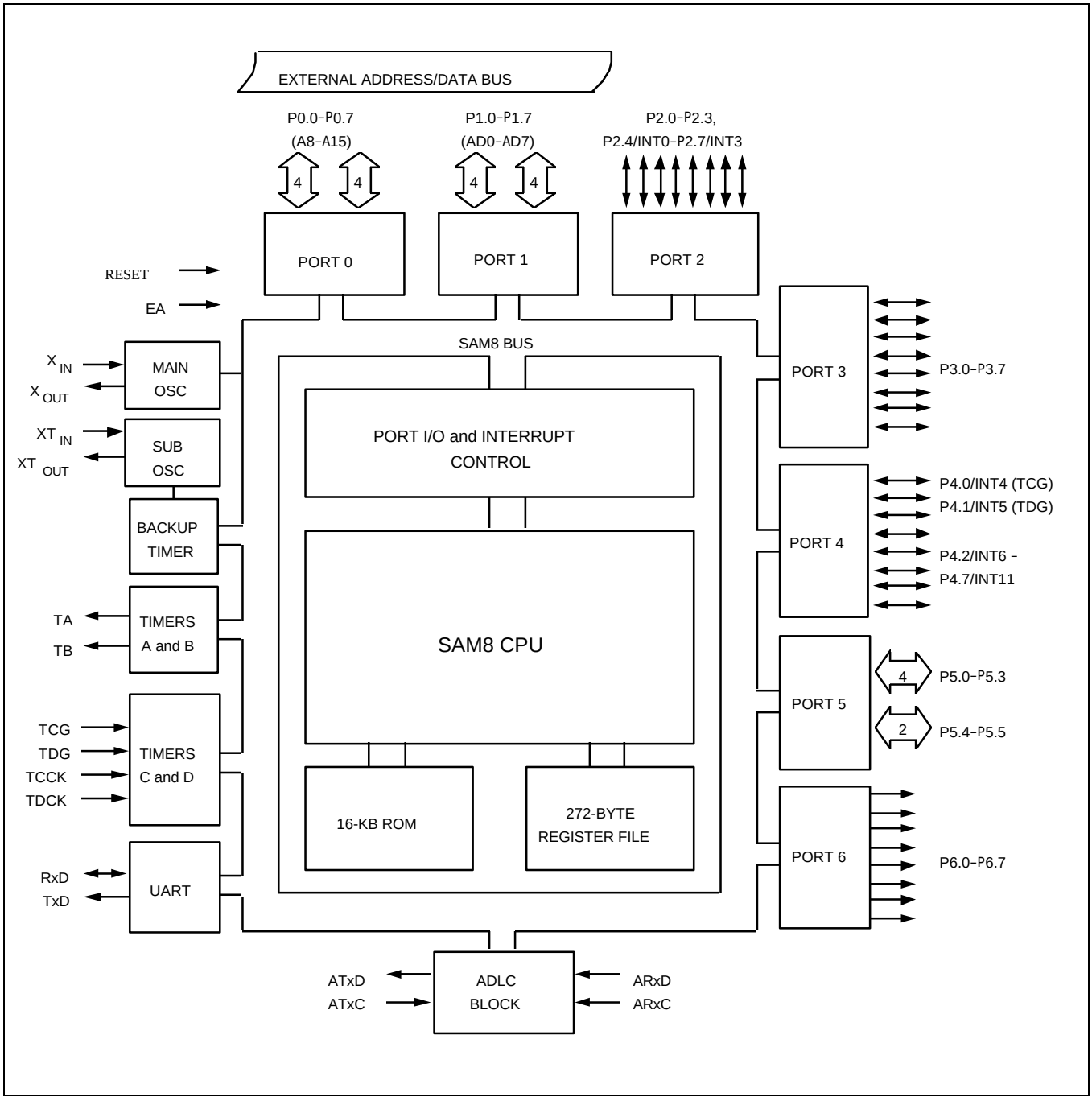

Figure 1. Block Diagram

PIN ASSIGNMENTS

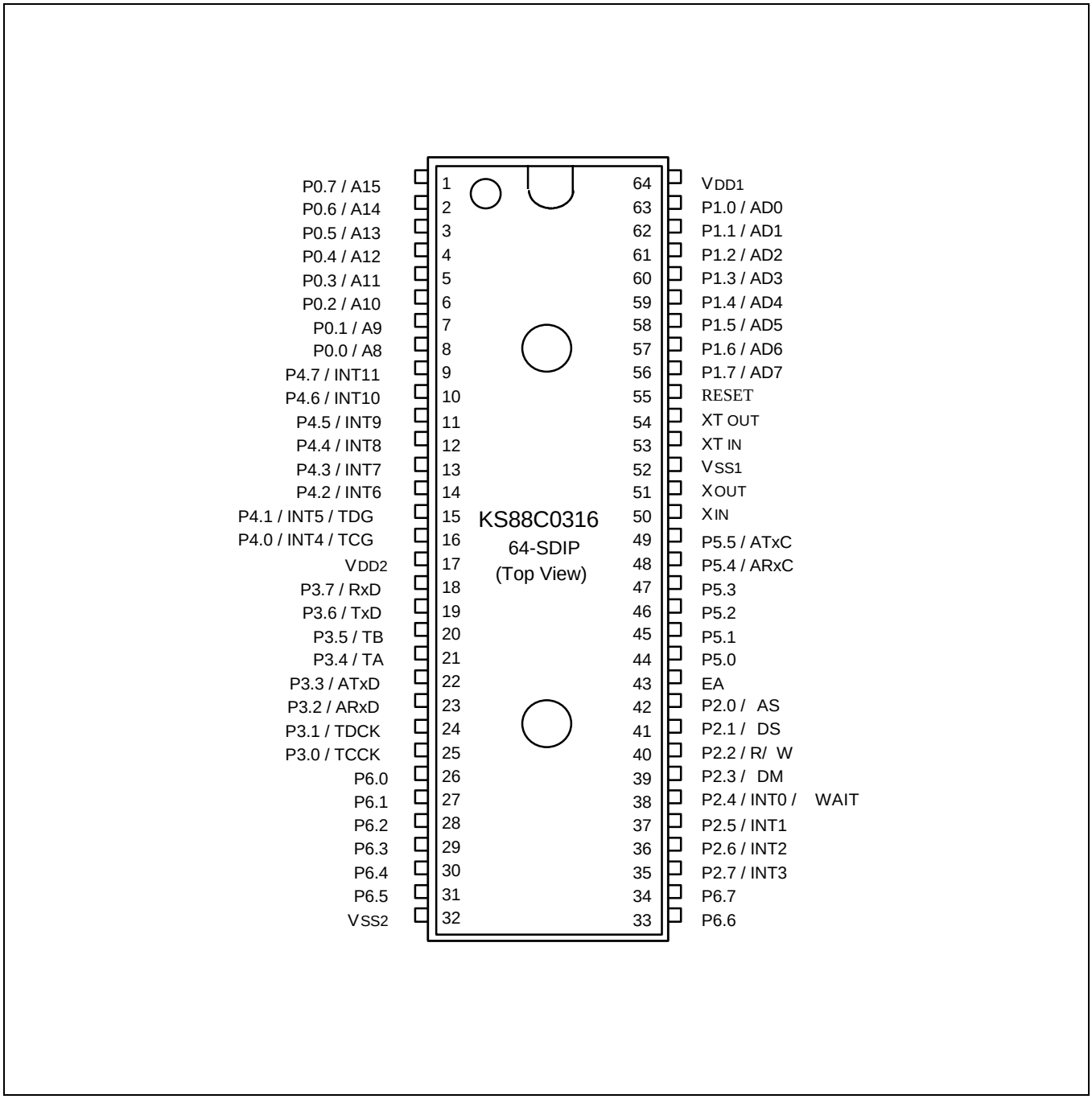

Figure 2. Pin Assignment Diagram (64-Pin SDIP Package)

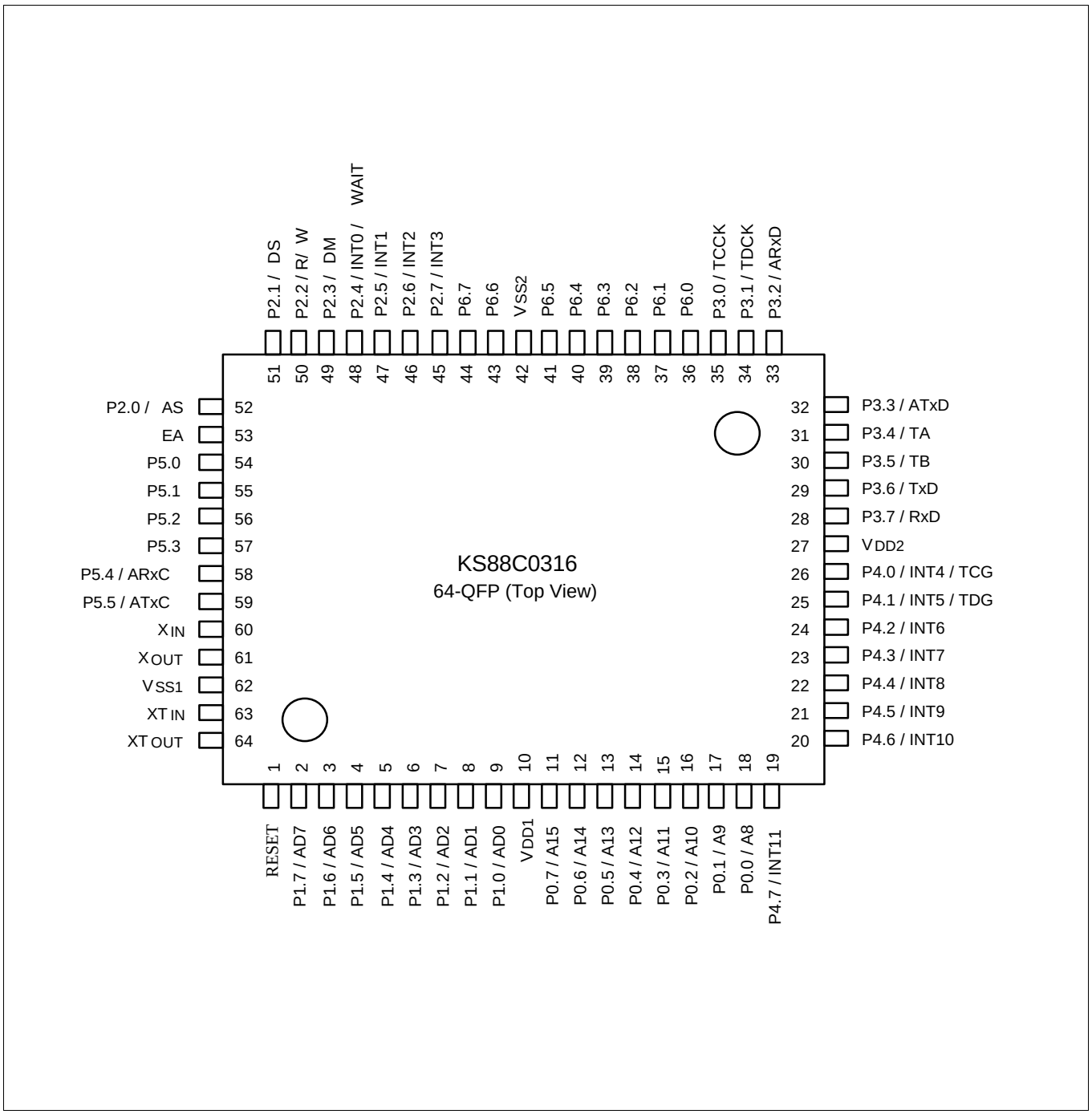

Figure 3. Pin Assignment Diagram (64-Pin QFP Package)

Table 1. KS88C0316 Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Number	SDIP Pin Number	Share Pins

P0.0–P0.7	I/O	Nibble-addressable I/O port for Schmitt trigger input or push-pull output. N-channel, open-drain, output mode and pull-up resistors are assignable by software. Port 0 can also be configured as external interface address lines A8–A15.	6	8–1	A8–A15
P1.0–P1.7	I/O	Same general characteristics as port 0. Port 1 can alternatively be used as external interface address/data lines AD0–AD7.	6	63–56	AD0–AD7
P2.0–P2.3 P2.4–P2.7	I/O	I/O port for Schmitt trigger input or push-pull output. P2.0–P2.3 can be configured for external bus control signals. Upper nibble pins P2.4–P2.7 are bit-programmable for external interrupts INT0–INT3. P2.4 can be used as a WAIT signal input for the external interface.	5 (lower nibble); 4 (upper nibble; with noise filter)	42–39; 38–35	AS, DS, DM, R/W; INT0–INT3, WAIT
P3.0–P3.7	I/O	I/O port with bit-programmable pins; Schmitt trigger input or push-pull output. Each port 3 pin has an alternative function: P3.0: TCCK (timer C clock input) P3.1: TDCK (timer D clock input) P3.2: ARxD (ADLC receiver data input) P3.3: ATxD (ADLC transmitter data output) P3.4: TA (timer A output) P3.5: TB (timer B output) P3.6: TxD (UART transmit) P3.7: RxD (UART receive) (ADLC and UART pins are multiplexed.)	5	25–18	(See pin description)
P4.0–P4.7	I/O	Bit-addressable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are software-assignable. Alternate functions include external interrupt inputs INT4–INT11 (with interrupt enable and pending control) and the timer C and timer D gate inputs at P4.0 and P4.1, respectively.	3 (with noise filter)	16–9	INT4–INT11; TCG, TDG
P5.0–P5.5	I/O	Nibble-addressable I/O port for Schmitt trigger input or push-pull output. N-channel, open-drain, output mode and pull-ups are assignable by software. P5.4 and P5.5 are alternatively used as ADLC receiver and transmitter clock input pins, respectively. (The ADLC control pins are multiplexed.)	6	44–49	ARxC ATxC
P6.0–P6.7	O	N-channel, open-drain output port with up to 9-volt load capacity	2	26–31, 33–34	–
X_{IN}, X_{OUT}	–	System clock input and output pins	–	50, 51	–
XT_{IN}, XT_{OUT}	–	Sub-oscillator clock pins for backup timer	–	53, 54	–

Table 1. KS88C0316 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Number	SDIP Pin Number	Share Pins
RESET	I	System reset pin (internal pull-up: 280 k)	1	55	–
EA	I	External access (EA) pin with three modes: 0 V: Normal operation (internal ROM) 5 V: ROM-less operation (external interface) 7 V to 10 V: Factory test mode	–	43	–
V_{DD2}, V_{SS2}	–	Power input pins for peripherals (external)	–	17, 32	–
V_{DD1}, V_{SS1}	–	Power input pins for CPU (internal)	–	64, 52	–

PIN CIRCUITS

Table 2. Pin Circuit Assignments for the KS88C0316

Circuit Number	Circuit Type	KS88C0316 Assignments
1	Input	RESET
2	Output	Port 6
3	I/O	Port 4
4	I/O	Port 2 (P2.4–P2.7 only)
5	I/O	Port 2 (P2.0–P2.3 only) and port 3
6	I/O	Ports 0, 1, and 5

NOTE: Diagrams of circuit types 1–6 are presented below.

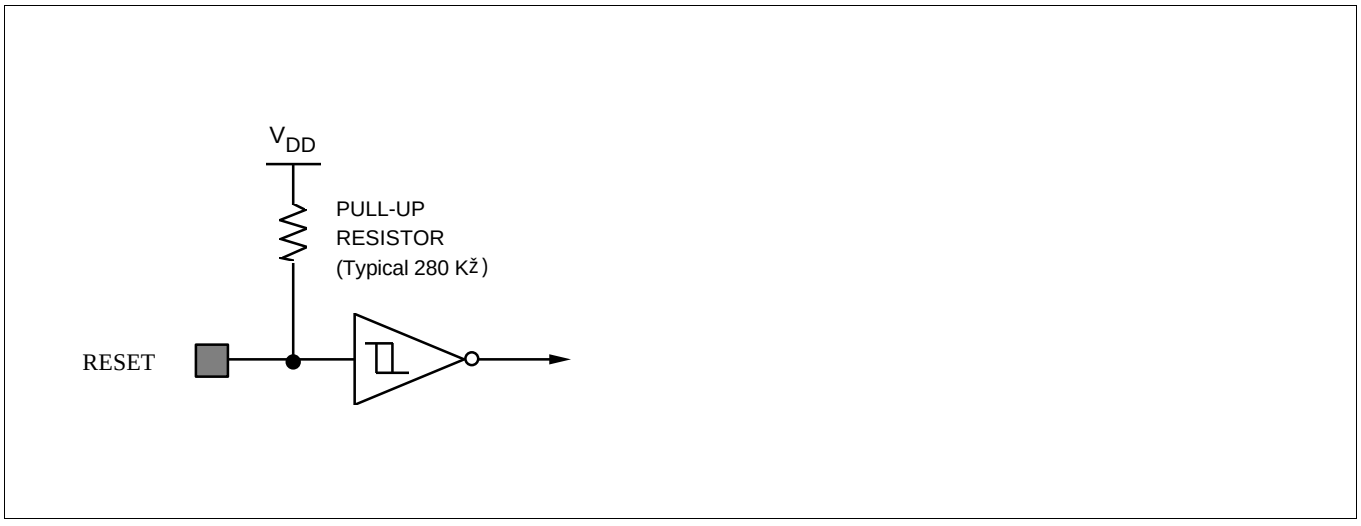

Figure 4. Pin Circuit Type 1 (RESET)