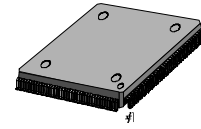


INTRODUCTION

KS7301B is a CMOS IC designed for the Digital Camcorder System. This Processor is Compatible with NTSC/PAL & the Hi-band/Normal Camcorder System.

160-QFP-2424



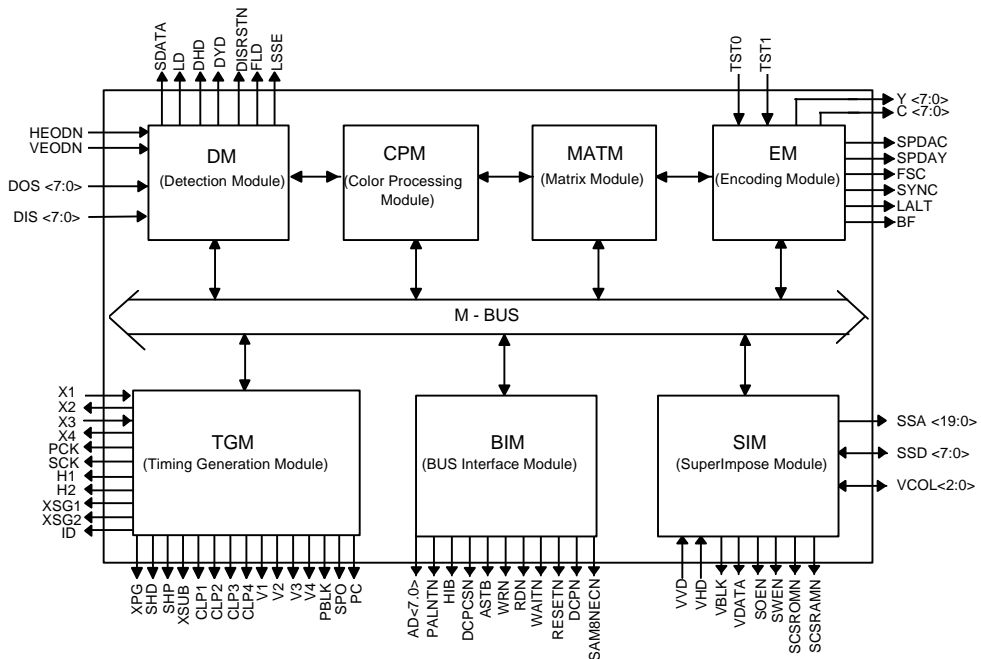
FEATURES

- Luminance & Chroma Signal Procession
- Built-in Timing Generator
- Built-in Sync. Generator
- Built-in Memory for Detection Part (6bit* 64 word*2 page)
- Built-in 1H delay line (1H *2, 8 bit *910)
- Built-in Encoder for PAL/NTSC
- Built-in DIS Interface Block
- Built-in Super Impose function
- Built-in Title Mix Block
- Compatible with NORMAL/Hi-band System
- Built in Micro Controller Interface Block

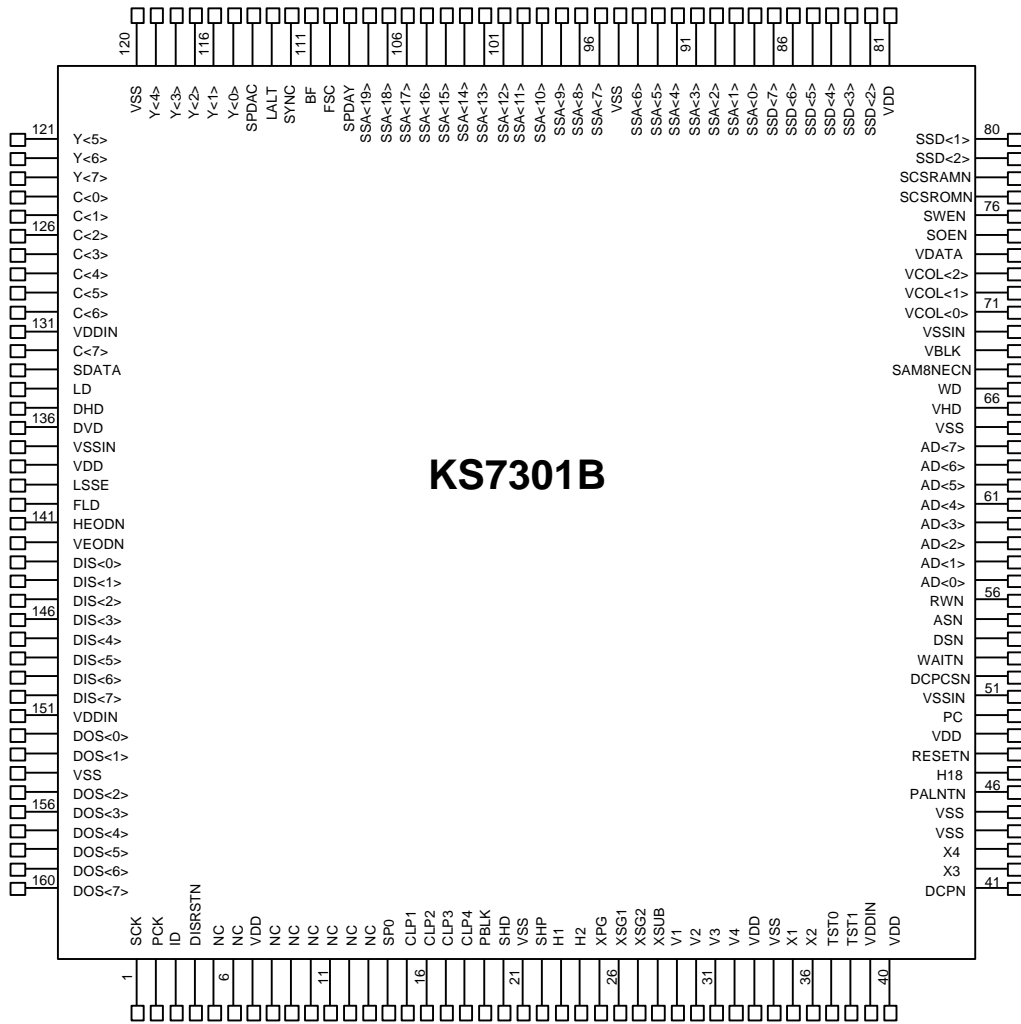
ORDERING INFORMATION

Device	Package	Operating Temperature
KS7301B	160-QFP-2424	-20°C ~ +75 °C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

No.	Symbol	I/O	Description	Remarks
1	SCK	O	Secondary Pipe Line clock (PCK/2)	
2	PCK	O	Main Pipe Line Clock	* 1
3	ID	O	CCD Line ID Signal	
4	DISRSTN	O	DZE Reset Signal (Active Low)	
5	NC	-	No connection	
6	NC	-	No connection	
7	VDD	-	I/O Power supply	
8	NC	-	No connection	
9	NC	-	No connection	
10	NC	-	No connection	
11	NC	-	No connection	
12	NC	-	No connection	
13	NC	-	No connection	
14	SP0	O	A/D Converter Sampling Clock	
15	CLP1	O	Clamp Pulse 1	
16	CLP2	O	Clamp Pulse 2	
17	CLP3	O	Clamp Pulse 3	
18	CLP4	O	Clamp Pulse 4	
19	PBLK	O	Video Pre - Blanking Pulse	
20	SHD	O	Data Sample & Hold Pulse For CDS	
21	VSS	-	Ground	
22	SHP	O	Pre-Charge Sample & Hold Pulse For CDS	
23	H1	O	Horizontal Driving Pulse 1 For CCD	
24	H2	O	Horizontal Driving Pulse 2 For CCD	
25	XPG	O	Pre-Charge Gate Pulse For CCD	
26	XSG1	O	Read Out Pulse 1 For CCD	
27	XSG2	O	Read Out Pulse 2 For CCD	
28	XSUB	O	Discharge Pulse For CCD	
29	V1	O	Vertical Driving Pulse 1 For CCD	
30	V2	O	Vertical Driving Pulse 2 For CCD	
31	V3	O	Vertical Driving Pulse 3 For CCD	
32	V4	-	Vertical Driving Pulse 4 For CCD	
33	VDD	-	I/O Power Supply	
34	VSS	-	Ground	
35	X1	I	Main X-tal Input	*2
36	X2	O	Main X-tal Output	
37	TST0	I	IC Test pin	*3
38	TST1	I	IC Test pin	*3
39	VDDIN	-	Power Supply (INTERNAL)	
40	VDD	I	Power Supply For X - tal	

PIN DESCRIPTION (Continued)

No.	Symbol	I/O	Description	Remarks
41	DCPN	I	IC Test Pin	*3
42	X3	I	4Fsc X - tal Input For PAL (17.73447MHz)	
43	X4	O	4Fsc X - tal Output For PAL	
44	Vss	-	Ground X - tal	
45	Vss	-	Ground	
46	PALNTN	I	PAL/NTSC Mode Select ion Pin	
47	HI8	I	760H/510H CCD Mode Selection Pin	
48	RESETN	I	IC Reset Input	
49	V _{DD}	-	I/O Power Supply	
50	PC	O	Phase Comparator Output Of PAL PLL	*4
51	VSSIN	-	Ground (INTRENAL)	
52	DCPCSN	I	DCP Chip Select Pin (Low Active)	
53	WAITN	O	Wait For Micom Interface (Low Active)	
54	DSN(RDN)	I		*5
55	ASN(AS)	I		*6
56	RWN	I		*7
57	AD<0>	I/O	Micro controller Address / Data Bus I / O	
58	AD<1>	I/O		
59	AD<2>	I/O		
60	AD<3>	I/O		
61	AD<4>	I/O		
62	AD<5>	I/O		
63	AD<6>	I/O		
64	AD<7>	I/O		
65	VSS	-	Ground	
66	VHD	I	VCR Part HD Pulse (VCR PB Mode Title Mix)	
67	VVD	I	VCR Part VD Pulse (VCR PB Mode Title Mix)	
68	SAM8NECH	I	Microcontroller Type Select Pin (SAM8:High, NEC:Low)	
69	VBLK	O	Title Blank Signal For VCR PB Mode Title Mix	
70	VSSIN	-	Ground (INTERNAL)	
71	VCOL<0>	O	Title Color Signal For VCR PB Mode Title Mix	
72	VCOL<1>	O		
73	VCOL<2>	O		
74	VDATA	O	Title Data Enable Signal For VCR PB Mode Title Mix	
75	SOEN	O	ROM Enable For Superimpose (Low Active)	
76	SWEN	O	RAM Enable For Superimpose (Low Active)	
77	SCSROMN	O	ROM Chip Select For Superimpose (Low Active)	
78	SCSRAMN	O	RAM Chip Select For Superimpose (Low Active)	
79	SSD<0>	I/O	Memory Interface Data I/O For Superimpose	
80	SSD<1>	I/O		

PIN DESCRIPTION (Continued)

No.	Symbol	I/O	Description	Remarks
81	VDD	-	Power supply For I/O	
82	SSD<2>	I/O	Memory Interface Data I/O For Superimpose	
83	SSD<3>	I/O		
84	SSD<4>	I/O		
85	SSD<5>	I/O		
86	SSD<6>	I/O		
87	SSD<7>	I/O		
88	SSA<0>	O	Memory Interface Address Output For Superimpose	
89	SSA<1>	O		
90	SSA<2>	O		
91	SSA<3>	O		
92	SSA<4>	O		
93	SSA<5>	O		
94	SSA<6>	O		
95	VSS	-	Ground	
96	SSA<7>	O	Memory Interface Address Output For Superimpose	
97	SSA<8>	O		
98	SSA<9>	O		
99	SSA<10>	O		
100	SSA<11>	O		
101	SSA<12>	O	Memory Interface Address Output For Superimpose	
102	SSA<13>	O		
103	SSA<14>	O		
104	SSA<15>	O		
105	SSA<16>	O		
106	SSA<17>	O		
107	SSA<18>	O		
108	SSA<19>	O		
109	SPDAY	O	D/A Converter Sampling Clock For Y Signal (PCK)	
110	FSC	O	Chroma Subcarrier (NTSC : 3.7595 MHz, PAL : 4.4336 MHz)	
111	BF	O	Burst Flag Pulse	
112	SYNC	O	Video Composite SYNC signal	
113	LALT	O	Line Alternate Pulse For PAL	
114	SPDAC	O	D/A Converter Sampling Clock for C Signal (4Fsc)	
115	Y<0>	O	Y Video Signal Output	
116	Y<1>	O		
117	Y<2>	O		
118	Y<3>	O		
119	Y<4>	O		
120	VSS	-	Ground	

PIN DESCRIPTION (Continued)

No.	Symbol	I/O	Description	Remarks
121	Y<5>	O	Y Video Signal Output	
122	Y<6>	O		
123	Y<7>	O		
124	C<0>	O	C Video Signal Output	
125	C<1>	O		
126	C<2>	O		
127	C<3>	O		
128	C<4>	O		
129	C<5>	O		
130	C<6>	O		
131	VDDIN	-	Power supply (INTERNAL)	
132	C<7>	O	C Video Signal Output	
133	SDATA	O	DZE Interface Serial Data	
134	LD	O	DZE Interface Load Signal	
135	DHD	O	HD signal for DIS	
136	DVD	O	VD signal for DIS	
137	V _{SSIN}	-	Ground (INTERNAL)	
138	VDD	-	Power supply For I/O	
139	LSSE	O	Low Shutter Speed Enable	
140	FLD	O	Video Field Signal	
141	HEODN	I	Chroma S1, S2 Pixel Control (Default : High)	
142	VEODN	I	Chroma 2R-G, G-2B Line Control (Default : High)	
143	DIS<0>	I/O	CCD Video Input Signal	
144	DIS<1>	I/O		
145	DIS<2>	I/O		
146	DIS<3>	I/O		
147	DIS<4>	I/O		
148	DIS<5>	I/O		
149	DIS<6>	I/O		
150	DIS<7>	I/O		
151	V _{DDIN}	-	Power supply (INTERNAL)	
152	DOS<0>	I	DZE Video Input Signal	
153	DOS<1>	I		
154	V _{SS}	-	Ground	
155	DOS<2>	I	DZE Video Input Signal	
156	DOS<3>	I		
157	DOS<4>	I		
158	DOS<5>	I		
159	DOS<6>	I		
160	DOS<7>	I		

< REMARKS >

- *1. Main Pipe Line Clock
510H: NTSC 1820/3 fh, PAL 18
760H:NTSC 910 fh, PAL 908 fh

- *2. Main X-tal Input
NTSC:28.63636 MHz, PAL:28,375 Mhz

- *3. IC Test Pin (TST1, TST0, DCPN)
(0,0,0) : TEST (CPM)
(0,0,1) : TEST (MATM)
(0,1,0) : TEST (TGM)
(0,1,1) : TEST (SIM)
(1,0,0) : TEST (DC LOW)
(1,0,1) : TEST (DC HIGH)
(1,1,0) : NORMAL
(1,1,1) : RESERVED

- *4. Phase Comparator Output Of PAL PLL
Include Charge Pump Part

- *5. SAM 8 Mode : Data Strobe Signal Input (Low Active)
NEC Mode : Read Enable (Low Active)

- *6. Address Strobe For Micom Interface
SAM 8 : Low Active, NEC : High Active

- *7. SAM 8 Mode : Read / Write Enable (Read : High, Write : Low)
NEC Mode : Write Enable (Low Active)

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V _{DD}	-0.5~6.5	V
Input Voltage	V _{IN}	-0.5~V _{DD} +0.5	V
Output Voltage	V _{OUT}	-0.5~V _{DD} +0.5	V
Power Dissipation	P _D	1	W
Operating Temperature	T _{OPR}	-20~+75	°C
Storage Temperature	T _{STG}	-65~+150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC}=5V, Ta = 25 °C, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit	Remark
Supply Voltage	V _{DD}	-	4.5	5.0	5.5	V	
Input Leakage Current	I _U	-	-	-	1	uA	
Output Leakage Current	I _{LO}	-	-	-	1	uA	
Operating Current	I _{CC}	V _{DD} =5V	-	140	180	mA	
High-Level Input Voltage	V _{IH}	-	0.8V _{DD}	-	V _{DD}	V	
Low-Level Input Voltage	V _{IL}	-	0	-	0.2V _{DD}	V	
Output High Voltage 1	V _{OH1}	I _{OH} =-2mA	V _{DD} -0.5	-	-	V	*1
Output Low Voltage 1	V _{OL1}	I _{OL} =4mA	-	-	0.45	V	*1
*Output High Voltage 2	V _{OH2}	I _{OH} =-4mA	V _{DD} -0.5	-	-	V	*2
*Output Low Voltage 2	V _{OL2}	I _{OL} =8mA	-	-	0.45	V	*2
**Output High Voltage 3	V _{OH3}	I _{OH} =-8mA	V _{DD} -0.5	-	-	V	*3
**Output Low Voltage 3	V _{OL3}	I _{OL} =8mA	-	-	0.45	V	*3

*: XPG, SHP, SHD Pulse

** :H1, H2 Pulse

*1 : IO=2mA

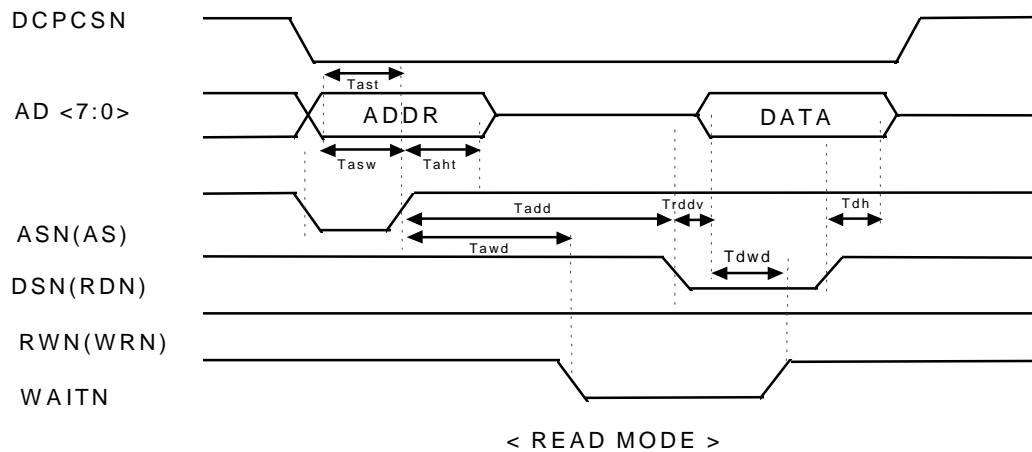
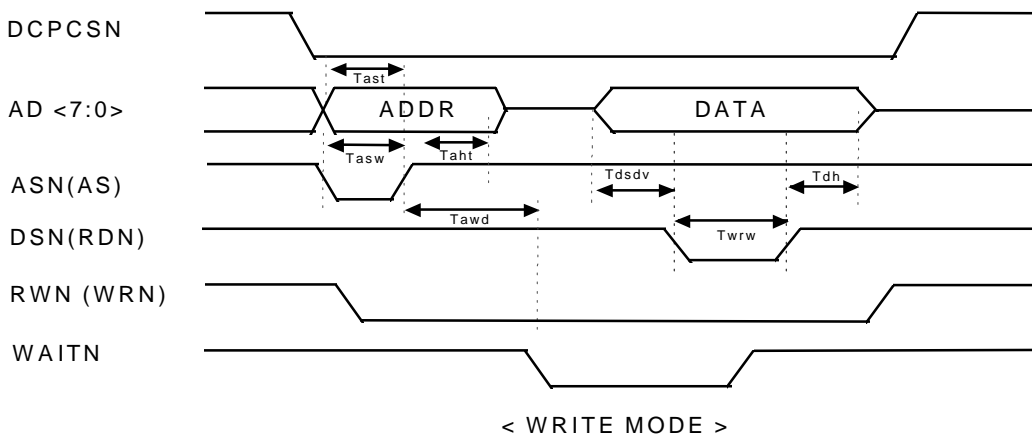
*2 : IO=4mA

*3 : IO=8mA

Micro controller Interface I : for SAM8 (PIN68A → HIGH)

Characteristics	Symbol	Min	Typ	Max	Unit	Remarks
Address setup time	Tast	15	-	-	nsec	-
Address hold time	Taht	35	-	-	nsec	-
ASTB pulse width	Tasw	35	-	-	nsec	-
ASTB, WAITN distance	Tawd	-	-	35	nsec	-
DSN delay from Data	Tdsdv	35	-	-	nsec	Write
WRN width	Twrw	400	-	-	nsec	-
Data hold time	Tdh	0	-	-	nsec	-
Data delay from DSN	Trdrv	-	-	270	nsec	Read
Data, WAITN distance	Tdwd	35	-	-	nsec	-
ASN, DSN distance	Tadd	-	-	140	nsec	Read

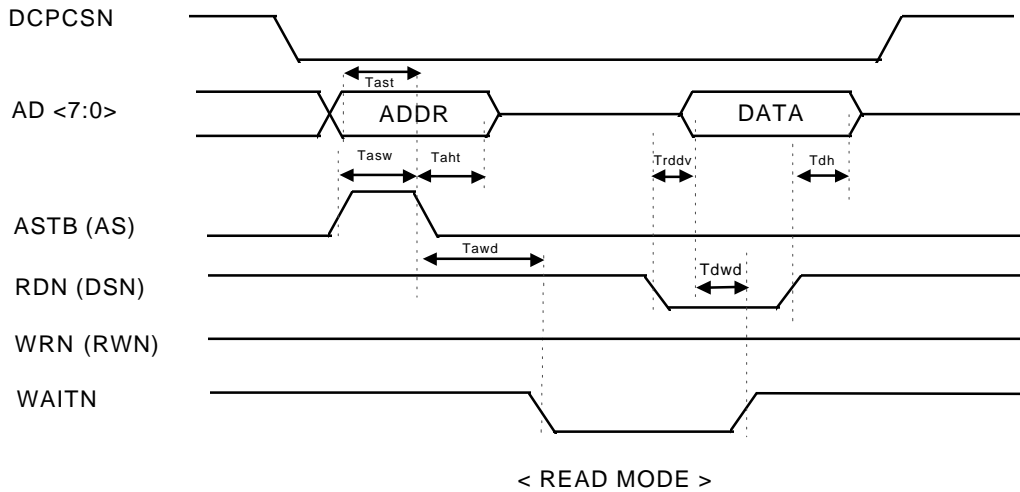
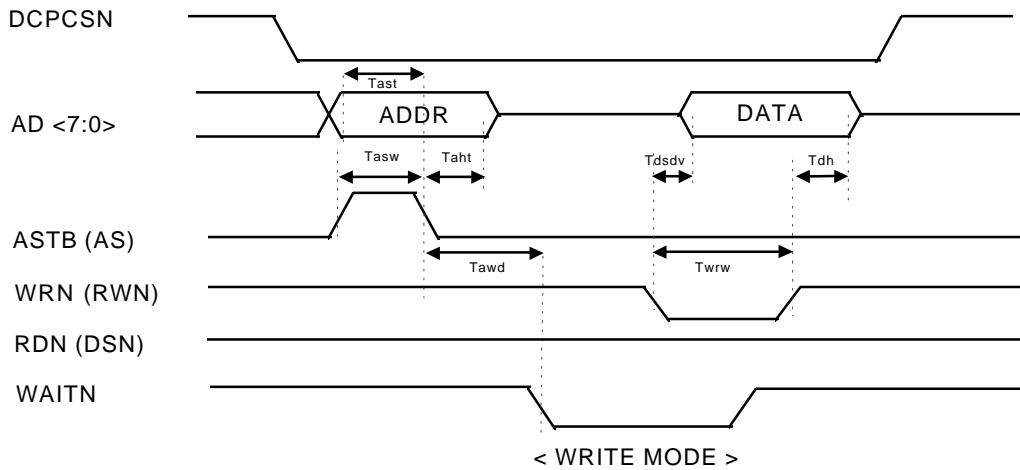
Timing Chart for Micro controller Interface I : for SAM8 (PIN68 → HIGH)



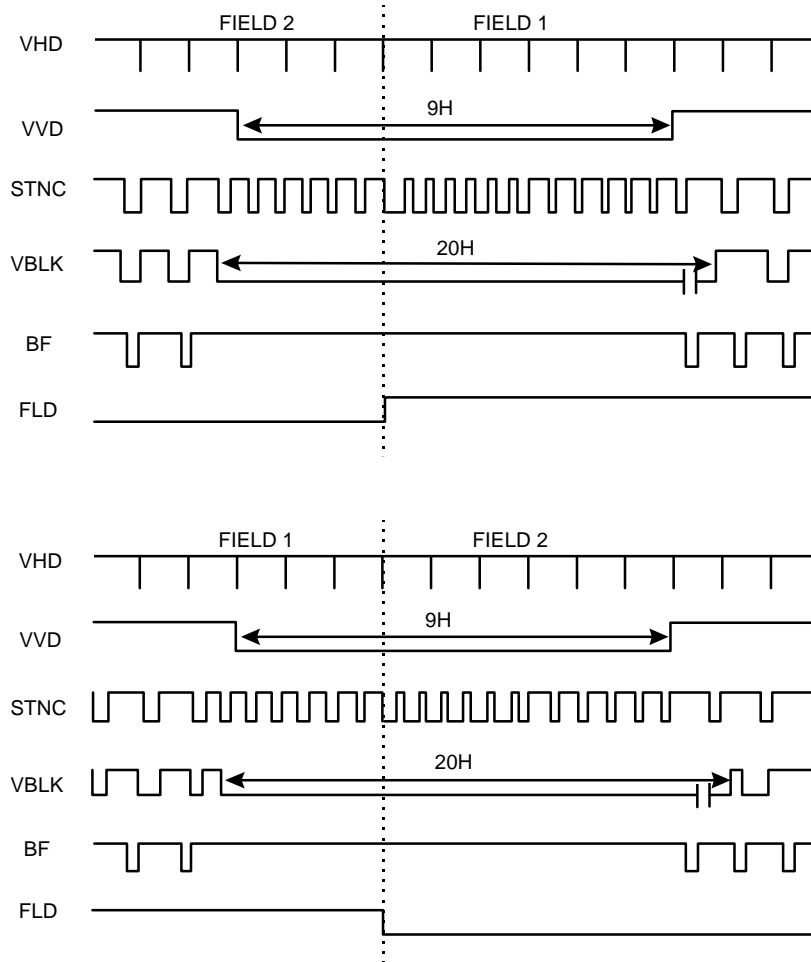
Micro controller Interface II: for NEC (PIN68 → LOW)

Characteristics	Symbol	Min	Typ	Max	Unit	Remarks
Address setup time	Tast	15	-	-	nsec	-
Address hold time	Taht	35	-	-	nsec	-
ASTB pulse width	Tasw	35	-	-	nsec	-
ASTB, WAITN distance	Tawd	-	-	35	nsec	-
DSN delay from DSN	Tdsdy	35	-	100	nsec	Write
WRN width	Twrw	400	-	-	nsec	-
Data hold time	Tdh	0	-	-	nsec	-
Data delay from RDN	Trdrv	-	-	270	nsec	Read
Data, WAITN distance	Tdwd	35	-	-	nsec	-
ASN, DSN distance	Tadd	-	-	140	nsec	Read

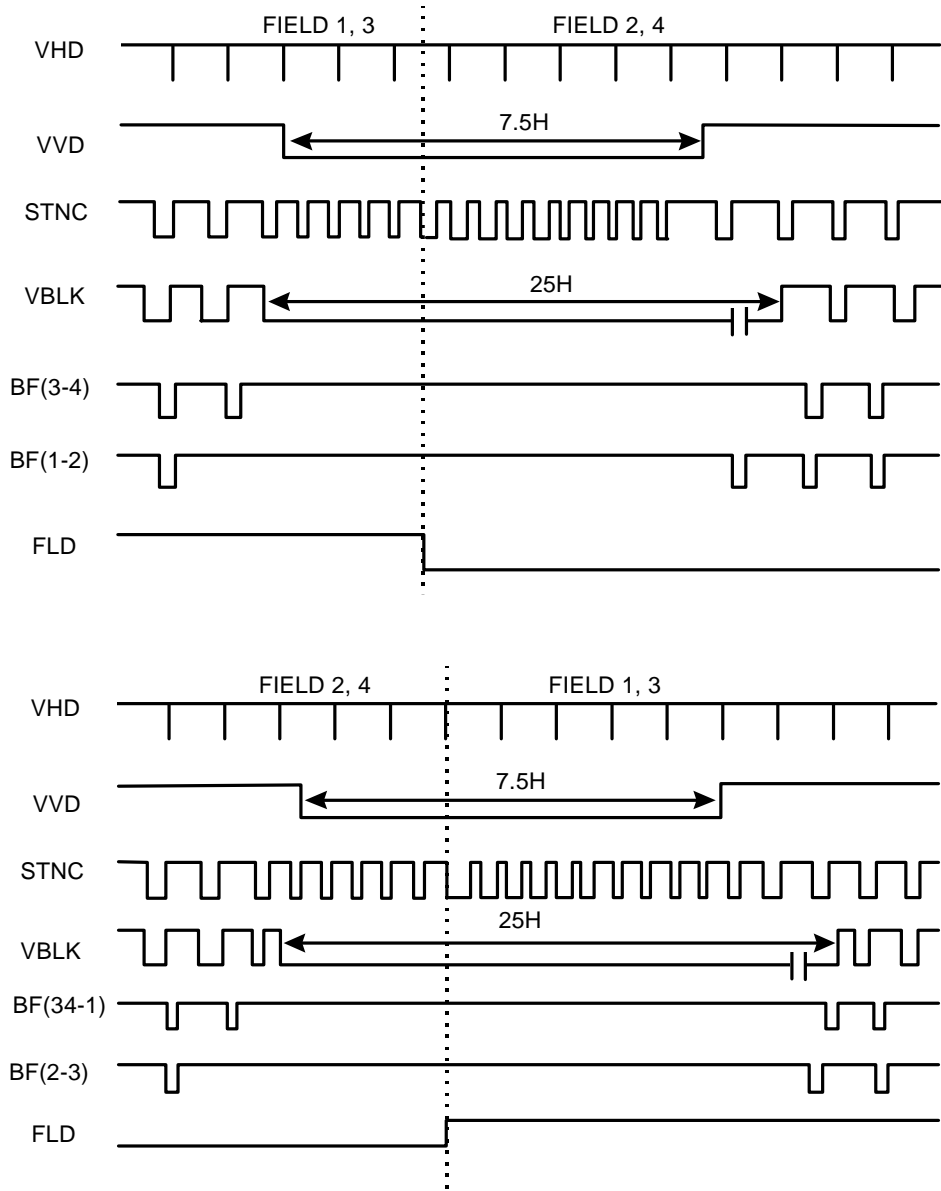
Timing Chart for Micro controller Interface II : for NEC (PIN68 → LOW)



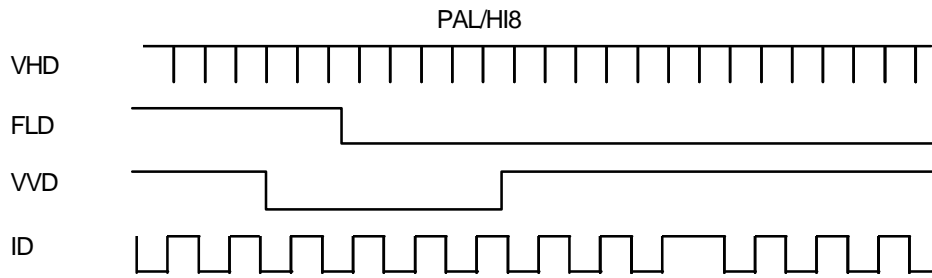
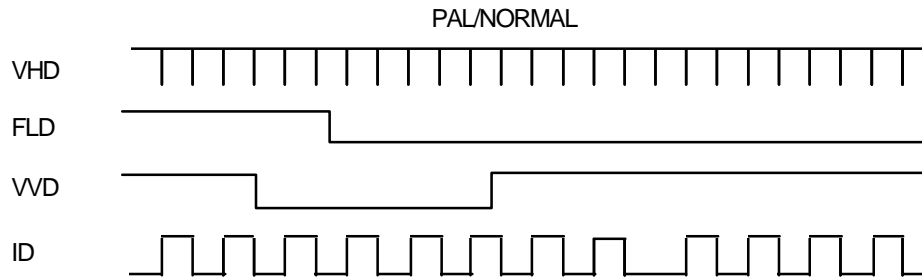
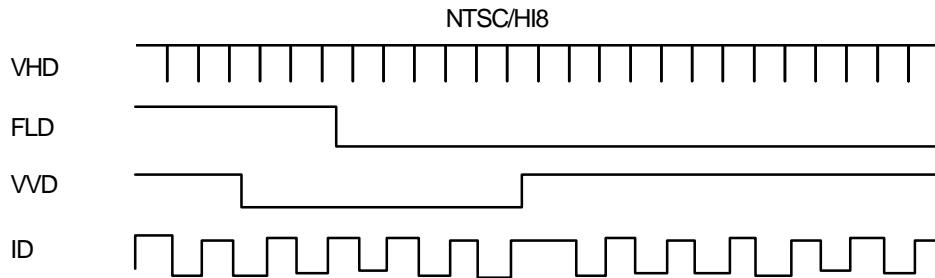
Vertical Timing for SYNC signal
(1) NTSC



(2) PAL

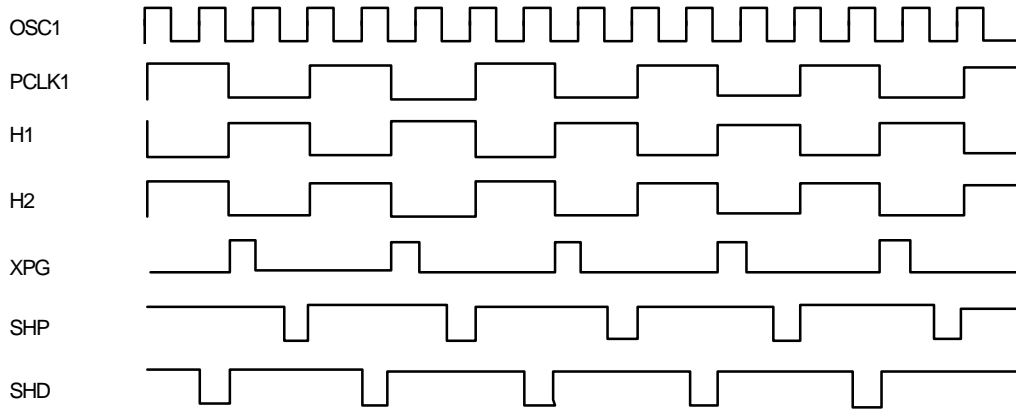


ID

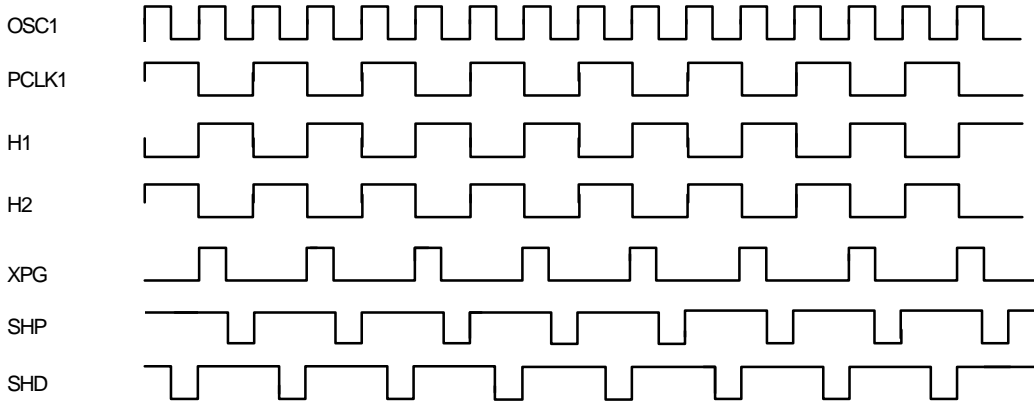


SHP, SHD, H1, H2

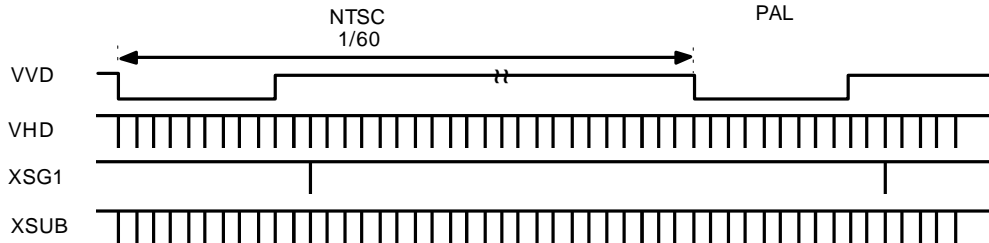
NTSC/NORMAL



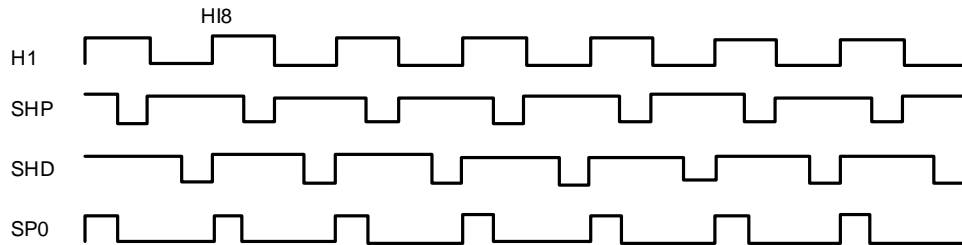
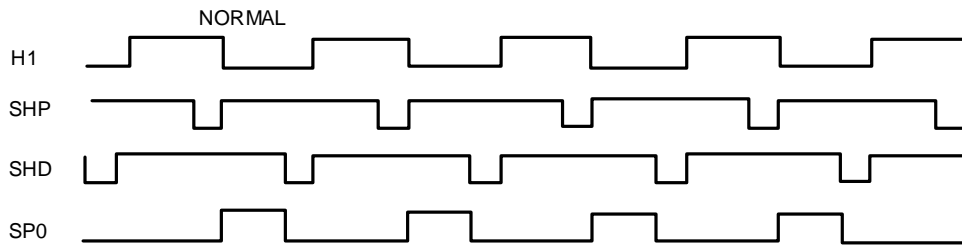
NTSC / HI8



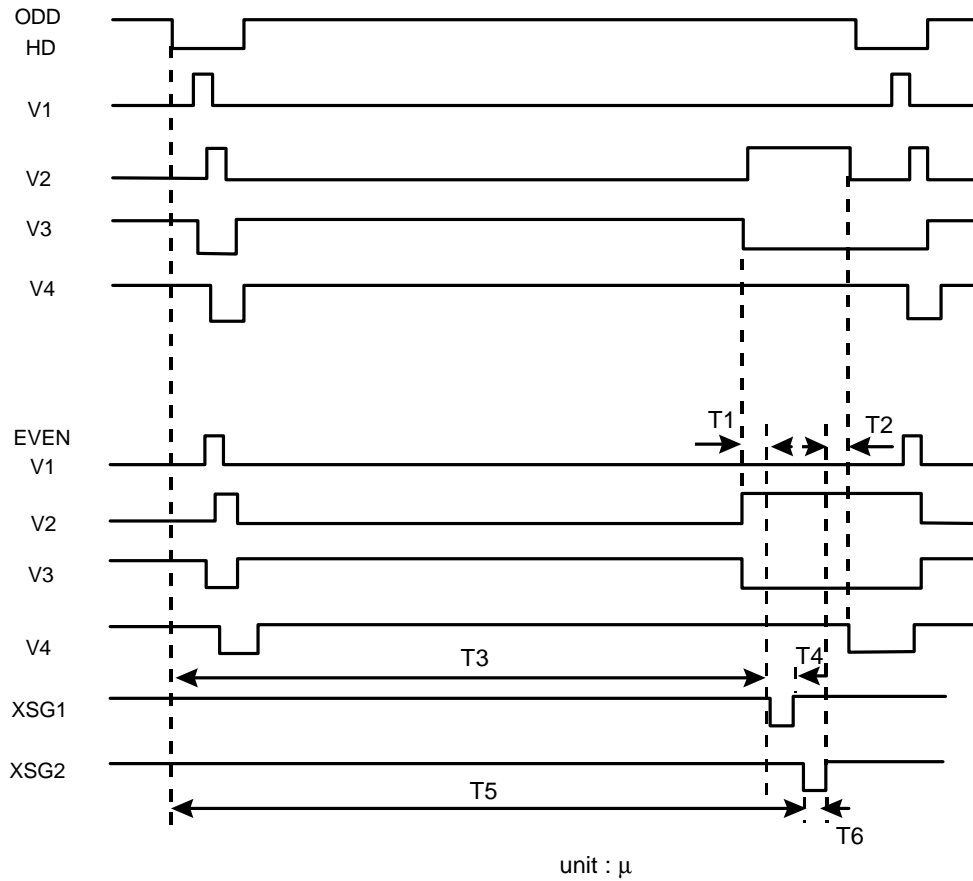
XSUB (1 / 10000 sec Low Shutter Speed Mode)



SP0

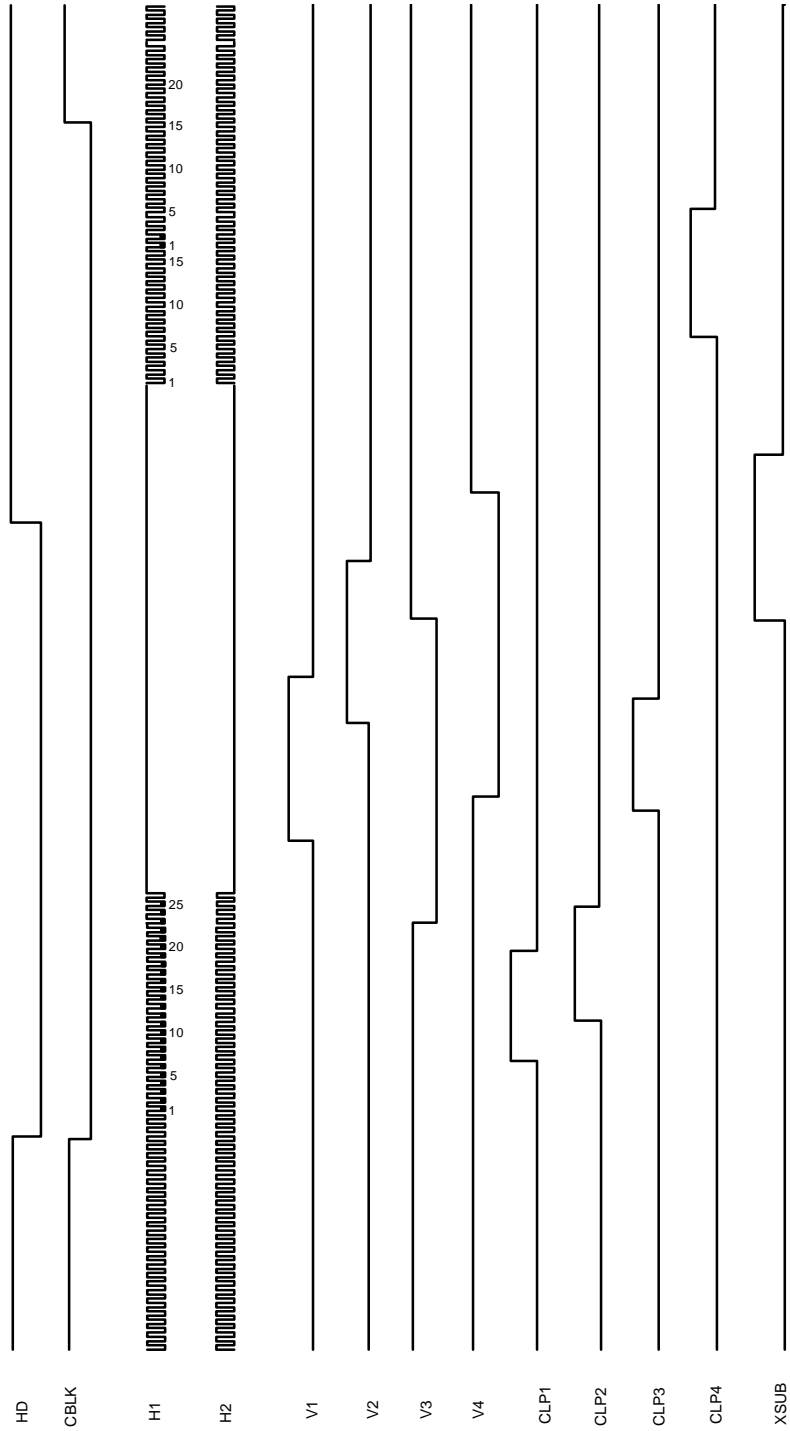


Horizontal Timing of V1 - V4, XSG1, XSG2

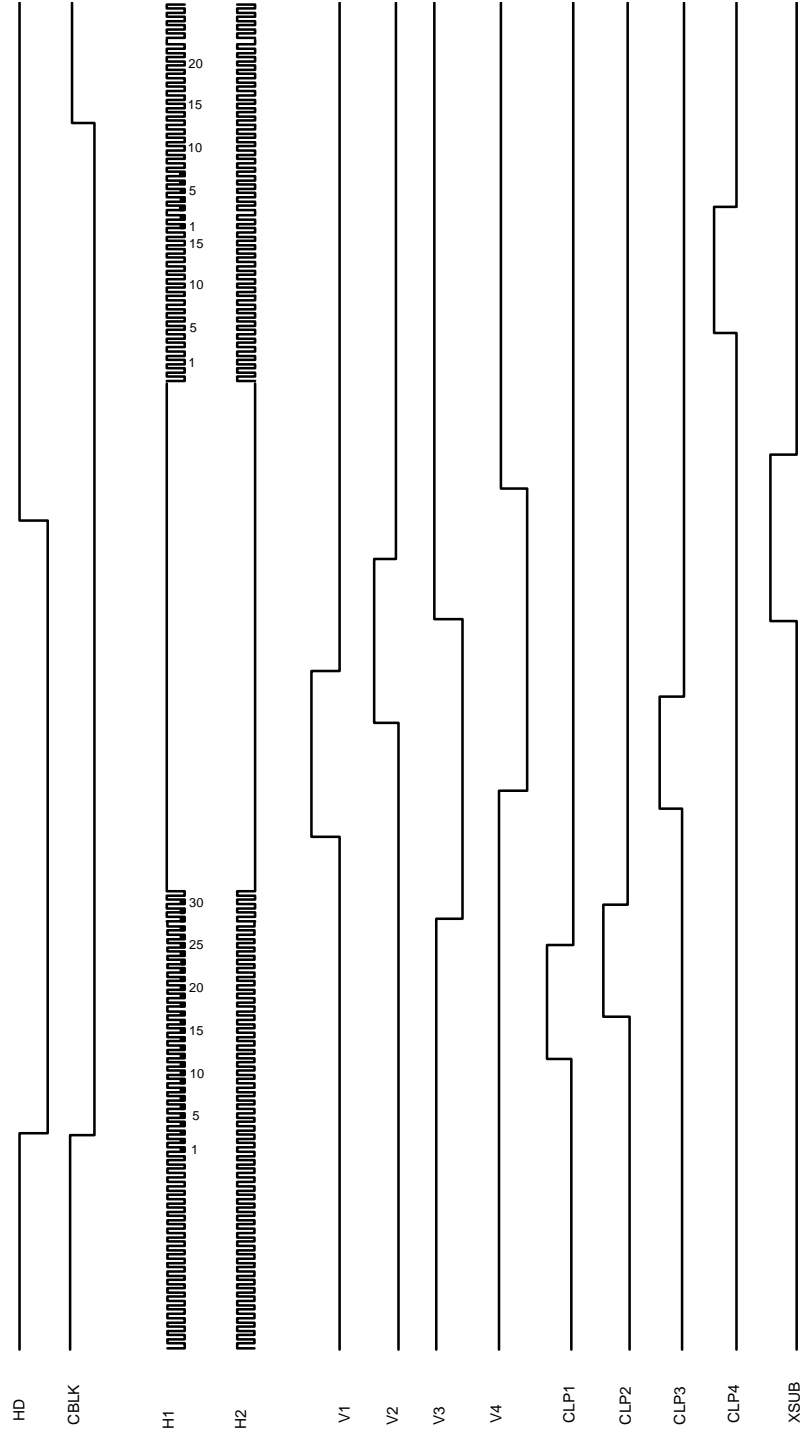


	Normal	Hi18
T1	1.1	1.6
T2	2	2.5
T3	39.5	42.2
T4	2.5	2.5
T5	43.5	47.2
T6	2.5	2.5

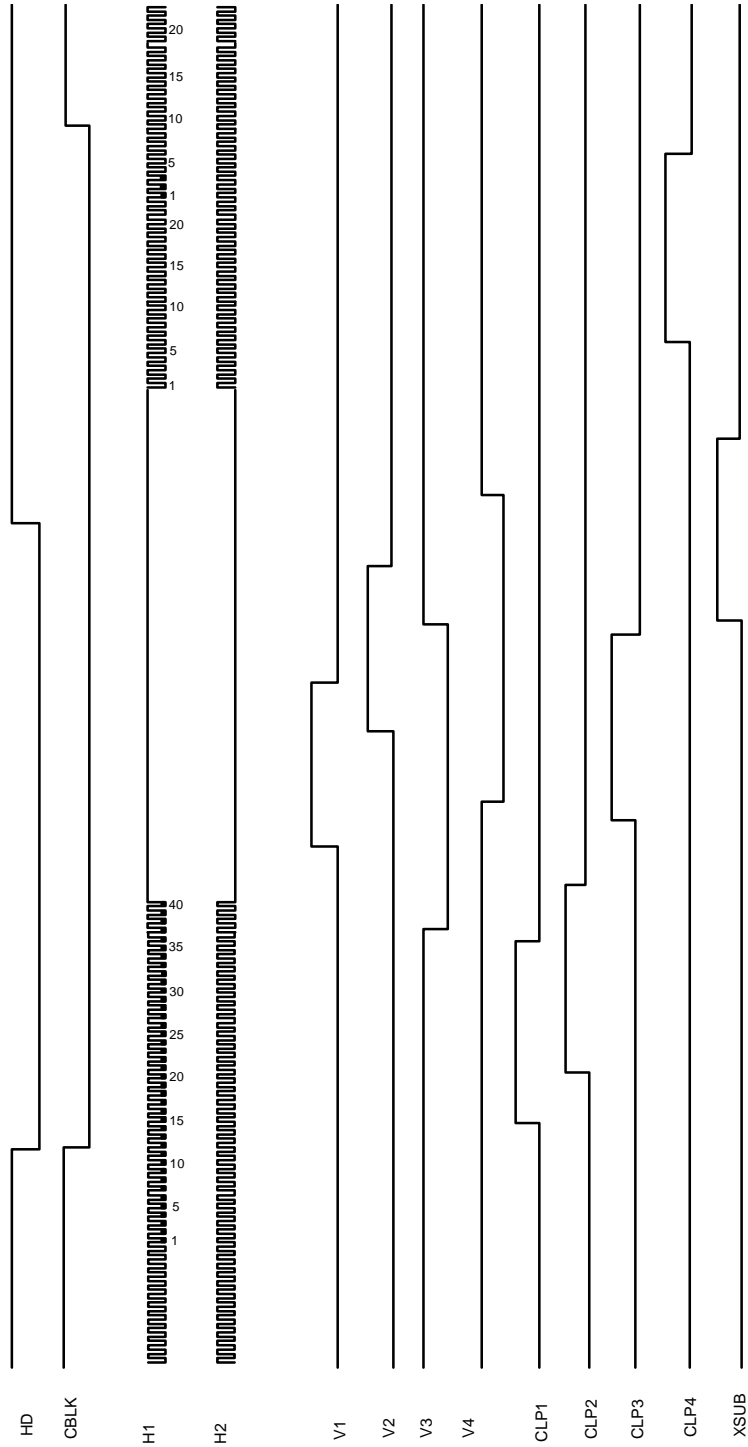
Horizontal Timing For CCD (NTSC/NORMAL)



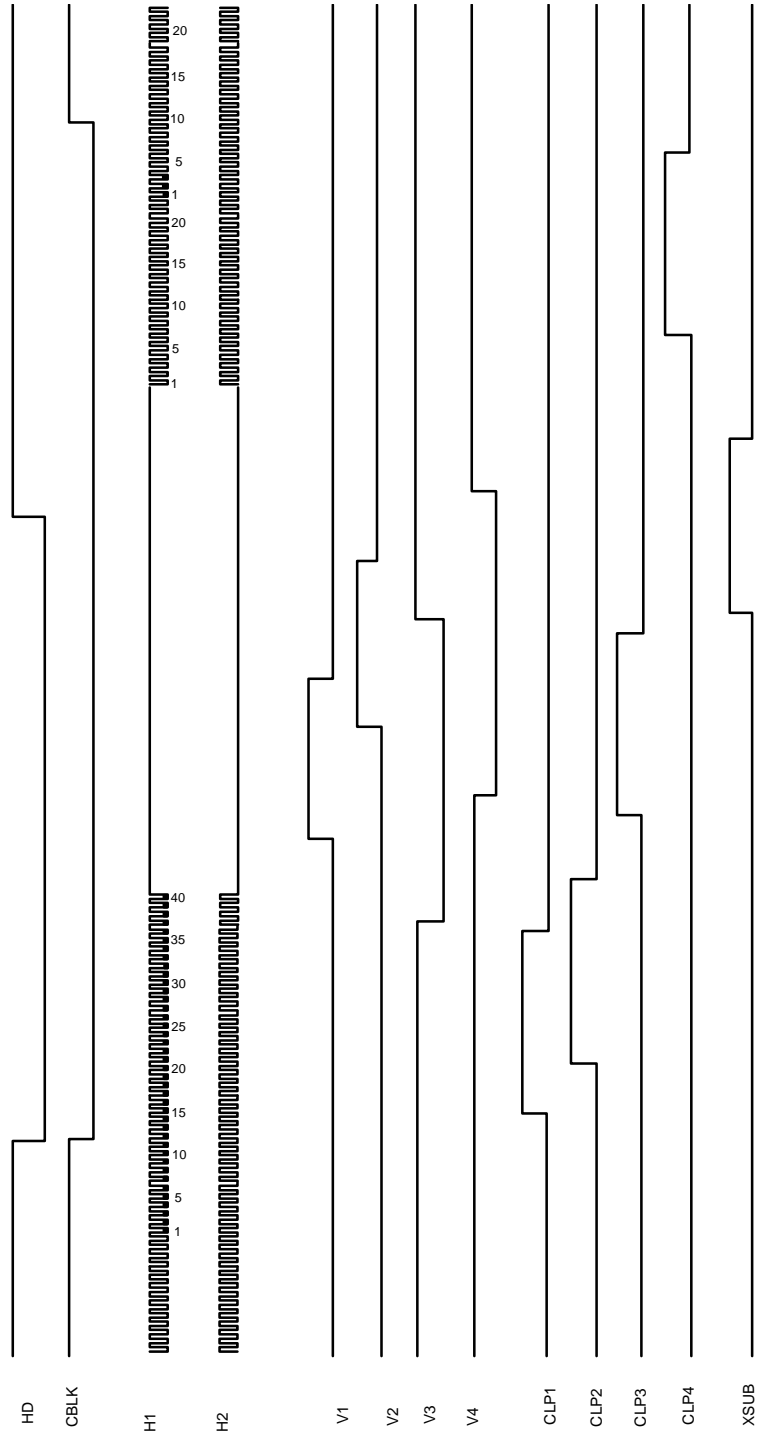
Horizontal Timing For CCD (PAL/NORMAL)



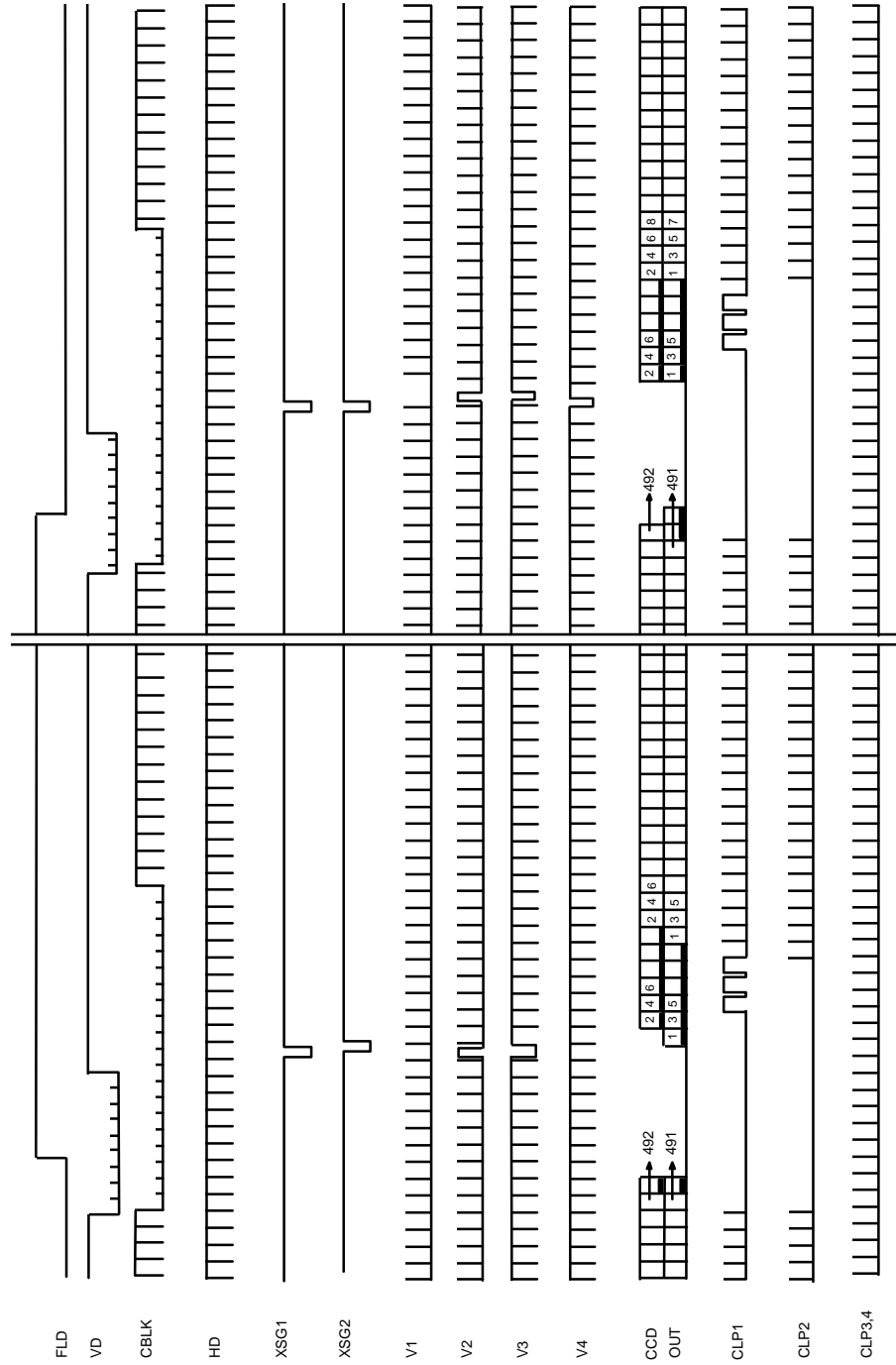
Horizontal Timing For CCD (NTSC/H18)



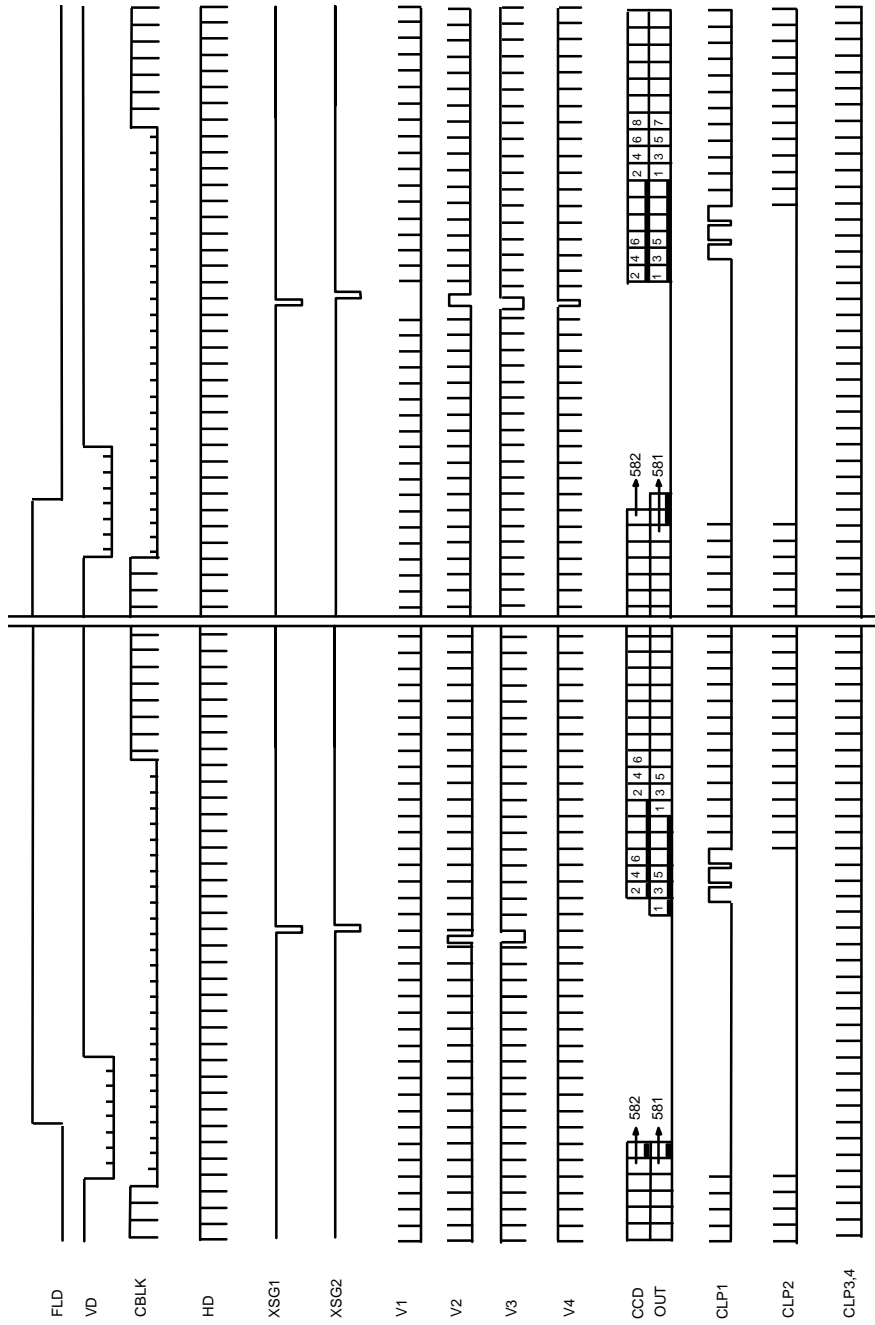
Horizontal Timing For CCD (PAL/Hi8)



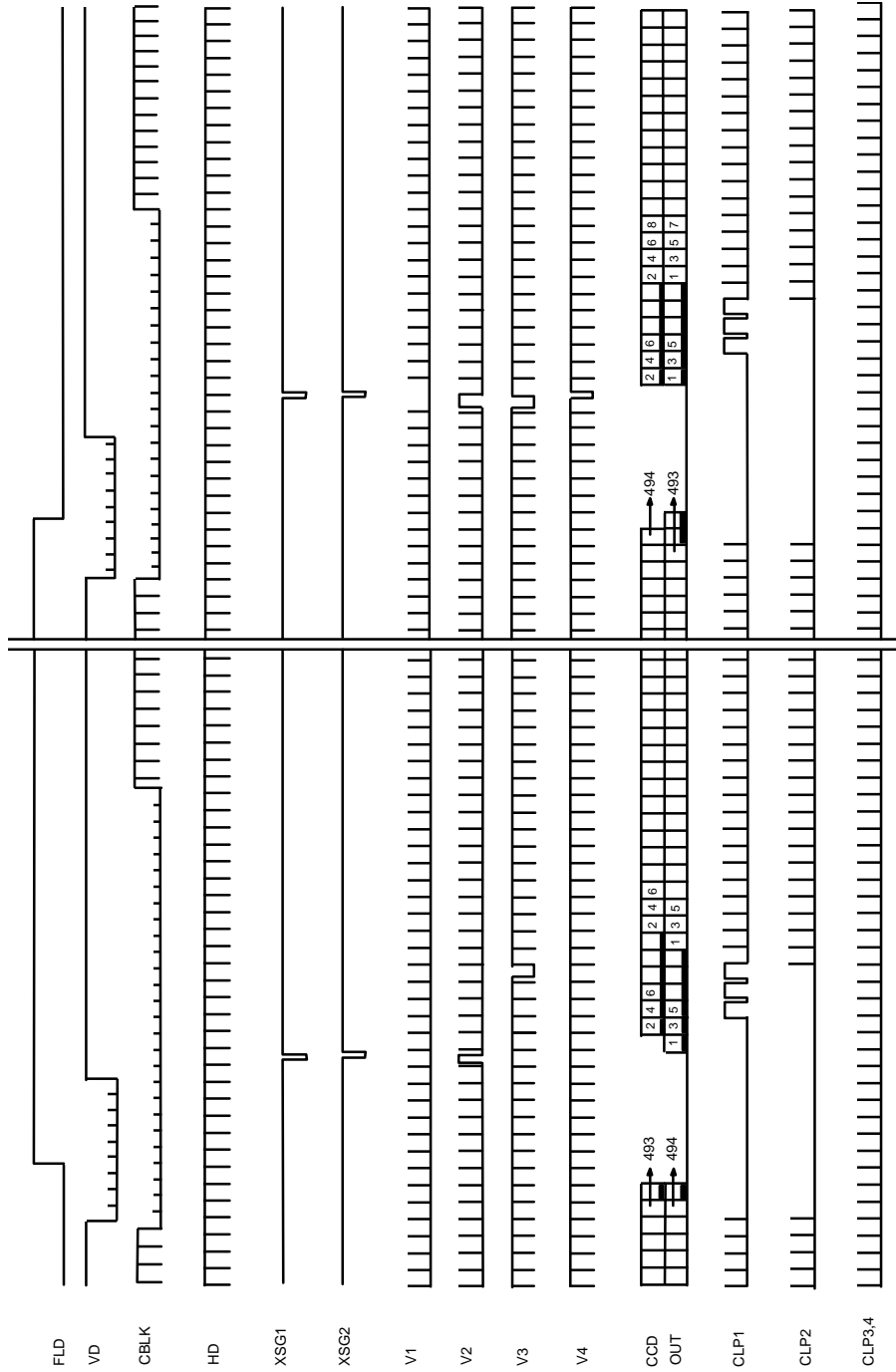
Vertical Timing For CCD (NTSC/NORMAL)



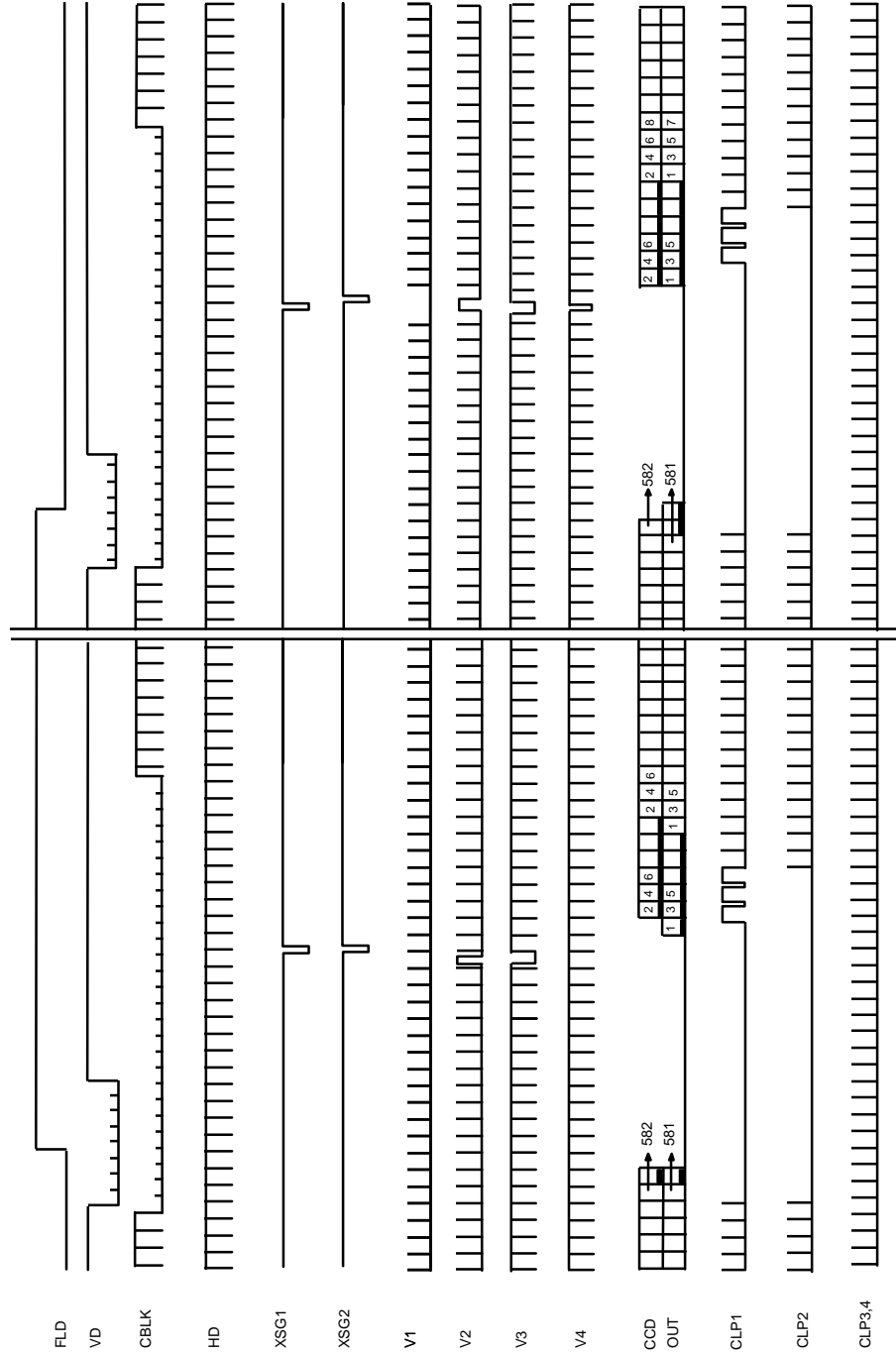
Vertical Timing For CCD (PAL/NORMAL)



Vertical Timing For CCD (NTSC/H18)



Vertical Timing For CCD (PAL/Hi8)



REGISTER MAPPING

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION
BST	00	3	RD	DCP Status Register
DADR	20	6	WR	Detection RAM Address Pointing Register When the start point is assigned, the address increases by one automatically. To read the first small picture, set the Address value to 00(HEX) (LSB 6 bit using)
DMDL	21	8	R/W	Detection Data Register
DMDH	22	8	R/W	In read cycle, the detection data is output in the order of DMDH -> DMDL Register.
DCMD	23	8	WR	Command Register

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION						
DDIS	27	8	WR	DZE Mode Control Register						
COV1	40	8	WR	Knee Delta Coeff. Register (Default : Hex 00) Range : 0 ~ 255(FF)						
COV2	41	8	WR	Knee Coeff. Register (Half value of Knee Point) Range : 0 ~ 255(FF)						
CAG	42	8	WR	Aperture Gain Register Range : 0 ~ 255(FF)						
CCOA	43	8	WR	Color Coeff.1 Register (Default : 0.12) Range : 0 ~ 6dB(FF)						
CCOB	44	8	WR	Color Coeff.2 Register (Default : 0.2) Range : 0 ~ 6dB(FF)						
CAKP	45	8	WR	Knee Point Value Range : 0 ~ 255(FF)						
CNSL	46	8	WR	Aperture Noise Slice Level Range : 0 ~ 255(FF)						
CAPS	47	7	WR	Edge Chroma Suppress <div style="text-align: center;"> <table border="1" style="margin: auto;"> <tr> <td style="width: 15px;">7</td> <td style="width: 20px;">6-5</td> <td style="width: 20px;">4-0</td> </tr> <tr> <td style="text-align: center;">-</td> <td style="text-align: center;">Gain</td> <td style="text-align: center;">Suppress Limit Level</td> </tr> </table> <p style="margin-left: 100px;"> 00: X1 01: X 1/2 10: X 1/4 11: X 2 </p> </div> <p>Deciding the amount of Max, Suppress by fixing the suppress Limit Level</p>	7	6-5	4-0	-	Gain	Suppress Limit Level
7	6-5	4-0								
-	Gain	Suppress Limit Level								
CRCO	48	8	WR	Cr(=2R-G) Gain Range : 0 ~ 6 dB (FF)						
CBCO	49	8	WR	Cb(=G-2B) Gain Range : 0 ~ 6 dB (FF)						
CGCO	4A	8	WR	YL Gain Range : 0 ~ 6 dB (FF)						
CUTH	4B	5	WR	Superimpose RAM Mode Input Data High Threshold Range : 0 ~ 32 (1F)						
CLTH	4C	5	WR	Superimpose RAM Mode Input Data Low Threshold Range : 0 ~ 32 (1F)						

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION
MRPW	60	8	WR	Red Pre-white Balance Coeff. Range : 0 ~ 18dB (FF) 0dB : HEX 20
MGPW	61	8	WR	Green Pre-white Balance Coeff. Range : 0 ~ 18dB (FF) 0dB : HEX 20
MBPW	62	8	WR	Blue Pre-white Balance Coeff. Range : 0 ~ 18dB (FF) 0dB : HEX 20
MRWB	63	8	WR	Red White Balance Coeff. Range : 0 ~ 18dB (FF) 0dB : HEX 20
MBWB	64	8	WR	Blue White Balance Coeff. Range : 0 ~ 18dB (FF) 0dB : HEX 20
MDSCR	65	8	WR	RGB Black Balance Coeff. (2°C Data) Range : -127(HEX 81) ~ +127 (HEX 7F)
MDSCG	66	8	WR	
MDSCB	67	8	WR	
MRHC	68	8	WR	R-Y Hue Control Value (MRHC*[B-Y]) Range : -(B-Y) ~ +(B-Y) MSB 7 : Sign bit LSB 0 ~ 6 : Absolute Value
MBHC	69	8	WR	B-Y Hue Control Value (MBHC*[R-Y]) Range : -(R-Y) ~ +(R-Y) MSB 7 : Sign bit LSB 0 ~ 6 : Absolute Value
MRYG	6A	8	WR	R-Y Gain Range : 0~18dB (FF) 0dB : HEX 20
MBYG	6B	8	WR	B-Y Gain Range : 0 ~ 18dB (FF) 0dB : HEX 20
MA1C	6C	8	WR	Color difference signal Matrix Coeff Range : 0 ~ 18 dB (FF) Recommand Value: MA1C : 0.7 (Hex B3) MB1C : 0.3 (Hex 4d) MA2C : 0.11 (Hex 1C) MB2C : 0.89 (Hex E4)
MB1C	6D	8	WR	
MA2C	6E	8	WR	
MB2C	6F	8	WR	

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION																
EHSBY	A0	8	WR	B-Y axis direction Burst Level (2'C Data) Range : -128(HEX 80) ~ + 127 (HEX 7F) MSB 7 : Sign bit LSB 6 ~ 0 : 2'C Value																
EHSRY	A1	8	WR	R-Y axis direction Burst Level (2' C Data) Range : -128(HEX 80) ~ + 127 (HEX 7F) MSB 7 : Sign bit LSB 6 ~ 0 : 2'C Value																
ECFAD	A2	8	WR	Chroma Fade Control Value Range : 0 ~ 6dB (FF) 0dB : HEX 80																
EWCLP	A3	8	WR	White Clip Level Range : 0 ~ 255																
EYFAD	A4	8	WR	Luminance Fade Control Value Range : 0 ~ 18dB (FF) 0dB : HEX 80																
ESET	A5	8	WR	Set-up Level Range : 0 ~ 255 (FF)																
EBLK	A6	8	WR	Blanking Level Range : 0 ~ 255 (FF)																
ECMD1	A7	8	WR	Command Register																
<p>Bit field diagram for ECMD1 register:</p> <table border="1"> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>EN</td><td>DVR</td><td>DAC</td><td>DAY</td><td>AR1</td><td>AR0</td><td>PS</td><td>NP</td> </tr> </table> <ul style="list-style-type: none"> NP: 1: Negative Effect, 0: Normal Operation PS: 1: Output Pin Disable, 0: Normal Operation AR1, AR0: 00: Normal Operation, 01: 16 steps Art Freeze, 10: 8 steps Art Freeze, 11: 4 steps Art Freeze DAY: 1: Y D/A Clock Inverting, 0: Normal Operation DAC: 1: Digital VCR Interface Mode, 0: Normal Operation DVR, EN: 1: Y/C Output Enable, 0: Y/C Output Disable 					7	6	5	4	3	2	1	0	EN	DVR	DAC	DAY	AR1	AR0	PS	NP
7	6	5	4	3	2	1	0													
EN	DVR	DAC	DAY	AR1	AR0	PS	NP													
ECMD2	A8	5	W	Delay Adjust																
				<table border="1"> <tr> <td>7~5</td> <td>4, 3</td> <td>2~0</td> </tr> <tr> <td>----</td> <td>Title Y/C delay daj. Range:0~3PCK</td> <td>Y/C delay adj. Range:0~3 PCLK</td> </tr> </table>	7~5	4, 3	2~0	----	Title Y/C delay daj. Range:0~3PCK	Y/C delay adj. Range:0~3 PCLK										
7~5	4, 3	2~0																		
----	Title Y/C delay daj. Range:0~3PCK	Y/C delay adj. Range:0~3 PCLK																		

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION																
TCMD1	10	7	WR	Shutter Speed Control																
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>-</td><td>TSE</td><td>SS1</td><td>SS0</td><td>HS3</td><td>HS2</td><td>HS1</td><td>HS0</td> </tr> </table> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>000 : 1/60 sec (PAL 1/50 sec) 001 : 1/85 sec 010 : 1/125 sec 011 : 1/185 sec 100 : 1/250 sec 101 : 1/375 sec 110 : 1/500 sec 111 : 1/750 sec 000 : 1/1000 sec 001 : 1/1500 sec 010 : 1/2000 sec 011 : 1/2500 sec 100 : 1/4000 sec 101 : 1/6000 sec 110 : 1/10000 sec 111 : Flicker Mode</p> <p>00 : 1/30 sec 01 : 1/15 sec 10 : 1/8 sec 11 : 1/4 sec</p> <p>0 : Normal 1 : Low Shutter Speed enable</p> </div> <div style="width: 50%; border-left: 1px solid black; padding-left: 10px;"> <p>000 : 1/60 sec (PAL 1/50 sec) 001 : 1/85 sec 010 : 1/125 sec 011 : 1/185 sec 100 : 1/250 sec 101 : 1/375 sec 110 : 1/500 sec 111 : 1/750 sec 000 : 1/1000 sec 001 : 1/1500 sec 010 : 1/2000 sec 011 : 1/2500 sec 100 : 1/4000 sec 101 : 1/6000 sec 110 : 1/10000 sec 111 : Flicker Mode</p> <p>00 : 1/30 sec 01 : 1/15 sec 10 : 1/8 sec 11 : 1/4 sec</p> <p>0 : Normal 1 : Low Shutter Speed enable</p> </div> </div>					7	6	5	4	3	2	1	0	-	TSE	SS1	SS0	HS3	HS2	HS1	HS0
7	6	5	4	3	2	1	0													
-	TSE	SS1	SS0	HS3	HS2	HS1	HS0													
ECMD2	11	1	WR	Flickerless Control																
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>FLM</td> </tr> </table> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"></div> <div style="width: 50%; border-left: 1px solid black; padding-left: 10px;"> <p>1 : NTSC 1/120 sec, PAL 1/100 sec 0 : Flickerless Mode Off</p> </div> </div>					7	6	5	4	3	2	1	0	-	-	-	-	-	-	-	FLM
7	6	5	4	3	2	1	0													
-	-	-	-	-	-	-	FLM													

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION	REMARKS
SCMD	80	8	WR	Superimpose Command Register	

Superimpose Instruction Set Format

7	6	5	4	3	2	1	0
FIL	OUT	CT1	CT0	Sub Instruction CODE			

1) TYPE 0 (CT1=0, CT2=0) : Environmental Instruction

7	6	5	4	3	2	1	0
-	-	0	0	-	C2	C1	C0

* NML Conditions :

- ROM : 0
- TOG : 0
- MEDi : 0
- SWAP : 0
- PB : 0
- TST : 0
- DMA : 0
- WRN : 0

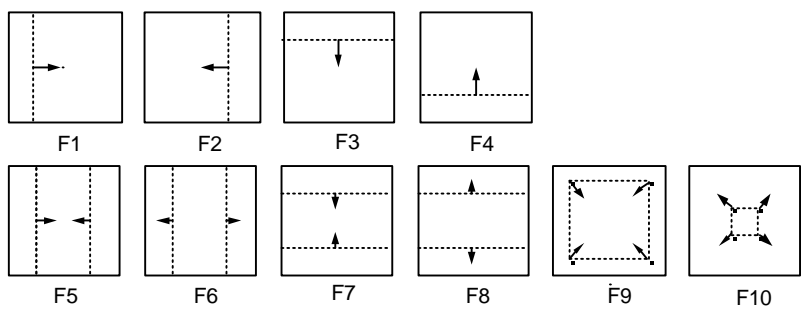
- 000 : ---
- 001 : NML
- 010 : STOP
- 011 : TOG
- 100 : MEDi
- 101 : ROM
- 110 : SWAP
- 111 : ---

2) TYPE 1 (CT1=0, CT0=0) : Configure Environment 1 (R/W, SCOLL)

7	6	5	4	3	2	1	0
-	-	0	1	-	C2	C1	C0

- 000 : ----
- 001 : READ
- 010 : WRITE
- 011 : SCi
- 100 : SCo
- 101 : ----
- 110 : ----
- 111 : ----

* Execute Superimpose Busy Flag ' 1 ' while in sci, sco operation Mode.
It is, impossible to excute the other superimpose intermediate while in this status,
for about 4 seconds.

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION	REMARKS																
3) TYPE2 (CT1 = 1, CT2 = 0) : Environmental Instructions																					
		<table border="1"> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>FIL</td><td>OUT</td><td>1</td><td>0</td><td>F3</td><td>F2</td><td>F1</td><td>F0</td> </tr> </table>	7	6	5	4	3	2	1	0	FIL	OUT	1	0	F3	F2	F1	F0		<p> 0000 : --- 0001 : F1 0010 : F2 0011 : F3 0100 : F4 0101 : F5 0110 : F6 0111 : F7 1000 : F8 1001 : F9 1010 : F10 1011 : --- 1100 : --- 1101 : --- 1110 : --- 1111 : --- </p>	
7	6	5	4	3	2	1	0														
FIL	OUT	1	0	F3	F2	F1	F0														
		<p> FIL: 0 : Normal Wiper, 1 : Inverse Wiper OUT: 0 : Normal, 1 : FILL Mode </p>																			
																					
				<p>* Execute Superimpose Busy Flag '1' in while in wiper operation Mode. It is impossible to excute the other superimpose intermediate while in this status, for about 4 seconds.</p>																	
4) TYPE 3 (CT1 = 1, CT0 = 1) : Configure Environment 3																					
		<table border="1"> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>-</td><td>-</td><td>1</td><td>1</td><td>-</td><td>C2</td><td>C1</td><td>C0</td> </tr> </table>	7	6	5	4	3	2	1	0	-	-	1	1	-	C2	C1	C0		<p> 000 : --- 001 : PB 010 : TST1 011 : DMA 100 : WRN 101 : --- 110 : --- 111 : --- </p>	
7	6	5	4	3	2	1	0														
-	-	1	1	-	C2	C1	C0														

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION	REMARKS																																				
SCOL	81	7	R/W	Super Impose Color Status Register																																					
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>C02</td><td>C01</td><td>C00</td><td>-</td><td>ROM</td><td>SWP</td><td>TOG</td><td>FIL</td> </tr> </table> <div style="margin-left: 200px;"> <p>0 : Medi off 1 : Medi on</p> <p>0 : Toggle off 1 : Toggle on</p> <p>0 : Swap off 1 : Swap on</p> <p>0 : RAM Mode 1 : ROM Mode</p> <p>000 : Blank 001 : Blue 010 : Red 011 : Magenta 100 : Green 101 : Cyan 110 : Yellow 111 : White</p> </div> <p>*MSB [7~5] Color status bit is READ/WRITE, all other bits are READ only</p>						7	6	5	4	3	2	1	0	C02	C01	C00	-	ROM	SWP	TOG	FIL																				
7	6	5	4	3	2	1	0																																		
C02	C01	C00	-	ROM	SWP	TOG	FIL																																		
SDAT	82	8	R/W	Data Register (Buffer of using at DMA test mode)																																					
SPG	83	3	WR	Setting RAM mode stage																																					
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td> </tr> <tr> <td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>PG1</td><td>PG0</td><td>SWP</td> </tr> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>PG1</td><td>PG2</td><td>Normal</td><td>Hi8</td> </tr> <tr> <td>0</td><td>0</td><td>Page 0</td><td>Page 0</td> </tr> <tr> <td>0</td><td>1</td><td>Page 1</td><td>Page 1</td> </tr> <tr> <td>1</td><td>0</td><td>Page 2</td><td>-</td> </tr> <tr> <td>1</td><td>1</td><td>Page 3</td><td>-</td> </tr> </table>						7	6	5	4	3	2	1	0	-	-	-	-	-	PG1	PG0	SWP	PG1	PG2	Normal	Hi8	0	0	Page 0	Page 0	0	1	Page 1	Page 1	1	0	Page 2	-	1	1	Page 3	-
7	6	5	4	3	2	1	0																																		
-	-	-	-	-	PG1	PG0	SWP																																		
PG1	PG2	Normal	Hi8																																						
0	0	Page 0	Page 0																																						
0	1	Page 1	Page 1																																						
1	0	Page 2	-																																						
1	1	Page 3	-																																						

REGISTER NAME	ADDRESS NO.(HEX)	BITS	MODE	DESCRIPTION	REMARKS						
SADR00	84	8	WR	ROM image 0 address register (20Bit)							
SADR01	85	8	WR								
SADR02	86	4	WR								
SADR10	87	8	WR	ROM image 1 address register (20Bit)							
SADR11	88	8	WR								
SADR12	89	4	WR								
SADR20	8A	8	WR	ROM image 2 address register (20Bit)							
SADR21	8B	8	WR								
SADR22	8C	4	WR								
SADR30	8D	8	WR	ROM image 3 address register (20Bit)							
SADR31	8E	8	WR								
SADR32	8F	4	WR								
SADR40	90	8	WR	ROM image 4 address register (20Bit)							
SADR41	91	8	WR								
SADR42	92	4	WR								
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">23 ~ 16</td> <td style="text-align: center;">15 ~ 8</td> <td style="text-align: center;">4~0</td> </tr> <tr> <td style="text-align: center;">* SADR2</td> <td style="text-align: center;">SADR1</td> <td style="text-align: center;">SADR0</td> </tr> </table> <p>* SADR2 uses only LSB 4Bit.</p>						23 ~ 16	15 ~ 8	4~0	* SADR2	SADR1	SADR0
23 ~ 16	15 ~ 8	4~0									
* SADR2	SADR1	SADR0									
STH	93	8	WR	Horizontal counter test register (Used in test)							
STV	94	8	WR	Vertical counter test register (Used in test)							
SSYN	95	8	WR	Title horizontal position adjusting value (After reset, 1 is set and 0 is not allowed.)							
SVRT	96	8	WR	Title vertical position adjusting value (After reset, 1 is set and 0 is not allowed.)							

PACKAGE DIMENSIONS

Unit : mm

