KS57C3016
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C3016 single-chip CMOS microcontroller is designed for very high performance using Samsung's newest 4-bit development approach, SAM4 (Samsung Arrangeable Microcontrollers). With an up-to-16-digit LCD direct drive capability, 4-channel A/D converter, 8-bit timer/counter, PLL frequency synthesizer, and 6-channel PWM outputs, the KS57C3016 offers you an excellent design solution for a wide variety of applications, especially those requiring DTS support.

Up to 55 pins of the 100-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the KS57C3016's advanced CMOS technology ensures low power consumption and a wide operating voltage range.

FEATURES

Memory

- 1,024 × 4-bit RAM
- 16,384 × 8-bit ROM

55 I/O Pins

- Input only: 4 pins
- Output only: 12 pins for bit output or LCD seg output
- I/O: 23 pins (16 I/O pins are n-channel, open-drain)

LCD Controller/Driver

- Maximum 16-digit LCD direct drive capability
- 32 segment × 4 common
- Display modes: static, 1/2duty (1/2 bias)
- 1/3 duty (1/2 or 1/3 bias), 1/4duty (1/3 bias)

8-Bit Basic Timer

- Four interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider
- Serial I/O clock generator

Watch Timer

- Time interval generation: 0.5s, 3.9 ms at 32768 Hz
- Four frequency outputs to BUZ pin
- Clock generation for LCD

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal/external clock source

A/D Converter

- 4 channels (8-bit resolution)
- 17.8 μs conversion speed at 4.5 MHz

PLL Frequency Synthesizer

- AM input: maximum 30 MHz
- FM input: maximum 200 MHz

Pulse Width Modulator

- 6-channel (8-bit resolution)

Intermediate Frequency (IF) Counter

- 16-bit binary counter
- Divide-by-2 and gate control

Interrupts

- Four internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Four Power-Down Modes

- Idle: Only CPU clock stops
- Stop 1: Only main system clock stops
- Stop 2: Both main and subsystem clocks stop
- CE low: PLL block stops

Oscillation Sources

- Crystal or ceramic for main clock
- Crystal for subsystem clock
- Main system clock frequency: 4.5 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider (4, 6, 64)

Instruction Execution Times

- 0.9, 1.8, 14.2 μs at 4.5 MHz
- 122 μs at 32.768 kHz

Operating Temperature Range

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 100-pin QFP

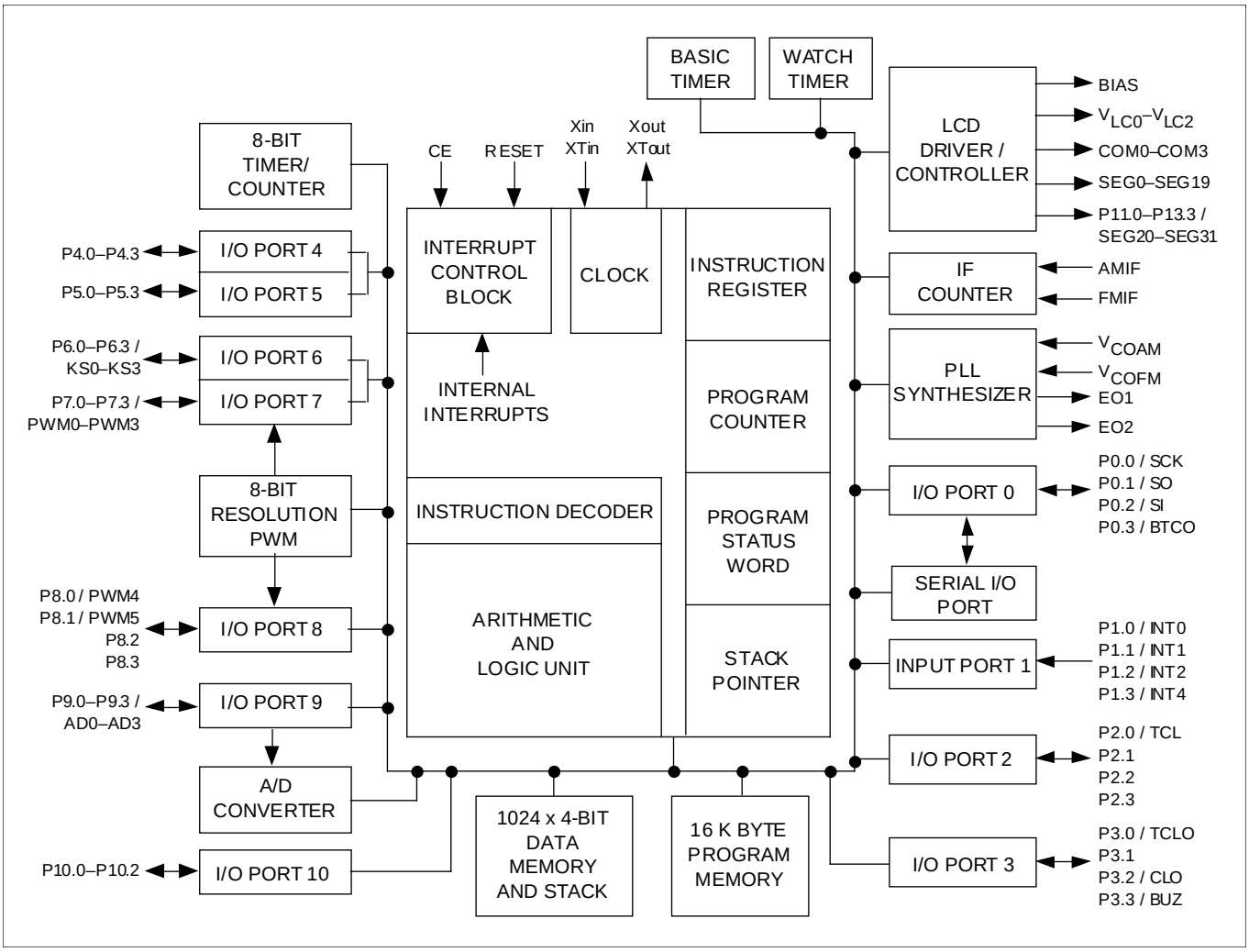

Figure 1. KS57C3016 Block Diagram

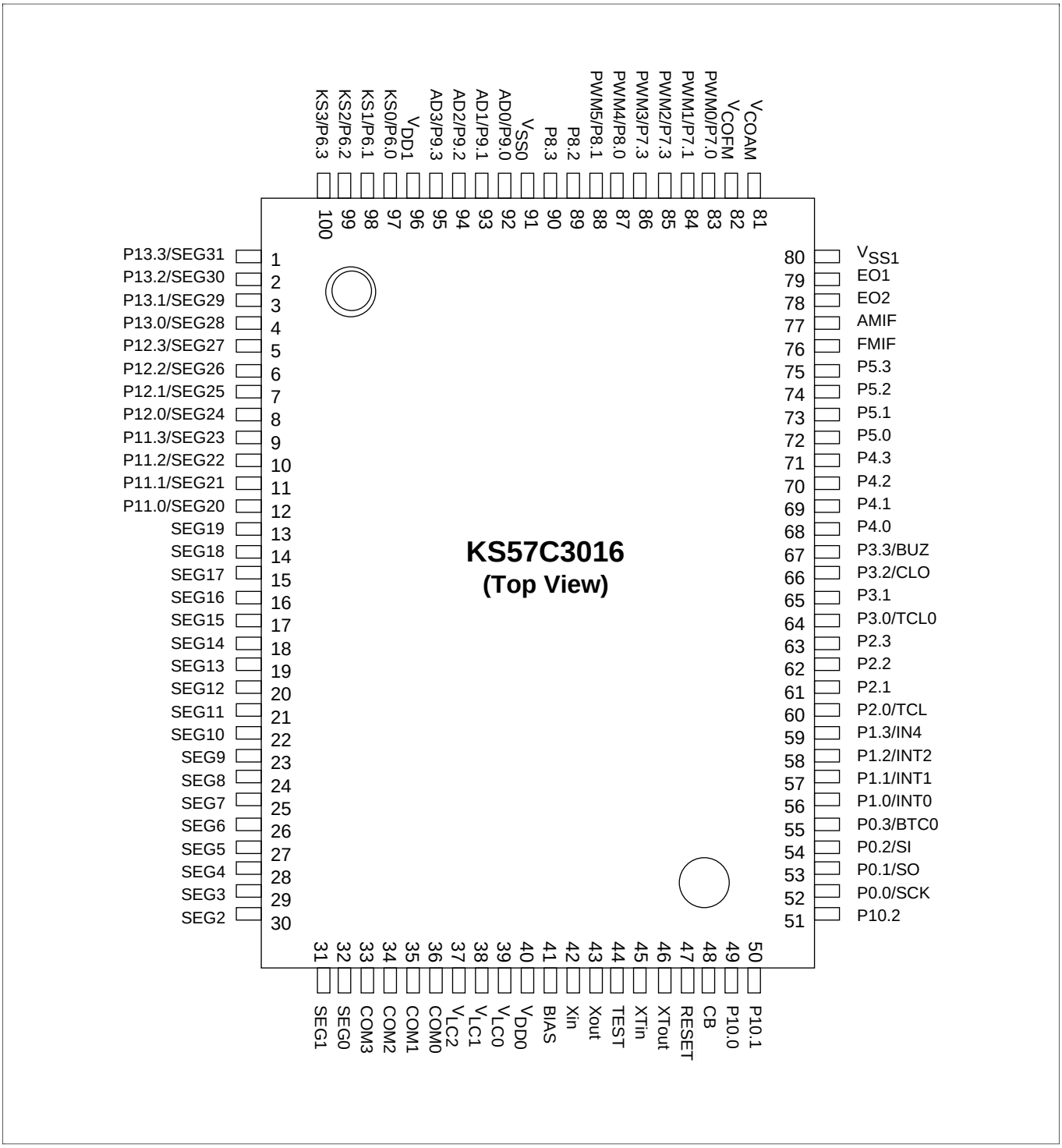

Figure 2. KS57C3016 Pin Assignments (100-QFP)

Table 1. KS57C3016 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins; pull-up resistors are automatically disabled for output pins.	52 53 54 55	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are assignable by software to pins P1.0, P1.1, and P1.2.	56 57 58 59	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0	60 61 62 63	TCL0
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0	64 65 66 67	TCLO0 — CLO BUZ
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. N-channel open-drain output up to 9volts. 1- and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to support 8-bit data transfer. Pull-up resistors are assignable to individual pins by mask option.	68–71 72–75	—
P6.0–P6.3	I/O	Same as port 0. Ports 6 and 7 can be paired to enable 8-bit data transfer.	97–100	KS0–KS3
P7.0–P7.3 P8.0–P8.3	I/O	N-channel open-drain 4-bit I/O ports up to 9 volts. 1-bit and 4-bit read/write and test is possible. Pins are individually software configurable as input or output. Pull-up resistors are assignable to individual pins by mask option.	83–86 87–90	PWM0–PWM3 PWM4–PWM5
P9.0–P9.3	I/O	Same as port 0	92–95	AD0–AD3
P10.0–P10.2	I/O	Same as port 0 except that port 10 is 3-bit I/O port.	49–51	—
P11.0–11.3 P12.0–12.3 P13.0–13.3	O	Output ports for 1-bit data	12–9 8–5 4–1	SEG20–SEG31
SCK	I/O	Serial I/O interface clock signal	52	P0.0
SO	I/O	Serial data output	53	P0.1
SI	I/O	Serial data input	54	P0.2

Table 1. KS57C3016 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
BTCO	I/O	Basic timer clock output	55	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	56–57	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	58	P1.2
INT4	I	External interrupt with detection of rising and falling edges	59	P1.3
TCL0	I/O	External clock input for timer/counter 0	60	P2.0
TCLO0	I/O	Timer/counter 0 clock output	64	P3.0
CLO	I/O	Clock output	66	P3.2
BUZ	I/O	2.2 kHz, 4.4 kHz, 8.8 kHz, or 17.6 kHz frequency output at 4.5 MHz for buzzer sound	67	P3.3
KS0–KS3	I/O	Quasi-interrupt inputs with falling edge detection	97–100	P6.0–P6.3
PWM0–PWM5	I/O	PWM outputs	83–88	P7.0–P8.1
AD0–AD3	I/O	A/D converter analog inputs	92–95	P9.0–P9.3
SEG0–SEG19	O	LCD segment data outputs	32–13	—
SEG20–SEG31	O	LCD segment data outputs	12–1	P11.0–P13.3
COM0–COM3	O	LCD common signal outputs	36–34	—
CE	I	Input pin for checking device power. High level during normal operation; low level when PLL operation stops.	48	—
EO1–EO2	O	Output for PLL error data	78–79	—
V_{COAM}, V_{COFM}	I	External V_{COAM} and V_{COFM} inputs	81–82	—
AMIF, FMIF	I	Intermediate AM/FM frequency input	77–76	—
TEST	I	Test signal input (must be connected to $V_{SS)}$	44	—
V_{DD0}	—	Main power supply	40	—
V_{SS0}	—	Main ground	91	—
V_{DD1}	—	Power supply for PLL prescaler	96	—
V_{SS1}	—	PLL prescaler ground	80	—
RESET	I	Reset signal	47	—
BIAS	—	LCD power control	41	—
V_{LC0}–V_{LC2}	—	LCD power supply. Voltage dividing resistors are assignable by mask option.	39–37	—
X_{in}, X_{out}	—	Crystal, ceramic, or RC oscillator signal for main system clock.	42, 43	—
XT_{in}, XT_{out}	—	Crystal oscillator signal for subsystem clock.	45, 46	—

Table 2. Supplemental KS57C3016 Pin Data

Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
52–55	P0.0–P0.3	SCK, SO, SI, BTCO	I/O	Input	6
56–59	P1.0–P1.3	INT0, INT1, INT2	I	Input	3
59	P1.3	INT4	I	Input	2
60–63	P2.0–P2.3	TCL0	I/O	Input	6
64–67	P3.0–P3.3	TCLO0, —, CLO, BUZ	I/O	Input	5
68–71	P4.0–P4.3	—	I/O	Note	10
72–75	P5.0–P5.3	—	I/O	Note	10
97–100	P6.0–P6.3	KS0–KS3	I/O	Input	6
83–86	P7.0–P7.3	PWM0–PWM3	I/O	Note	10
87–88 89–90	P8.0–P8.1 P8.2–P8.3	PWM4–PWM5 —	I/O	Note	10
92–95	P9.0–P9.3	AD0–AD3	I/O	Input	11
49–51	P10.0–P10.2	—	I/O	Input	5
9–12	P11.3–P11.0	SEG23–SEG20	O	Low	9
5–8	P12.3–P12.0	SEG27–SEG24	O	Low	9
1–4	P13.3–P13.0	SEG31–SEG28	O	Low	9
32–16	SEG0–SEG15	—	O	Low	9
15–13	SEG16–SEG19	—	O	Low	7
36–33	COM0–COM3	—	O	Low	8
39–37	V_{LC0}–V_{LC2}	—	—	—	—
41	BIAS	—	—	—	—
76, 77	FMIF, AMIF	—	I	Input	12
78, 79	EO2, EO1	—	O	Output	—
81, 82	V_{COAM}, V_{COFM}	—	I	Input	12
48	CE	—	I	—	—
42, 43	X_{in}, X_{out}	—	—	—	—
45, 46	XT_{in}, XT_{out}	—	—	—	—
47	RESET	—	I	—	13

NOTE: When pull-up resistors are provided, high level; when pull-up resistors are not provided, high impedance.