1 PRODUCT OVERVIEW

The KS57C2916 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With an up-to-704-dot LCD direct drive capability, and flexible 8-bit timer/counter, the KS57C2916 offers an excellent design solution for a mid-end LCD game.

Up to 8 pins of the 80-pin QFP package can be dedicated to I/O. Six vectored interrupts provide fast response to internal and external events. In addition, the KS57C2916's advanced CMOS technology provides for low power consumption.

OTP

The KS57C2916 microcontroller is also available in OTP (One Time Programmable) version, KS57P2916. KS57P2916 microcontroller has an on-chip 16K-byte one-time-programable EPROM instead of masked ROM. The KS57P2916 is comparable to KS57C2916, both in function and in pin configuration.

FEATURES

MEMORY

- 256 × 4-bit RAM (excluding LCD display RAM)
- 16,384 × 8-bit ROM

8 I/O PINS

- I/O: 8 pins

LCD CONTROLLER/DRIVER

- 44 segments and 16 common terminals
  (8, 12 and 16 common selectable)
- Internal resistor circuit for LCD bias
- Voltage doubler
- All dot can be switched on/off

8-BIT BASIC TIMER

- 4 interval timer functions
- Watch-dog timer

8-BIT TIMER/COUNTER

- Programmable 8-bit timer
- Arbitrary clock output (TCLO0)
- Inverted clock output ($\overline{\text{TCLO0}}$)

WATCH TIMER

- Time interval generation: 0.5 s, 3.9 ms
  at 32768 Hz
- Four frequency outputs to BUZ pin and $\overline{\text{BUZ}}$ pin
- Clock source generation for LCD

INTERRUPTS

- Two internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

MEMORY-MAPPED I/O STRUCTURE

- Data memory bank 15

POWER-DOWN MODES

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)
- Sub system clock stop mode

OSCILLATION SOURCES

- Crystal, ceramic, or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

INSTRUCTION EXECUTION TIMES

- 0.95, 1.91, 15.3 µs at 4.19 MHz (main)
- 122 µs at 32.768 kHz (subsystem)

OPERATING TEMPERATURE

- – 40 °C to 85 °C

OPERATING VOLTAGE RANGE

- 2.2 V to 3.4 V (0.4 MHz to 4.19 MHz)

PACKAGE TYPE

- 80-pin QFP or pellet

BLOCK DIAGRAM

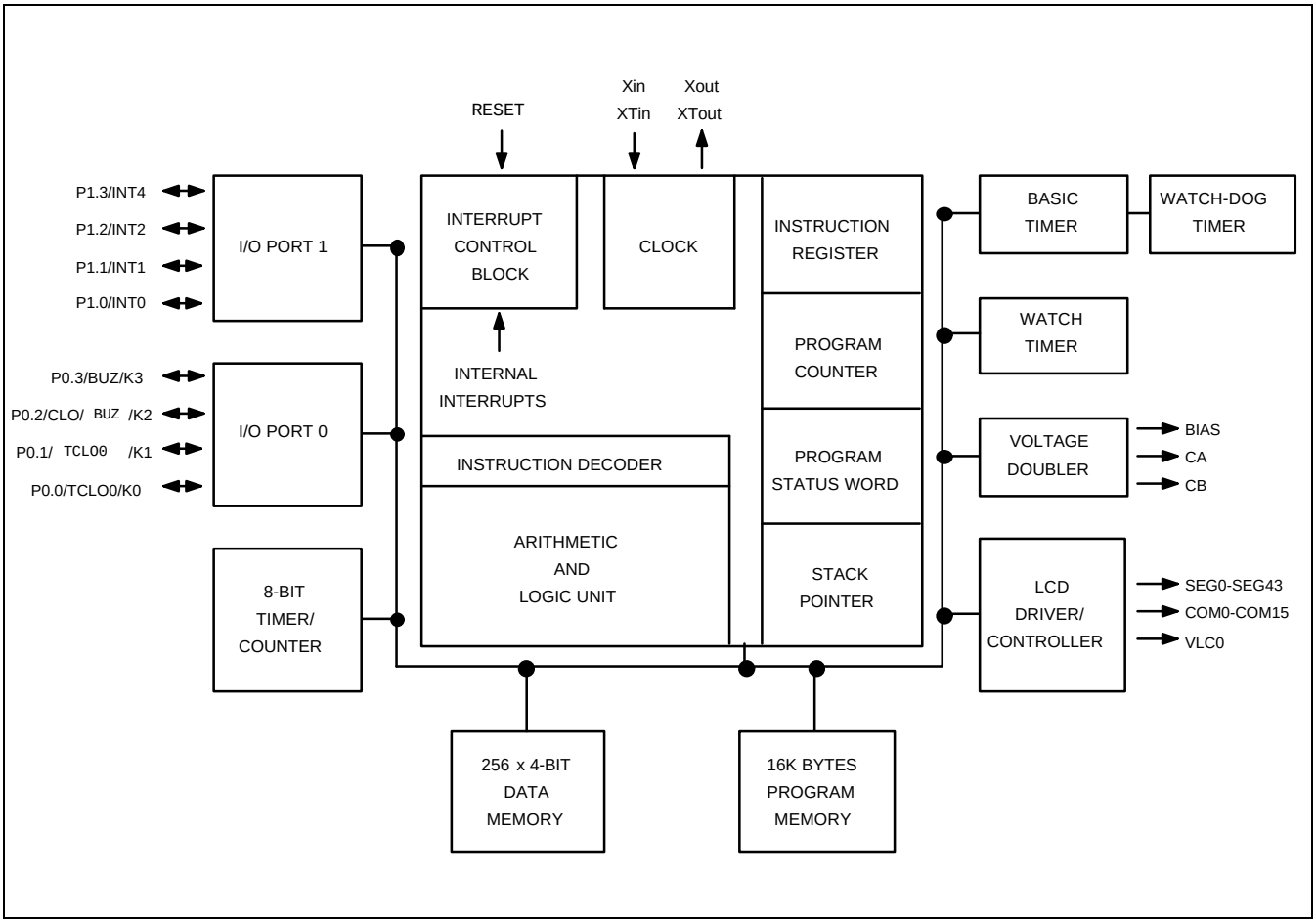

Figure 1-1. KS57C2916 Simplified Block Diagram

PIN ASSIGNMENTS

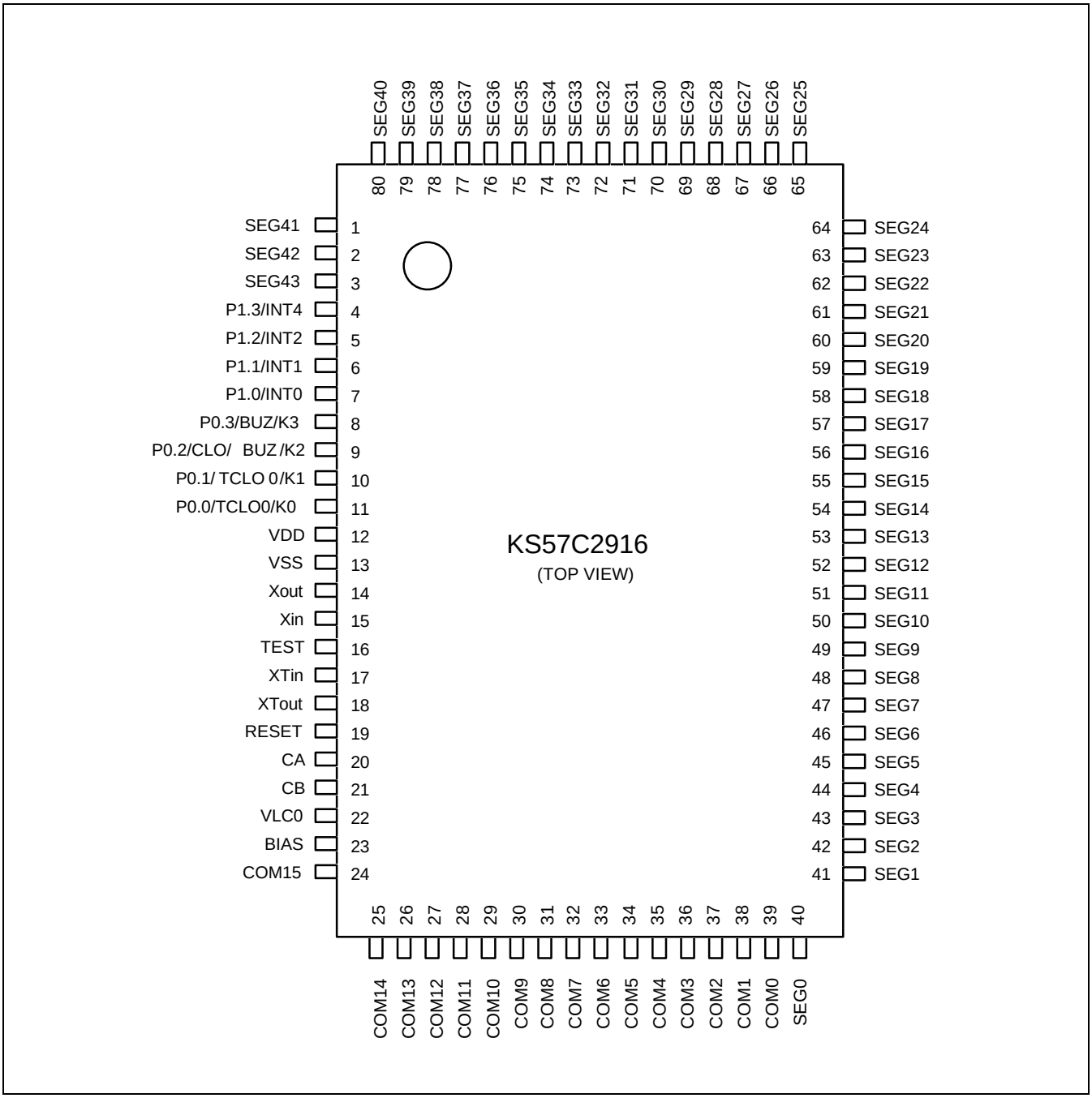

Figure 1-2. KS57C2916 80-QFP Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. KS57C2916 Pin Descriptions

Pin Name	Pin Type	Description	Circuit Type	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test are possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. Individual pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	E-1	11 10 9 8	TCLO0/K0 TCLO0/K1 BUZ/CLO/ K2 BUZ/K3
P1.0 P1.1 P1.2 P1.3	I/O	Same as port 0.	E-1	7 6 5 4	INT0 INT1 INT2 INT4
INT0, INT1	I/O	External interrupts. The triggering edge for INT0 and INT1 is selectable.		7, 6	P1.0, P1.1
INT2	I/O	Quasi-interrupt with detection of rising or falling edges		5	P1.2
INT4	I/O	External interrupt with detection of rising or falling edges.		4	P1.3
BUZ	I/O	2 kHz, 4 kHz, 8 kHz or 16 kHz frequency output for buzzer sound.		8	P0.3/K3
BUZ	I/O	Inverted BUZ signal		9	P0.2/CLO/K 2
CLO	I/O	Clock output		9	P0.2/BUZ/ K2
TCLO0	I/O	Timer/counter 0 inverted clock output		10	P0.1/K1
TCLO0	I/O	Timer/counter 0 clock output		11	P0.0/K0
COM0–COM15	O	LCD common signal output	H-6	39–24	–
SEG0–SEG43	O	LCD segment signal output	H-6	40–80, 1–3	–

Table 1-1. KS57C2916 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Circuit Type	Number	Share Pin
K0–K3	I/O	External interrupt (triggering edge is selectable)	E-1	11–8	P0.0–P0.3
V_{DD}	–	Power supply		12	–
V_{SS}	–	Ground		13	–
RESET	I	Reset input (active low)	B	19	–
CA, CB	–	Capacitor terminal for voltage doubling		20, 21	–
VCL0	–	LCD power supply input		22	–
BIAS	O	Doubling voltage level output		23	–
X_{in}, X_{out}	–	Crystal, ceramic or RC oscillator pins for system clock		15, 14	–
XT_{in}, XT_{out}	–	Crystal oscillator pins for subsystem clock		17, 18	–
TEST	I	Test input (must be connected to V_{SS})		16	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.