1. OVERVIEW

SAMSUNG's KS32C6200 16/32-bit RISC micro-controller is designed to provide a cost-effective and high performance micro controller solution for general applications. To reduce total system cost, KS32C6200 also provides 2-ch UART, 2-ch DMA, System Manager (Chip select logic, DRAM controller), 3-ch Timer, Parallel port, I/O ports.

An outstanding feature of the KS32C6200 is its CPU core, a 16/32-bit RISC processor (ARM7TDMI) designed by Advanced RISC Machines, Ltd. The ARM7TDMI core is a low-power, general purpose, microprocessor macro-cell that was developed for use in application-specific and custom-specific integrated circuits. Its simple, elegant, and fully static design is particularly suitable for cost-sensitive and power sensitive applications.

The KS32C6200 was developed using ARM7TDMI core, 0.5um CMOS standard cells, and memory compiler. Most of the on-chip function blocks were designed using an HDL synthesizer. The KS32C6200 has been fully verified in SAMSUNG's MCU test environment.

The integrated on-chip functions are as follows:

- Static ARM7TDMI CPU Core
- 2K byte Instruction/Data cache
- System Manager

  (DRAM Control, Chip Select logic)
- 2-ch DMA
- Parallel Ports (Support IEEE1284)
- 2-ch UART
- 3-ch Timer
- Interrupt Controller
- Tone Generator
- I/O ports
- Watch Dog Timer
- Derasterizer
- 208bit Shifter/Rotater
- On-Chip Debugging Support using JTAG

2. FEATURES

Architecture

- Integrated system for general embedded applications, image data processing
- Fully 16/32-bit RISC architecture
- Efficient and powerful ARM7TDMI CPU core
- Cost-effective JTAG-based debug solution

System manager

- 8/16-bit external bus support for ROM/SRAM,
- DRAM and external I/O
- Support EDO DRAM
- Programmable access cycle (From 2 to 7 wait cycles)
- Cost-effective memory-to-peripheral interface
- support Self refresh mode.

Unified Instruction/Data cache

- Two way set associative cache with 2KBinstructions/data words)
- LRU (Least Recently Used)
- Four depth write buffer

UART (SIO)

Two channel UART (Serial I/O) with DMA based or interrupt based operation; supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive

- Programmable baud rate
- Infra-red(IR) Tx/Rx support(IrDA)

Programmable I/O Ports

- 5 programmable I/O ports (GIOP)
- 6 input ports (GIP)
- 13 output ports (GOP)

Derasterizer / Shifter

- 16×16 bit rotate by 90/270 degree for raster data rotation
- Reverse 16bit data
- Left/right shift/rotate 7 half words with selectable direction

Parallel Port Interface Controller

- DMA-based or interrupt-based operation
- Supports IEEE Standard 1284 communication modes (Compatibility mode, nibble mode, bytes mode, and ECP mode)
- Supports ECP protocol with or without run-length encoding (RLE)
- Automatic handshaking mode for any forward or reverse protocol with software/DMA

DMA (Direct Memory Access) Controller

- 2-channel DMAC
- Memory-to-memory,memory-to-parallel port,parallel-to-memory,UART-to-memory, memory-to-UART, I/O-to-memory, memory-to-I/O data transfers without CPU intervention.
- Initiated by software or external DMA request.
- Increments or decrements source or 8-bit, 16-bit or 32-bit data transfer

Timers

- Three programmable 16-bit timers

Tone Generator

- Programmable square wave generator

Watch Dog Timer

- 16-bit timer useful for periodic reset or interrupts

Interrupt Controller

- 15 interrupt sources (External : 2)
- Normal or fast interrupt modes(IRQ, FIQ)

Operating Voltage Range

- 4.75 to 5.25 volt

Operating Frequency

- up-to 33MHz

Package Type

- 160-pin TQFP

Block Diagram

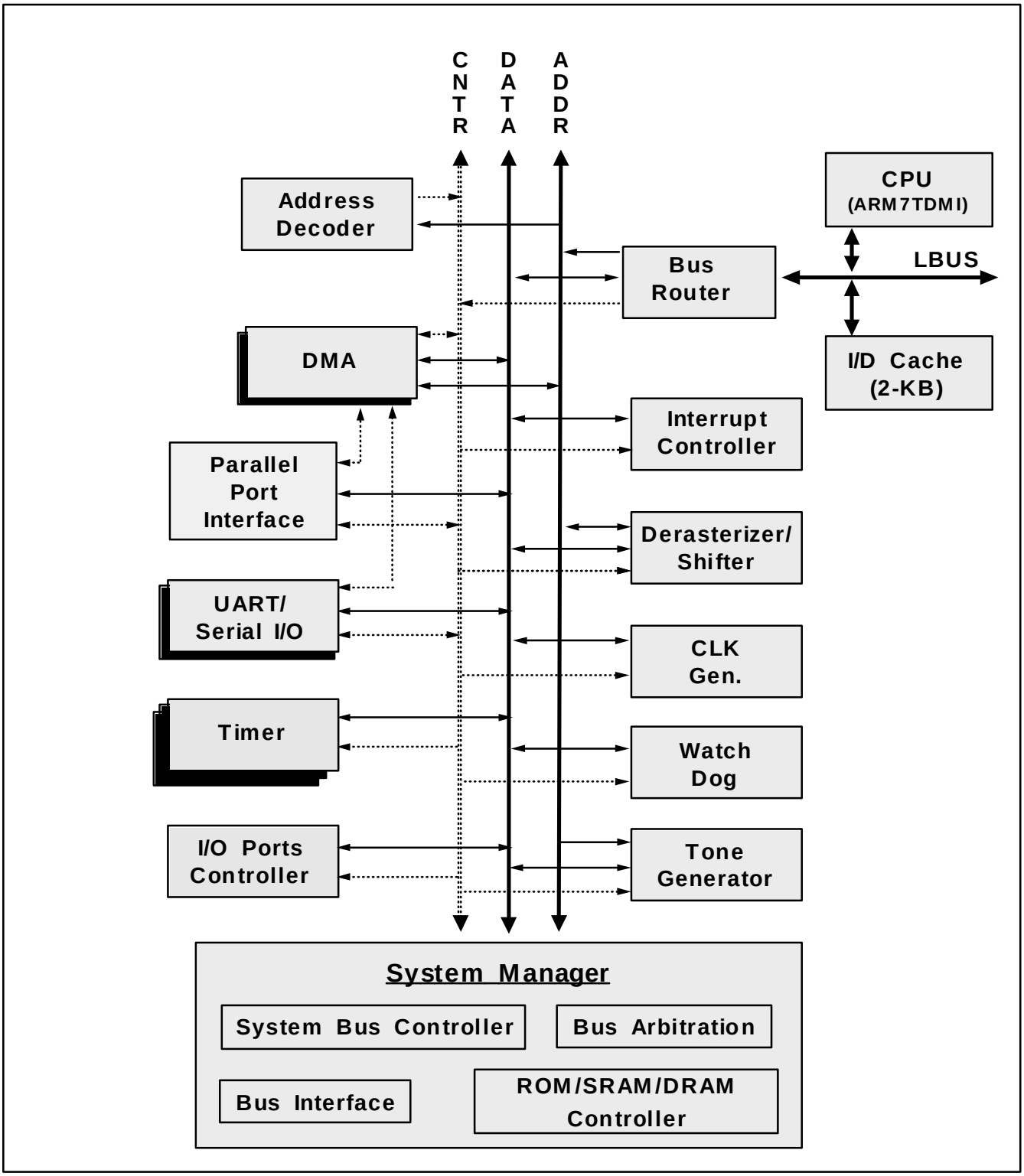
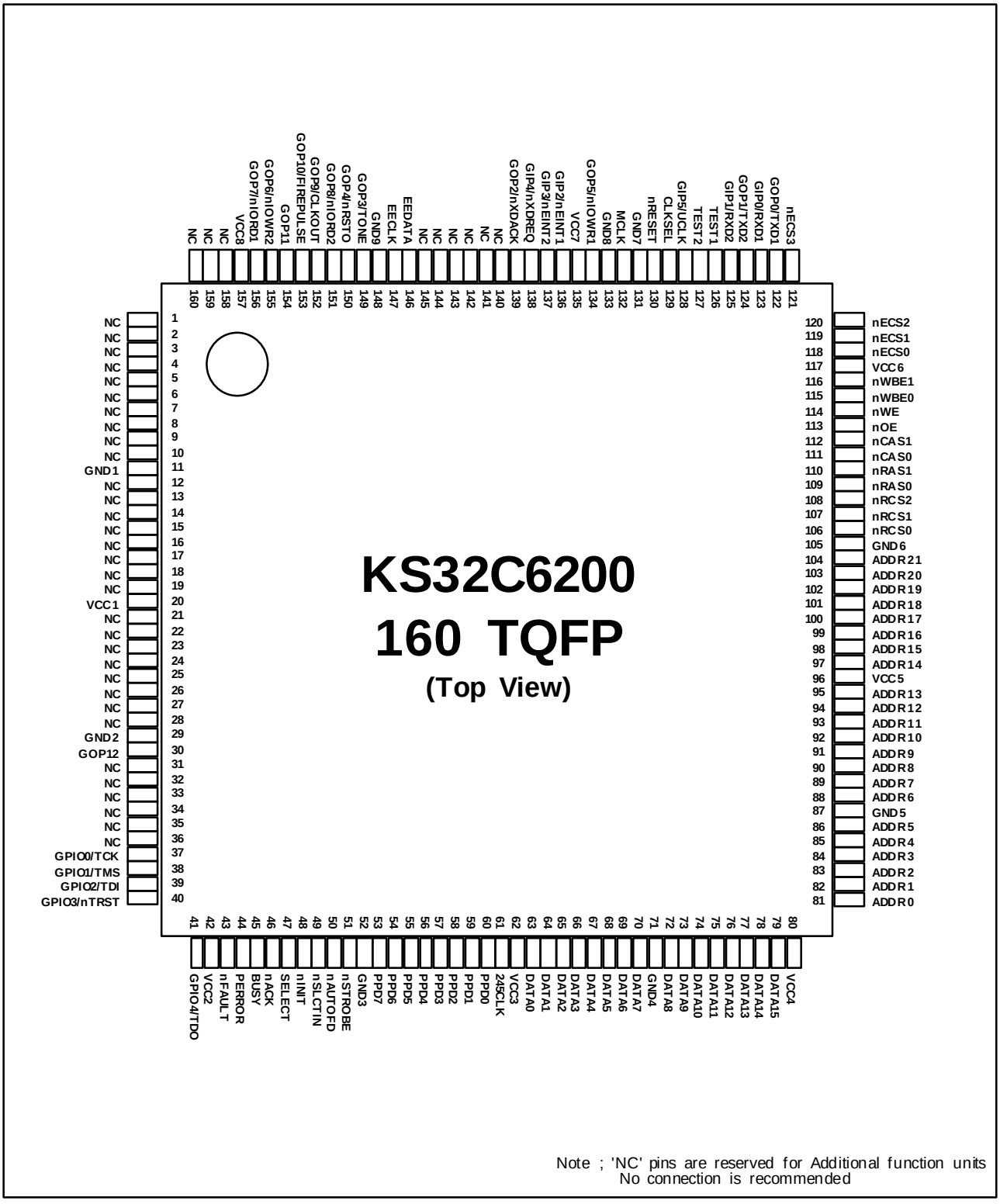


Figure 1. KS32C6200 Block Diagram

Pin Assignments



Note ; 'NC' pins are reserved for Additional function units
No connection is recommended

FIGURE 2. KS32C6200 PIN ASSIGNMENTS