1. Introduction

120 channel common driver for STN LCD

KS0795 is a 120 channel common driver IC enabled to drive dot matrix STN LCD panel. This device is consists of 60 x 2 bits bidirectional shift register, 60 x 2 bits level shift and 60 x 2 bits output driver and can control number of output driver with cascade connection.

Low power consumption and high voltage operation are available by high voltage CMOS process technology.

2. Features

. STN LCD common driver with 120 channel output

. Left/Right shift mode selection

. Power supply voltage : 2.7 ~ 5.5(V)

. Supply voltage for display : 14V¡-38V

. Available 4 mode operation with bidirectional 60 X 2 bits shift register and driver

¨ç X1 ¡æ X120 ¨è X120 ¡æ X1

¨é X1 ¡æ X60, X61 ¡æ X120 ¨ê X120 ¡æ X61, X60 ¡æ X1

. Operating frequency : -20¡É ~ +75¡É

. ON resistance : 0.5K§Ù typ. (20V, 1/13 bias, 25¡É)

1.0K§Ù max. (20V, 1/13 bias, 75¡É)

. Interface

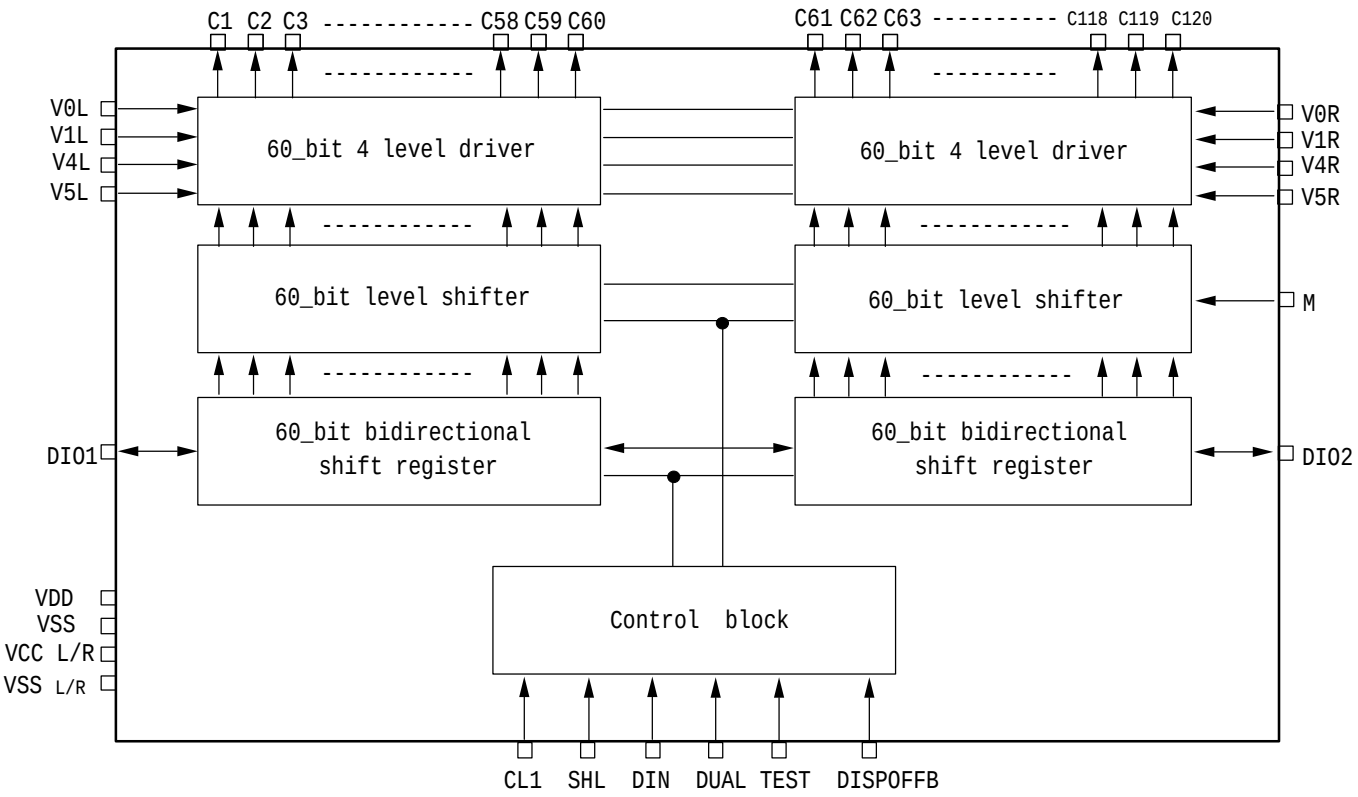
COMMON	SEGMENT
Other KS0795	KS0794

. Applicable LCD duty : 1/64 ~ 1/480

. High voltage CMOS process

. 142 pin slim TCP package

3. Block diagram



4. Terminal descriptions

<table>
<tr><th>Pin Name</th><th>Input
Output</th><th>Function</th><th>Interface</th></tr>
<tr><td>VDD</td><td rowspan="4"></td><td>For logical circuit (+5V¡¾10%, +3V¡¾10%)</td><td rowspan="4">POWER</td></tr>
<tr><td>Vss</td><td>For logical circuit (GND)</td></tr>
<tr><td>VCCR, VCCL</td><td>Maximum supply voltage for LCD drive circuit.</td></tr>
<tr><td>VSSR, VSSL</td><td>GND</td></tr>
<tr><td>V0R, VOL
V1R, V1L
V4R, V4L
V5R, V5L</td><td>Input</td><td>Bias supply voltage terminals to drive the LCD.
Bias voltage divided by the resistance is usually used as supply voltage source.
V0R, V0L, V5R, V5L : selection level
V1R, V1L, V4R, V4L : non-selection level</td><td>POWER</td></tr>
<tr><td>C1 ~ C120</td><td>Output</td><td>Display data output for LCD driving.
One of V0, V1, V4 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal.
<table>
<tr><th>DISPOFFB</th><th>M</th><th>DATA</th><th>OUTPUT LEVEL</th></tr>
<tr><td rowspan="4">H</td><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>V1</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V0</td></tr>
<tr><td>L</td><td>V4</td></tr>
<tr><td>L</td><td>X</td><td>X</td><td>V5</td></tr>
</table></td><td>LCD</td></tr>
<tr><td>DISPOFFB</td><td>Input</td><td>Control input pin for display data output level (C1¡-C120).
V5 level is output from C1¡-C120 terminal during "L"level input.
LCD becomes non-selected by V5 level output from every output of common drivers and every output of segment drivers.</td><td>CONTROLLER</td></tr>
<tr><td>M</td><td>Input</td><td>Alternate signal input pin for LCD driving.</td><td>CONTROLLER</td></tr>
<tr><td>CL1</td><td>Input</td><td>The signal for latching the shift register contents is input to this terminal.
The display data is latched at the falling edge of clock pulse.</td><td>CONTROLLER</td></tr>
<tr><td>DIN</td><td>Input</td><td>DIN = Open : Normal opration (Built-in pull-down resistor)
DIN = High : Data input</td><td></td></tr>
<tr><td>TEST</td><td>Input</td><td>TEST = Open : Normal opration (Built-in pull-down resistor)
TEST = High : Test mode</td><td></td></tr>
<tr><td>DUAL</td><td>Input</td><td>DUAL = Low : 120 ch mode
DUAL = High : 60ch x 2 mode</td><td></td></tr>
<tr><td>SHL</td><td>Input</td><td>Selection of the shift direction</td><td></td></tr>
<tr><td>DIO1, DIO2</td><td>Input
Output</td><td>Data input/output pin of internal shift register</td><td></td></tr>
</table>

5. Functional descriptions

5.1 60_bit 4 level driver

The 60_bit 4 level driver block is generates four voltage levels V0, V1, V4 and V5 which drive the LCD panel. One of these four levels is output to the corresponding C1 ~ C120 pin, selects the output voltage level according to the M and latched data valve.

- Relationship of M & data

M	DATA	OUTPUT LEVEL(C1 ~ C120)
H	H	V5
	L	V1
L	H	V0
	L	V4

5.2 60_bit level shifter

The 60_bit level shifter changes logic control signal(3.0V ~ 5.5V) into high voltage signal for 4 level driver.

5.3 60_bit bidirectional shift register

1_bit input data(from DIO1 or DIO2) is shifted by the direction according to the SHL signal input. The 1_bit of Shifted out data is output from DIO1 or DIO2 pin to the next driver IC. Both actions occur simultaneously at the falling edge of each shift clock pulse(CL1).

5.4 Control block

5.4.1 Display off functions

Display off functions is LCD driver output level controls. A "DISPOFFB=L" sets the LCD drive outputs C1 ~ C120 to the V5 level. DISPOFFB terminal is normally "H" sets used.

- Display off functions

DISPOFFB	M	DATA	OUTPUT LEVEL(C1 ~ C120)
H	H	H	V5
		L	V1
	L	H	V0
		L	V4
L	X	X	V5

X:Don'tcare

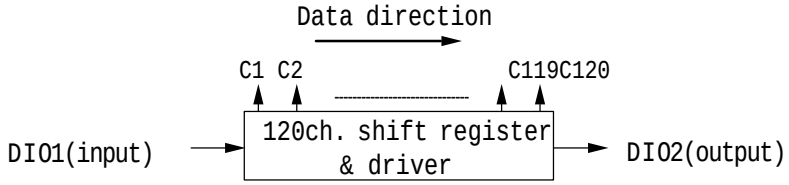
5.4.2 Single/Dual mode functions

DUAL	SHL	DIO1	DIN	DIO2	Shift direction of LCD driving output
L	L	INPUT	OPEN	OUTPUT	DIO1 ¡æ C1 ¡æ C2 ¡æ ..... ¡æ C119 ¡æ C120 ¡æ DIO2
	H	OUTPUT	OPEN	INPUT	DIO2 ¡æ C120 ¡æ C119 ¡æ ..... ¡æ C2 ¡æ C1 ¡æ DIO1
H	L	INPUT	INPUT	OUTPUT	DIO1 ¡æC1¡æ .... ¡æC60, DIN¡æC61¡æ .... ¡æC120¡æ DIO2
	H	OUTPUT	INPUT	INPUT	DIO2 ¡æC120¡æ .... ¡æC61, DIN¡æC60¡æ .... ¡æC1¡æ DIO1

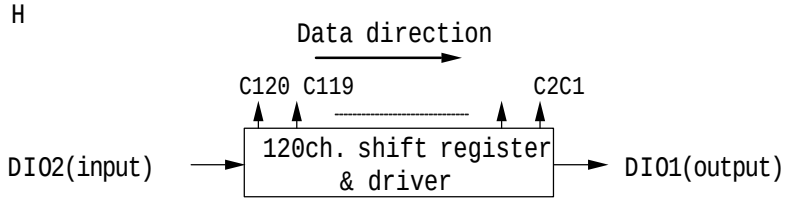
- Output shift direction

1) Single mode (120channel mode, DUAL=L)

SHL= L

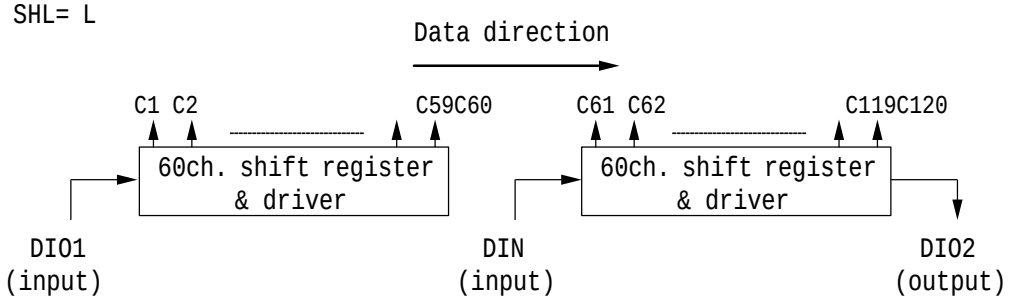


SHL= H

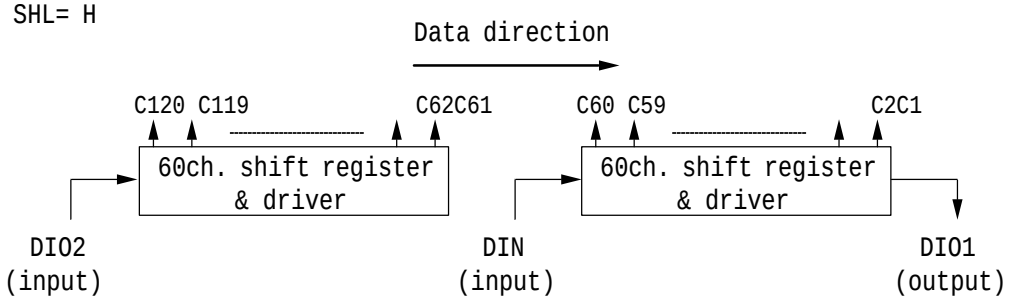


2) Dual mode (60channel X 2 mode, DUAL=H)

SHL= L



SHL= H



6. MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Power supply voltage	VDD	-0.3 ~ 6.5	V
Driver supply voltage	VCC	-0.3 ~ 42	
	V0, V1, V4, V5	-0.3 ~ VCC + 0.3	
Input voltage *	Vin	-0.3 ~ VDD + 0.3	V
Operating temperature	Topr	-20 ~ +75	¡É
Storage temperature	Tstg	-40 ~ +125	

* Voltage greater than above may result in damage to the circuit.
  VCC ¡Ã V0 > V1 > V4 > V5 ¡Ã VSS
* Application pin ; CL1,M,SHL,DL,DR,DISPOFFB,DUAL,SDT,TEST

7. RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power supply voltage	VDD	2.7	-	5.5	V
Driver supply voltage	VCC	14	-	38	
	V0, V1, V4, V5	*			
Operating temperature	Topr	-20 ~ +75			¡É

* VCC ¡Ã V0 > V1 > V4 > V5 ¡Ã VSS

8. ELECTRICAL CHARACTERISTICS

8.1 DC Characteristics (VDD = 2.7 ~ 5.5V,VSS = 0V,VCC = 14 ~ 38V,Ta = -20 ~ +75¡É)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Operating voltage	VDD	-		2.7	-	5.5	V
	VCC	-		14	-	38	
Input voltage(*1)	V_{IH}	-		0.8VDD	-	VDD	
	V_{IL}	-		0	-	0.2VDD	
Output voltage(*2)	V_{OH}	I_{OH} = -0.5 mA		VDD-0.5	-	VDD	V
	V_{OL}	I_{OL} = 0.5 mA		0	-	0.5	
Output resistance(*3)	Ron	C1 ~ C120	VOUT = V0 - 0.5V	-	0.5	1.0	§Ú
			VOUT = V1 ¡¾ 0.5V	-			
			VOUT = V4 ¡¾ 0.5V	-			
			VOUT = V5 + 0.5V	-			
Input leakage current	I_{IL1}(*4)	V_{IN} = 0 ~ VDD		-1	-	1	§Ë
	I_{IL2}	VDD=5.5V, VCC=38V		-200	-	200	
	I_{IL3}	VDD=5.5V, TEST=5.5V, TEST pin		-	400	600	
Stand-by current	I_{STB}	(*5)		-1.0	-	1.0	§Ë
Supply current (*6)	I_{DD1}	VDD=5.0V, VCC=38V		-	-	60	§Ë
	I_{DD2}	VDD=3.0V, VCC=38V		-	-	20	
	I_{CC1}	VDD=5.0V, VCC=38V		-	-	150	§Ë
	I_{CC2}	VDD=3.0V, VCC=38V		-	-	100	

*1. Applied to CL1, M, SHL, DIN, DIO1, DIO2, DISPOFFB, DUAL,TEST pin

*2. Applied to DIO1, DIO2 pin

*3. VCC=V0=20V, 1/13 bias, V1=(12/13)V0, V4=(1/13)V0, V5=VSS=0V

*4. Applied to CL1, M, SHL, DIN, DIO1, DIO2, DISPOFFB, DUAL pin

*5. VDD=5.5V, VCC=38V, V_{IH}=VDD, V_{IL}=VSS, SHL=VSS, DISPOFFB=VDD, M=VSS

*6. fCL1=38.4KHz, FM= 80Hz, No load

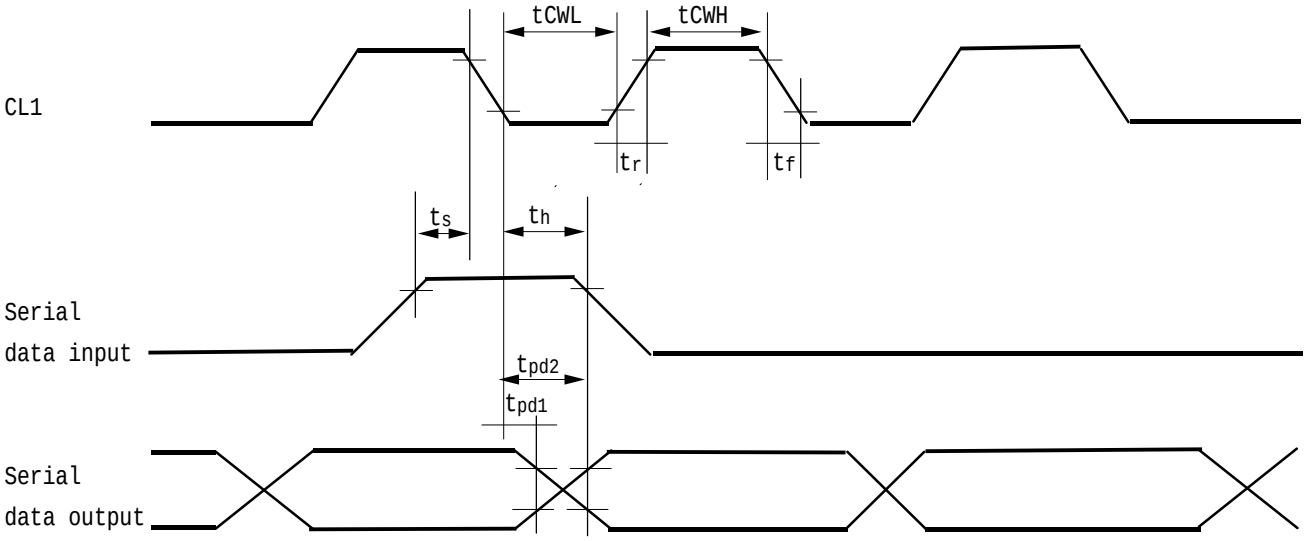
8.2 AC Characteristics

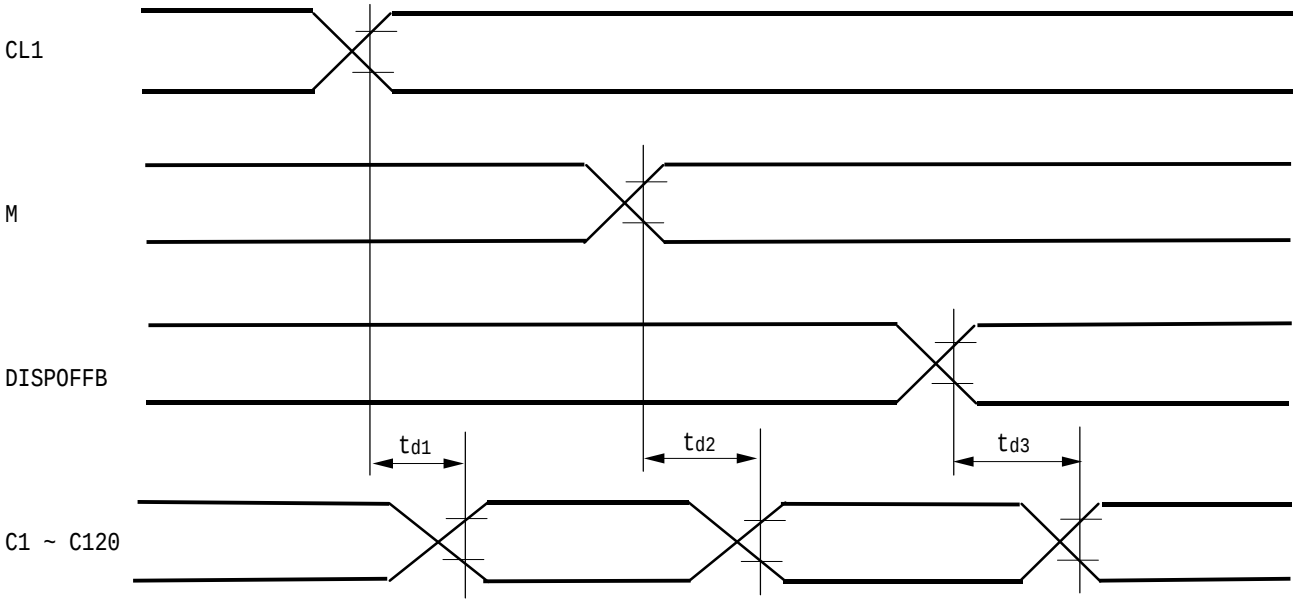
(VDD=2.7~5.5V,VSS=0V,VCC=14~42V,Ta=-20¡-+75¡É)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock pulse width (High)	t_{CWH}	CL1	12	-	-	
Clock pulse width (Low)	t_{CWL}	CL1	110	-	-	
Clock rise/fall time	t_r/t_f	CL1	-	-	20	
Data set-up time	t_s	DIO1, DIO2, DIN	45	-	-	
Data hold time	t_h		0	-	-	
Serial output delay time	t_{pd1}	DIO1, DIO2, C_L=10pF	15	-	-	
	t_{pd2}	DIO1, DIO2, C_L=10pF	-	-	200	
Output delay time	t_{d1}	CL1 ¡æ OUTPUT	-	-	500	
	t_{d2}	M ¡æ OUTPUT	-	-	500	
	t_{d3}	DISPOFFB ¡æ OUTPUT	-	-	500	

* Insert bypass capacitor (0.1uF) between VDD to VSS and VCC to VSS
  Place the bypass capacitor as close to the LSI as possible.

8.2 AC Characteristics (continued)





APPLICATION CIRCUIT EXAMPLE