INTRODUCTION

The KS0717 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It contains 55 common and 100 segment driver circuits. This chip is connected directly to a microprocessor, accepts 8-bit serial or parallel display data and stores in an on-chip display data RAM of 65 × 100 bits. It provides a highly-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. It also performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

- **Driver output circuits**
  - — 55 common outputs / 100 segment outputs
- **Applicable duty-ratios**

Duty Ratio	Applicable LCD Bias	Maximum Display Area
1/55	1/8 or 1/6	55 × 100
1/34	1/6 or 1/5	34 × 100

- **On-chip display data RAM**
  - — Capacity: 65 × 100 = 6,500 bits
  - — Bit data “1”: a dot of display is illuminated
  - — Bit data “0”: a dot of display is not illuminated
- **Microprocessor interface**
  - — 8-bit parallel bidirectional interface with 6800-series or 8080-series
  - — Serial interface (only write operation) available
  - — Multi-chip operation (master, slave) available
- **On-chip low power analog circuit**
  - — On-chip oscillator circuit
  - — Voltage converter (×2 / ×3 / ×4 / ×5)
  - — Voltage regulator (temperature coefficient: – 0.05% / °C, – 0.2% / °C or external input)
  - — On-chip electronic contrast control functions (64 steps)
  - — Voltage follower (LCD Bias: 1/5, 1/6 or 1/8)

- **Operating voltage range**
  - — Supply voltage (V_{DD}): 2.4V to 5.5V
  - — LCD driving voltage (V_{LCD} = V0–V_{SS}): 4.0V to 15.0V
- **Low power consumption**
  - — 100μA Max. (V_{DD} = 3V, 4 boosting, V0 = 11V, Internal power supply on)
  - — 10μA Max. (standby mode)
- **Package type**
  - — Slim chip for COG, and TCP available

BLOCK DIAGRAM

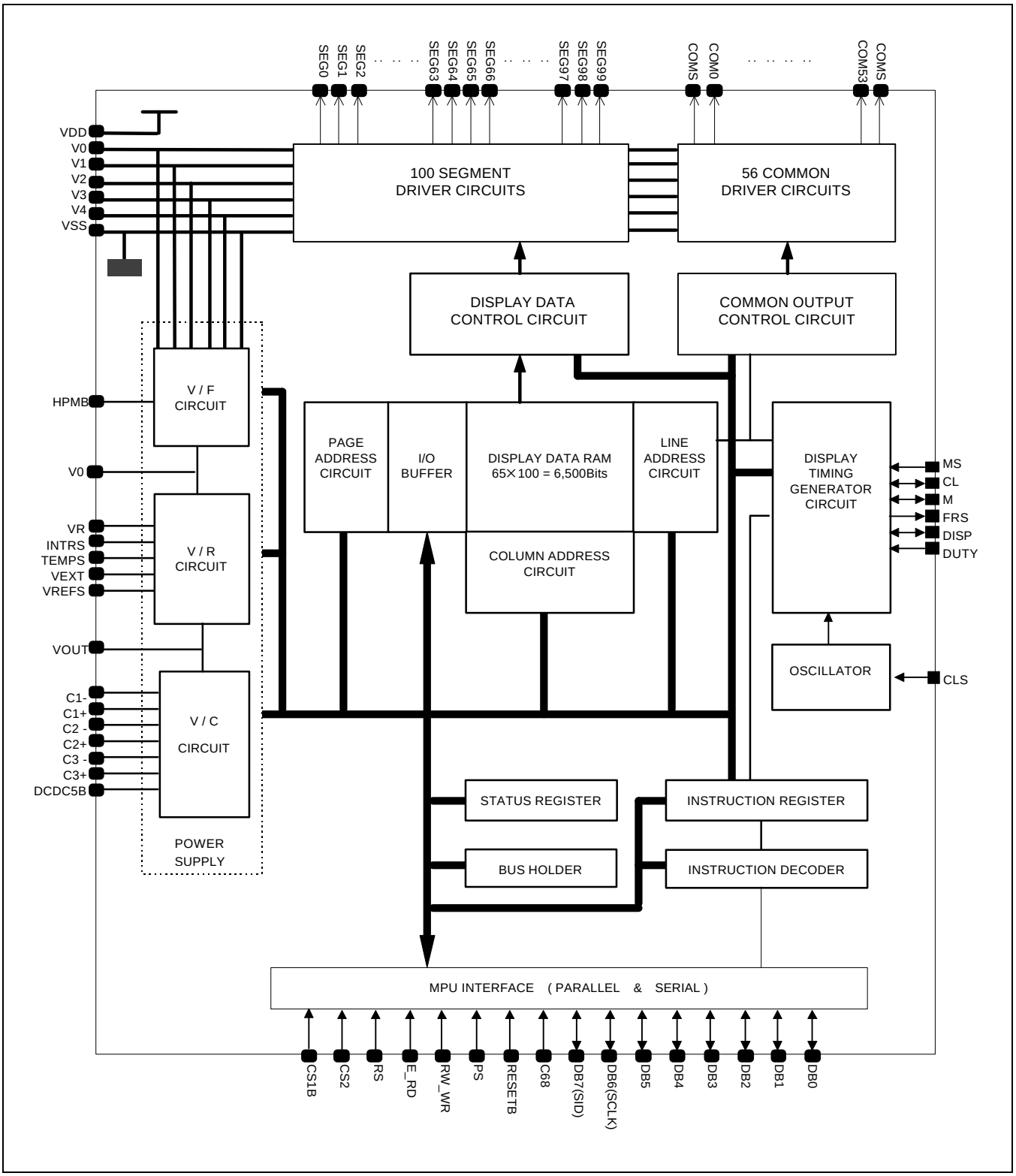


Figure 1. Block Diagram

PAD CONFIGURATION

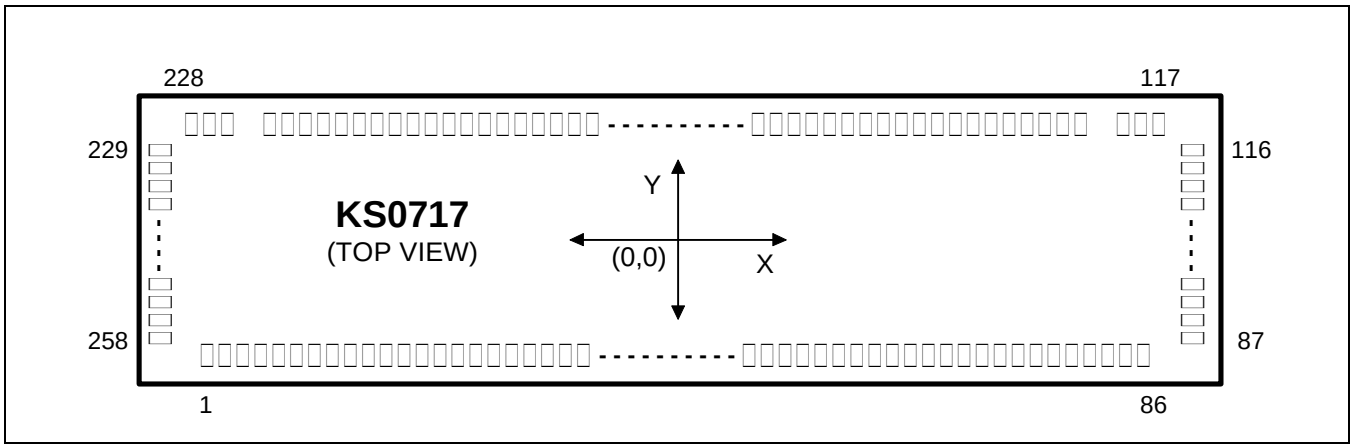


Figure 2. Pad Configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	–	9000	2350	μm
Pad pitch	1 to 86	90		
	87 to 258	70		
Bumped pad size	1 to 86	56	114	
	87 to 116	108	50	
	117 to 228	50	108	
	229 to 258	108	50	
Bumped pad height	1 to 258	17 (Typ.)		

PAD LOCATION

Table 1. Pad Location

[unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	DUMMY	-3825	-1051	51	C3-	675	-1051	101	COM13	4341	-35
2	FRS	-3735	-1051	52	C1-	765	-1051	102	COM12	4341	35
3	M	-3645	-1051	53	C1-	855	-1051	103	COM11	4341	105
4	CL	-3555	-1051	54	C1+	945	-1051	104	COM10	4341	175
5	DISP	-3465	-1051	55	C1+	1035	-1051	105	COM9	4341	245
6	Vss	-3375	-1051	56	C1+	1125	-1051	106	COM8	4341	315
7	CS1B	-3285	-1051	57	C2+	1215	-1051	107	COM7	4341	385
8	CS2	-3195	-1051	58	C2+	1305	-1051	108	COM6	4341	455
9	VDD	-3105	-1051	59	C2-	1395	-1051	109	COM5	4341	525
10	E_RD	-3015	-1051	60	C2-	1485	-1051	110	COM4	4341	595
11	RESETB	-2925	-1051	61	C2-	1575	-1051	111	COM3	4341	665
12	Vss	-2835	-1051	62	VDD	1665	-1051	112	COM2	4341	735
13	RS	-2745	-1051	63	VEXT	1755	-1051	113	COM1	4341	805
14	RW_WR	-2655	-1051	64	REF	1845	-1051	114	COM0	4341	875
15	DB0	-2565	-1051	65	Vss	1935	-1051	115	COMS	4341	945
16	DB1	-2475	-1051	66	V1	2025	-1051	116	DUMMY	4341	1015
17	DB2	-2385	-1051	67	V1	2115	-1051	117	DUMMY	3885	1016
18	DB3	-2295	-1051	68	V2	2205	-1051	118	DUMMY	3815	1016
19	DB4	-2205	-1051	69	V2	2295	-1051	119	DUMMY	3745	1016
20	DB5	-2115	-1051	70	V3	2385	-1051	120	DUMMY	3675	1016
21	DB6	-2025	-1051	71	V3	2475	-1051	121	DUMMY	3605	1016
22	DB7	-1935	-1051	72	V4	2565	-1051	122	DUMMY	3535	1016
23	Vss	-1845	-1051	73	V4	2655	-1051	123	SEG0	3465	1016
24	MS	-1755	-1051	74	V0	2745	-1051	124	SEG1	3395	1016
25	CLS	-1665	-1051	75	V0	2835	-1051	125	SEG2	3325	1016
26	VDD	-1575	-1051	76	VR	2925	-1051	126	SEG3	3255	1016
27	DCDC5B	-1485	-1051	77	VR	3015	-1051	127	SEG4	3185	1016
28	C68	-1395	-1051	78	Vss	3105	-1051	128	SEG5	3115	1016
29	Vss	-1305	-1051	79	Vss	3195	-1051	129	SEG6	3045	1016
30	Vss	-1215	-1051	80	PS	3285	-1051	130	SEG7	2975	1016
31	Vss	-1125	-1051	81	HPMB	3375	-1051	131	SEG8	2905	1016
32	Vss	-1035	-1051	82	VDD	3465	-1051	132	SEG9	2835	1016
33	Vss	-945	-1051	83	INTRS	3555	-1051	133	SEG10	2765	1016
34	Vss	-855	-1051	84	TEMPS	3645	-1051	134	SEG11	2695	1016
35	Vss	-765	-1051	85	Vss	3735	-1051	135	SEG12	2625	1016
36	DUTY	-675	-1051	86	DUMMY	3825	-1051	136	SEG13	2555	1016
37	VDD	-585	-1051	87	DUMMY	4341	-1015	137	SEG14	2485	1016
38	VDD	-495	-1051	88	COM26	4341	-945	138	SEG15	2415	1016
39	VDD	-405	-1051	89	COM25	4341	-875	139	SEG16	2345	1016
40	VDD	-315	-1051	90	COM24	4341	-805	140	SEG17	2275	1016
41	VDD	-225	-1051	91	COM23	4341	-735	141	SEG18	2205	1016
42	VDD	-135	-1051	92	COM22	4341	-665	142	SEG19	2135	1016
43	VDD	-45	-1051	93	COM21	4341	-595	143	SEG20	2065	1016
44	VOUT	45	-1051	94	COM20	4341	-525	144	SEG21	1995	1016
45	VOUT	135	-1051	95	COM19	4341	-455	145	SEG22	1925	1016
46	VOUT	225	-1051	96	COM18	4341	-385	146	SEG23	1855	1016
47	C3+	315	-1051	97	COM17	4341	-315	147	SEG24	1785	1016
48	C3+	405	-1051	98	COM16	4341	-245	148	SEG25	1715	1016
49	C3-	495	-1051	99	COM15	4341	-175	149	SEG26	1645	1016
50	C3-	585	-1051	100	COM14	4341	-105	150	SEG27	1575	1016

Table 1. Pad Location (Continued)

[unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
151	SEG28	1505	1016	201	SEG78	-1995	1016	251	COM48	-4341	-525
152	SEG29	1435	1016	202	SEG79	-2065	1016	252	COM49	-4341	-595
153	SEG30	1365	1016	203	SEG80	-2135	1016	253	COM50	-4341	-665
154	SEG31	1295	1016	204	SEG81	-2205	1016	254	COM51	-4341	-735
155	SEG32	1225	1016	205	SEG82	-2275	1016	255	COM52	-4341	-805
156	SEG33	1155	1016	206	SEG83	-2345	1016	256	COM53	-4341	-875
157	SEG34	1085	1016	207	SEG84	-2415	1016	257	COMS	-4341	-945
158	SEG35	1015	1016	208	SEG85	-2485	1016	258	DUMMY	-4341	-1015
159	SEG36	945	1016	209	SEG86	-2555	1016				
160	SEG37	875	1016	210	SEG87	-2625	1016				
161	SEG38	805	1016	211	SEG88	-2695	1016				
162	SEG39	735	1016	212	SEG89	-2765	1016				
163	SEG40	665	1016	213	SEG90	-2835	1016				
164	SEG41	595	1016	214	SEG91	-2905	1016				
165	SEG42	525	1016	215	SEG92	-2975	1016				
166	SEG43	455	1016	216	SEG93	-3045	1016				
167	SEG44	385	1016	217	SEG94	-3115	1016				
168	SEG45	315	1016	218	SEG95	-3185	1016				
169	SEG46	245	1016	219	SEG96	-3255	1016				
170	SEG47	175	1016	220	SEG97	-3325	1016				
171	SEG48	105	1016	221	SEG98	-3395	1016				
172	SEG49	35	1016	222	SEG99	-3465	1016				
173	SEG50	-35	1016	223	DUMMY	-3535	1016				
174	SEG51	-105	1016	224	DUMMY	-3605	1016				
175	SEG52	-175	1016	225	DUMMY	-3675	1016				
176	SEG53	-245	1016	226	DUMMY	-3745	1016				
177	SEG54	-315	1016	227	DUMMY	-3815	1016				
178	SEG55	-385	1016	228	DUMMY	-3885	1016				
179	SEG56	-455	1016	229	DUMMY	-4341	1015				
180	SEG57	-525	1016	230	COM27	-4341	945				
181	SEG58	-595	1016	231	COM28	-4341	875				
182	SEG59	-665	1016	232	COM29	-4341	805				
183	SEG60	-735	1016	233	COM30	-4341	735				
184	SEG61	-805	1016	234	COM31	-4341	665				
185	SEG62	-875	1016	235	COM32	-4341	595				
186	SEG63	-945	1016	236	COM33	-4341	525				
187	SEG64	-1015	1016	237	COM34	-4341	455				
188	SEG65	-1085	1016	238	COM35	-4341	385				
189	SEG66	-1155	1016	239	COM36	-4341	315				
190	SEG67	-1225	1016	240	COM37	-4341	245				
191	SEG68	-1295	1016	241	COM38	-4341	175				
192	SEG69	-1365	1016	242	COM39	-4341	105				
193	SEG70	-1435	1016	243	COM40	-4341	35				
194	SEG71	-1505	1016	244	COM41	-4341	-35				
195	SEG72	-1575	1016	245	COM42	-4341	-105				
196	SEG73	-1645	1016	246	COM43	-4341	-175				
197	SEG74	-1715	1016	247	COM44	-4341	-245				
198	SEG75	-1785	1016	248	COM45	-4341	-315				
199	SEG76	-1855	1016	249	COM46	-4341	-385				
200	SEG77	-1925	1016	250	COM47	-4341	-455				

PIN DESCRIPTION

Table 2. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Power Supply</td></tr>
<tr><td>V_{DD}</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>V_{SS}</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages. The voltage determined by LCD pixel is impedance converted by an operational amplifier for application. Voltage should have the following relationship:

$V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$

When the internal power circuit is active, these voltages are generated according to the state of LCD Bias, as shown in the following table.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/8 Bias</td><td>(7/8) V0</td><td>(6/8) V0</td><td>(2/8) V0</td><td>(1/8) V0</td></tr>
<tr><td>1/6 Bias</td><td>(5/6) V0</td><td>(4/6) V0</td><td>(2/6) V0</td><td>(1/6) V0</td></tr>
<tr><td>1/5 Bias</td><td>(4/5) V0</td><td>(3/5) V0</td><td>(2/5) V0</td><td>(1/5) V0</td></tr>
</table>
</td></tr>
<tr><td colspan="3">LCD Driver Supply</td></tr>
<tr><td>C1–</td><td>O</td><td>Capacitor 1– negative connection pin for voltage converter</td></tr>
<tr><td>C1+</td><td>O</td><td>Capacitor 1+ positive connection pin for voltage converter</td></tr>
<tr><td>C2–</td><td>O</td><td>Capacitor 2– negative connection pin for voltage converter</td></tr>
<tr><td>C2+</td><td>O</td><td>Capacitor 2+ positive connection pin for voltage converter</td></tr>
<tr><td>C3–</td><td>O</td><td>Capacitor 3– negative connection pin for voltage converter</td></tr>
<tr><td>C3+</td><td>O</td><td>Capacitor 3+ positive connection pin for voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>Voltage converter output</td></tr>
<tr><td>DCDC5B</td><td>I</td><td>5-times boosting circuit enable input pin. When this pin is low in 4-times boosting circuit, the 5-times boosted voltage appears at VOUT.</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjustment pin which is valid only when on-chip resistors are not used (INTRS = “L”).</td></tr>
<tr><td>VEXT</td><td>I</td><td>External V_{REF} input pin for the LCD power supply voltage regulator.</td></tr>
<tr><td>REF</td><td>I</td><td>Select the external V_{REF} voltage via the VEXT pin.
REF = “L”: using the external V_{REF}
REF = “H”: using the internal V_{REF}</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">System Control</td></tr>
<tr><td>MS</td><td>I</td><td>Master / slave mode select input. Master makes some signals for display, and slave gets them. This is for display synchronization.
MS = “H”: master mode
MS = “L”: slave mode
<table>
<tr><th>MS</th><th>CLS</th><th>OSC Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>M</th><th>FRS</th><th>DISP</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disable</td><td>Enable</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>–</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin.
CLS = “H”: enable
CLS = “L”: disable (external display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output. When KS0717 is used in master/slave mode (multi-chip), the CL pins must be connected to each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input/output. When KS0717 is used in master/slave mode (multi-chip), the M pins must be connected to each other.
MS = “H”: output
MS = “L”: input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver output. This pin is used together with the M pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input / output. When KS0717 is used in master/slave mode (multi-chip), the DISP pins must be connected to each other.
MS = “H”: output
MS = “L”: input</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal Resistor Select.

This pin selects the resistors for adjusting V0 voltage level and is available only in master mode.
INTRS = “H”: using built-in resistors
INTRS = “L”: not using built-in resistors. V0 voltage is controlled by VR pin and external resistive divider.</td></tr>
<tr><td>HPMB</td><td>I</td><td>Power control pin of the power supply circuit for LCD driver
HPMB = “L”: high power mode
HPMB = “H”: normal mode

This pin is available only in master mode.</td></tr>
<tr><td>TEMPS</td><td>I</td><td>Selects temperature coefficient of the reference voltage
TEMPS = “L”: – 0.05% / °C
TEMPS = “H”: – 0.2% / °C</td></tr>
<tr><td>DUTY</td><td>I</td><td>The LCD driver duty ratio depends on the following table.
DUTY = “L”: 1/34
DUTY = “H”: 1/55</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Microprocessor Interface</td></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin. When RESETB is low, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel/Serial data input select input
<table>
<tr><th>PS</th><th>Operating Mode</th><th>Chip Select</th><th>Data/ Instruction</th><th>Data Input/Output</th><th>Read/ Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RD, RW_WR</td><td>–</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>DB7 (SID)</td><td>Write Only</td><td>DB6 (SCLK)</td></tr>
</table>
NOTE: In serial mode, it is impossible to read data from the on-chip RAM. DB0 to DB5 is high impedance and E_RD and RW_WR must be fixed on high or low.</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor Interface select input in parallel mode
C68 = “H”: 6800-series MPU interface
C68 = “L”: 8080-series MPU interface</td></tr>
<tr><td>CS1B/CS2</td><td>I</td><td>Chip select inputs

Data input / output is enabled only when CS1B is low and CS2 is high. When chip select is non-active,DB0 to DB7 will be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input
RS = “H”: The data on DB0 to DB7 is display data.
RS = “L”: The data on DB0 to DB7 is control data.</td></tr>
<tr><td>RW_WR</td><td>I</td><td>When interfacing to a 6800-series MPU, Read / Write is enabled.
RW_WR = “H”: Read
RW_WR = “L”: Write

When interfacing to an 8080-series MPU, RW_WR is enabled at low.</td></tr>
<tr><td>E_RD</td><td>I</td><td>When interfacing to a 6800-series MPU: active high: This is used as an enabled clock input pin of the 6800-series MPU.

When interfacing to an 8080-series MPU: active low: This input connects the RD signal of the 8080-series MPU. While this signal is Low, KS0717 data bus output is enabled.</td></tr>
<tr><td>DB0 to DB7</td><td>I/O</td><td>8-bit bidirectional data bus. It is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = “L”):
DB0 to DB5: High impedance
DB6: Serial input clock (SCLK)
DB7: Serial input data (SID)

When chip select is not active, DB0 to DB7 will be high impedance.</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">LCD Driver Outputs</td></tr>
<tr><td>SEG0 to SEG99</td><td>O</td><td>LCD driver output for segment. The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">M</th><th colspan="2">SEGs Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>VO</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>H</td><td>L</td><td>V3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table></td></tr>
<tr><td>COM0 to COM53</td><td>O</td><td>LCD driver output for common. The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Display Data</th><th>M</th><th>COMs Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>V_{SS}</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons. The output signals of two pins are same. When not used, these pins should be left open. In multi-chip (master/slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
</table>

FUNCTION DESCRIPTION

MICROPROCESSOR INTERFACE

CHIP SELECT INPUT

There are CS1B and CS2 pins for chip selection. The KS0717 can interface with a microprocessor only when CS1B is low and CS2 is high. When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. In case of serial interface, the internal shift register and the counter are reset.

PARALLEL / SERIAL INTERFACE

KS0717 has three types of interface with MPU, one serial and two parallel. This parallel or serial interface is determined by PS pin as shown in Table 3.

Table 3. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	x	Serial-mode

NOTE: "x" = Don't care

Parallel interface (PS = "H")

The 8-bit bidirectional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in Table 4. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in Table 5.

Table 4. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	RD	WR	DB0 to DB7	8080-series

Table 5. Parallel Data Transfer

Common	6800-Series		8080-Series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (RD)	RW_WR (WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (Instruction)

Serial interface (PS = “L”)

When KS0717 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. Not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easily affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

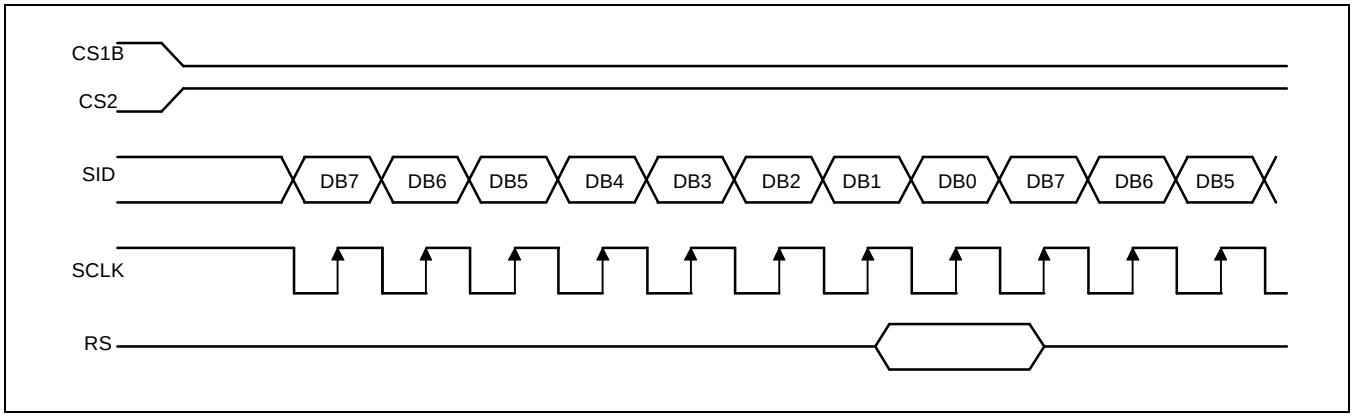


Figure 3. Serial Interface Timing

BUSY FLAG

The busy flag indicates whether the KS0717 is operating or not. When DB7 is HIGH in Read Status operation, this device is in busy status and will accept only Read Status instruction. If the cycle time is correct, the microprocessor need not check this flag before each instruction, which improves the microprocessor performance.

DATA TRANSFER

The KS0717 uses a bus holder and an internal data bus for data transfer with MPU. When writing data from the MPU to an on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 2. And when reading data from an on-chip RAM to MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 6.3. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the Read Display Data instruction right after the address sets, but can be output at the second read of data.

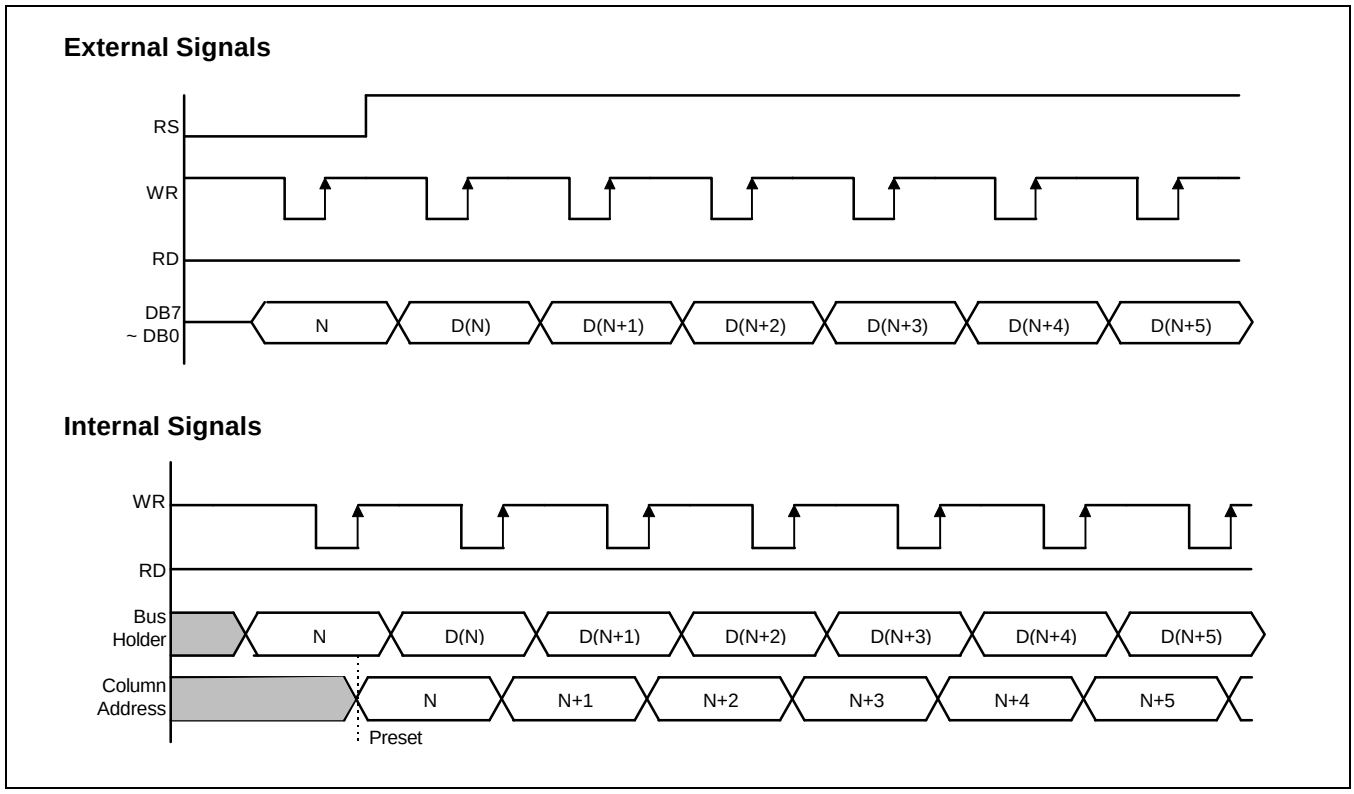


Figure 4. Write Timing

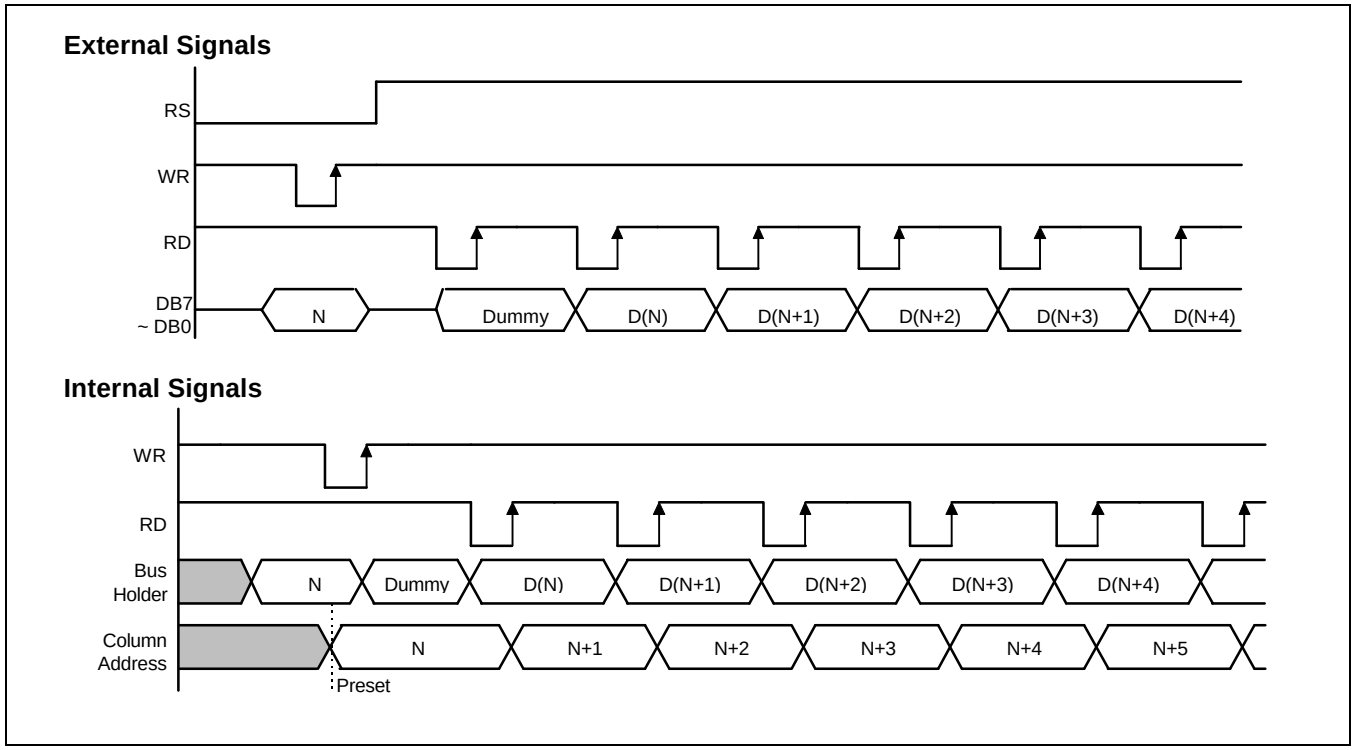


Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The display data RAM stores pixel data for the LCD. It is a 65-row ((8 page by 8-bit) + 1) by 100-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the ninth page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in Figure 6.

The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is displayed without causing the LCD to flicker.

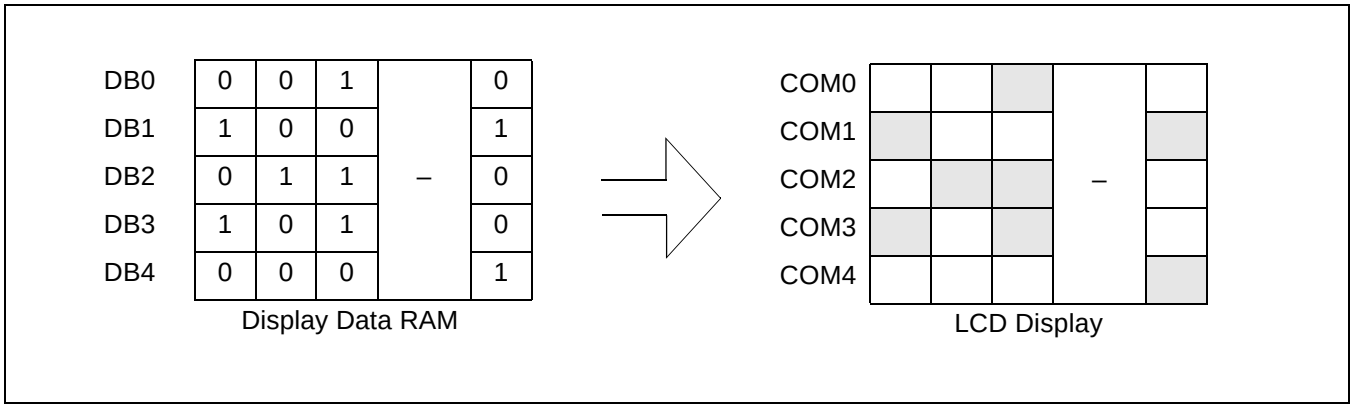


Figure 6. RAM-to-LCD Data Transfer

PAGE ADDRESS CIRCUIT

The function of this circuit is to provide a page address to the display data RAM shown in Table 7. It incorporates a 4-bit page address register changed only by the set page instruction. Page address 8 (DB3 is high, but DB2, DB1 and DB0 are low) is a special RAM area for icons, and only display data DB0 is valid. When page address is above 8, it is impossible to access the on-chip RAM.

LINE ADDRESS CIRCUIT

This circuit assigns DDRAM a line address corresponding to the first line (COM0) of the display. Therefore, by setting the line address repeatedly, it is possible to scroll the screen and switch the page without changing the contents of the on-chip RAM (refer to Table 7). It incorporates a 6-bit line address register which can only be changed by the Initial display line instruction and a 6-bit counter circuit. At the beginning of each LCD frame, the contents of a register are copied to the line counter which is increased by the CL signal, and generates the line address for transferring the 100-bit RAM data to the 100 display data latch circuit. However, display data of icons are not scrolled because the microprocessor cannot access the line address of icons.

COLUMN ADDRESS CIRCUIT

Column address circuit has a 7-bit preset counter that provides column address to the display data RAM (shown in Table 7). When Set Column Address MSB / LSB instruction is issued, 7-bit [Y6:Y0] is updated. Since this address is increased by 1 each time there is a Read or Write Data instruction, the microprocessor can access the display data continuously. However, the counter is not increased and it is locked at a non-existing address above 63H. It is unlocked if a column address is set again by Set Column Address MSB/LSB instruction. The column address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. Refer to the following Table 6.

Table 6. Segment Output Direction According to ADC

SEG Output	SEG0	SEG1	SEG2	SEG3	.....	SEG96	SEG97	SEG98	SEG99
Column address [Y6:Y0]	00H	01H	02H	03H	.....	60H	61H	62H	63H
Display data	1	0	1	0		1	1	0	0
LCD panel display (ADC = 0)	■		■		.....	■	■		
LCD panel display (ADC = 1)			■	■	.....		■		■

Table 7. Display Data RAM Addressing

Page Address P3, P2, P1, P0				Data	Column Address													Line Address (HEX)	Common Output (1/55)	Common Output (1/34)
0	0	0	0	DB0							Page0							00	COM36	–
				DB1														01	COM37	–
				DB2														02	COM38	–
				DB3														03	COM39	–
				DB4														04	COM40	–
				DB5														05	COM41	–
				DB6														06	COM42	–
				DB7														07	COM43	–
0	0	0	1	DB0							Page1							08	COM44	–
				DB1														09	COM45	–
				DB2														0A	COM46	–
				DB3														0B	COM47	–
				DB4														0C	COM48	–
				DB5														0D	COM49	–
				DB6														0E	COM50	–
				DB7														0F	COM51	–
0	0	1	0	DB0							Page2							10	COM52	–
				DB1														11	COM53	–
				DB2														12	–	–
				DB3														13	–	–
				DB4														14	–	–
				DB5														15	–	–
				DB6														16	–	–
				DB7														17	–	–
0	0	1	1	DB0							Page3							18	–	–
				DB1														18	–	–
				DB2														1A	–	–
				DB3														1B	–	–
				DB4														1C	COM0	COM0
				DB5														1D	COM1	COM1
				DB6														1E	COM2	COM2
				DB7														1F	COM3	COM3
0	1	0	0	DB0							Page4							20	COM4	COM4
				DB1														21	COM5	COM5
				DB2														22	COM6	COM6
				DB3														23	COM7	COM7
				DB4														24	COM8	COM8
				DB5														25	COM9	COM9
				DB6														26	COM10	COM10
				DB7														27	COM11	COM11
0	1	0	1	DB0							Page5							28	COM12	COM12
				DB1														29	COM13	COM13
				DB2														2A	COM14	COM14
				DB3														2B	COM15	COM15
				DB4														2C	COM16	COM16
				DB5														2D	COM17	COM17
				DB6														2E	COM18	COM18
				DB7														2F	COM19	COM19

Table 7. Display Data RAM Addressing (Continued)

Page Address P3, P2, P1, P0				Data	Column Address													Line Address (HEX)	Common Output (1/55)	Common Output (1/34)
0	1	1	0	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page6							30 31 32 33 34 35 36 37	COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27	COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27
0	1	1	1	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7							Page7							38 39 3A 3B 3C 3D 3E 3F	COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35	COM28 COM29 COM30 COM31 COM32 – – –
1	0	0	0	DB0							Page8								COMS	COMS
Column Address [HEX]			ADC = 0		00	01	02	03	04	05	- - - - - -	5E	5F	60	61	62	63			
			ADC = 1		63	62	61	60	5F	5E	- - - - - -	05	04	03	02	01	00			
LCD Output					SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	- - - - - -	SEG94	SEF95	SEG96	SEG97	SEG98	SEG99			

NOTE: When the initial display line address is 1CH.

LCD DISPLAY CIRCUITS

OSCILLATOR

This is a completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

DISPLAY TIMING GENERATOR CIRCUIT

This circuit generates some signals to be used to displaying LCD. The display clock (CL) generated by the oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of the on-chip RAM is generated in synchronization with the display clock (CL). While the 100-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor.

The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. 2-frame AC driver waveforms and internal timing signal are shown in Figure 7. When this KS0717 is used for multi-chip, the slave chip must receive the M, CL, DISP signals from the master. Table 8. shows the M, CL, and DISP status.

Table 8. Master and Slave Signal Status

Operation Mode	Oscillator ON / OFF	M	CL	DISP
Master	ON (internal clock used)	Output	Output	Output
	OFF (external clock used)	Output	Input	Output
Slave	–	Input	Input	Input

DISPLAY DATA LATCH CIRCUIT

This latch circuit temporarily stores the output display data from the display data RAM to the LCD driver in each instruction period. This latch circuit is controlled by the display ON / OFF, reverse display ON / OFF, and entire display ON / OFF instructions. The data in the display data RAM remains unchanged.

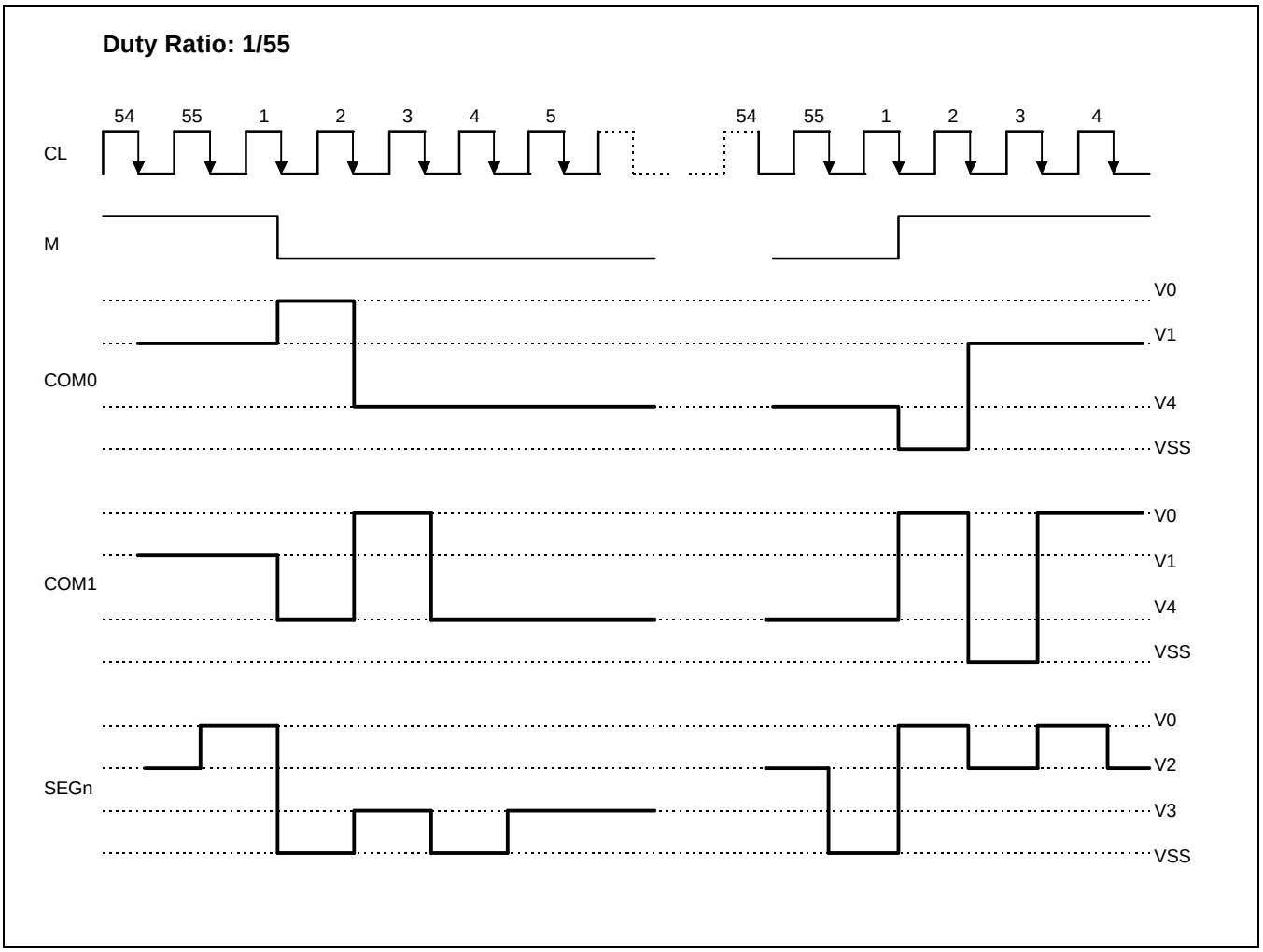


Figure 7. 2-Frame AC Driving Waveform

COMMON OUTPUT CONTROL CIRCUIT

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select instruction specifies the scanning direction of the common output pins.

Table 9. The Relationship Between Duty Ratio and Common Output

Duty	SHL	Common Output Pins			
		COM [0:16]	COM [17:37]	COM [38:53]	COMS
1/34	0	COM [0:16]	No connection	COM [17:32]	COMS
	1	COM [32:16]	No connection	COM [15:0]	COMS
1/55	0	COM [0:53]			COMS
	1	COM [53:0]			COMS

LCD DRIVER CIRCUIT

This driver circuit is configured by a 56-channel common driver and a 100-channel segment driver. This LCD panel driver voltage depends on the combination of display data and M signal.

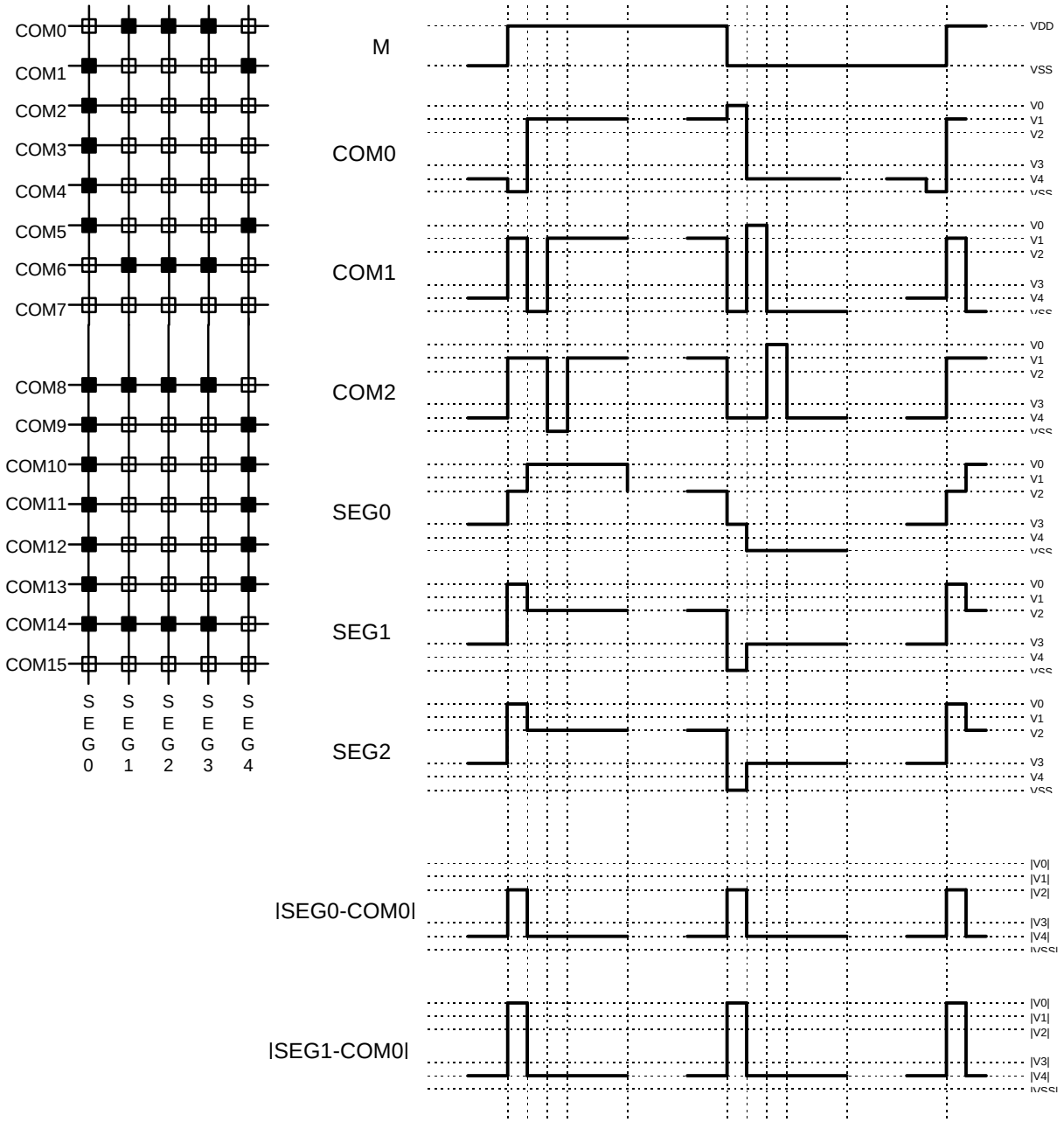


Figure 8. Segment and Common Timing

POWER SUPPLY CIRCUITS

The power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to “Instruction Description”. Table 10. shows the referenced combinations in using power supply circuits.

Table 10. Recommended Power Supply Combinations

User Setup	Power Control Register (VC VR VF)	V/C Circuits	V/R Circuits	V/F Circuits	VOUT Pin	V0 Pin	V1-V4 Pin
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External input	External input

VOLTAGE CONVERTER CIRCUITS

These circuits boost up the electric potential between V_{DD} and V_{SS} to 2, 3, 4, or 5 times toward positive side and boosted voltage is output from the VOUT pin.

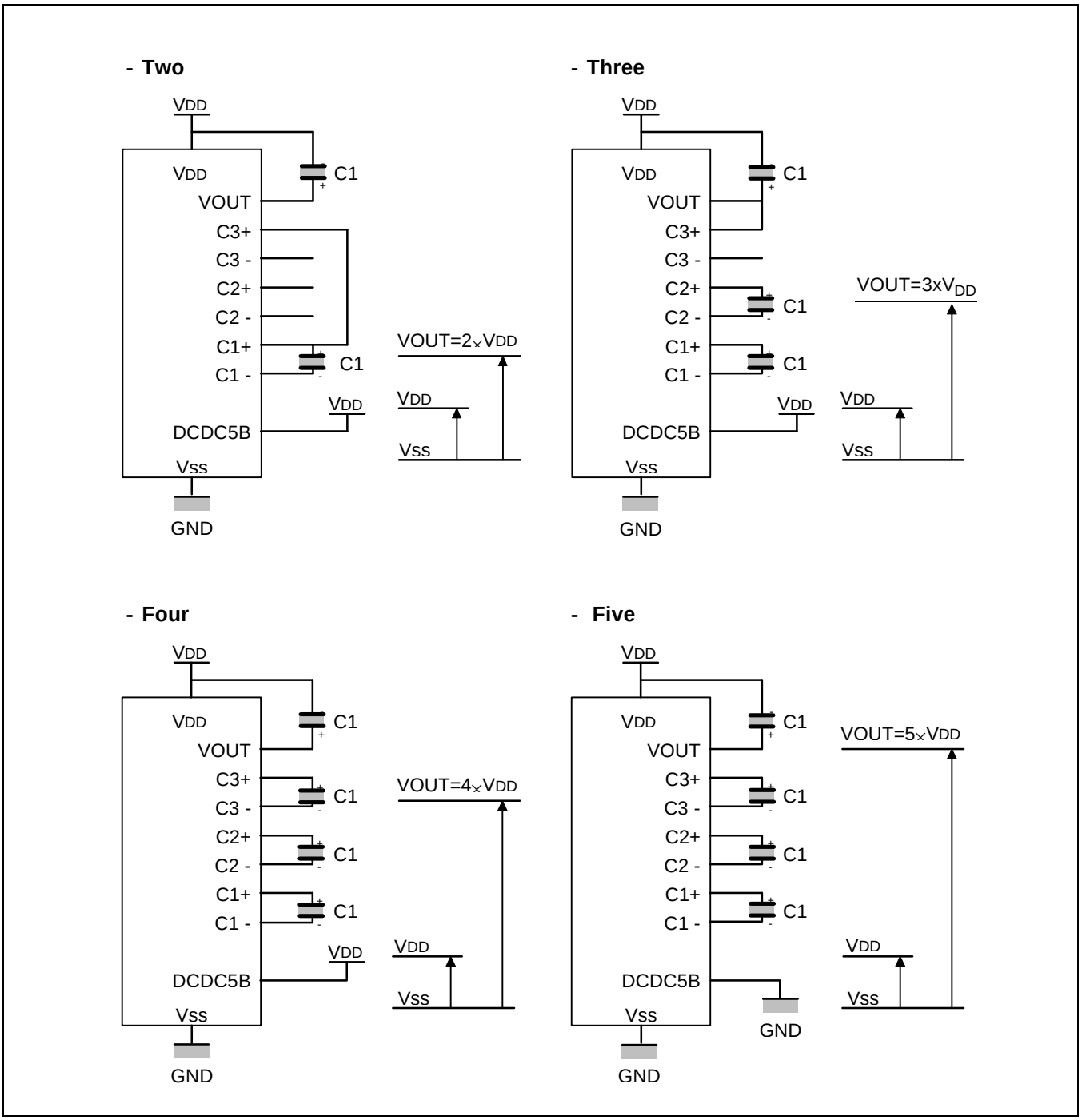


Figure 9. Boosting Two / Three / Four / Five Times Circuit

VOLTAGE REGULATOR CIRCUITS

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure. 10. it is necessary to be applied internally or externally.

For the Equation 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Equation 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in Table 11.

<Equation 1>

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V]$$

<Equation 2>

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{162}\right) \times V_{REF} \quad [V]$$

Table 11. V_{REF} Voltage at Ta = 25°C

VREFS	TEMPS	Temp. Coefficient	VREF [V]
0	0	– 0.05% / °C	2.1
	1	– 0.2% / °C	2.1
1	–	External Input	VEXT

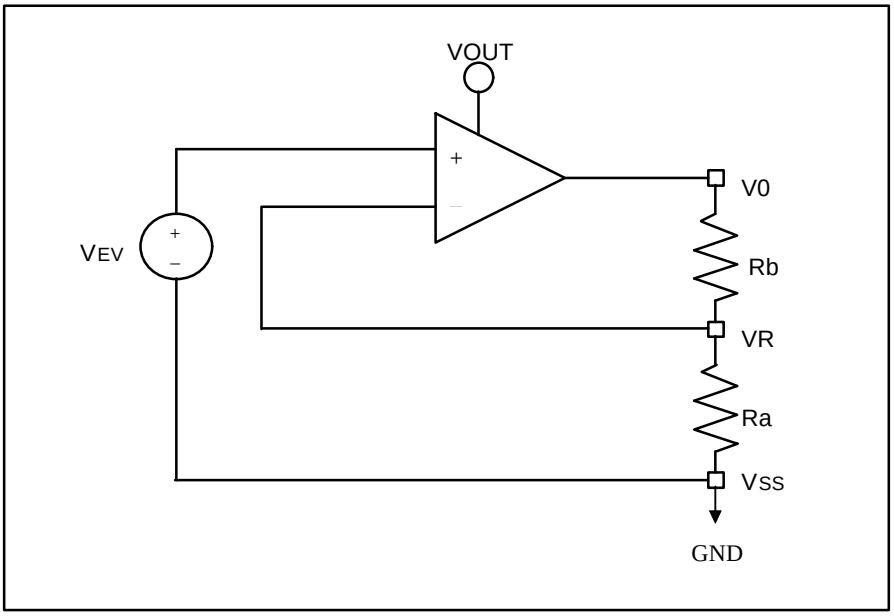


Figure 10. Internal Voltage Regulator Circuit

1) Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is high, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 12. Internal Rb/Ra Ratio Depending on 3-Bit Data (R2 R1 R0)

	3-Bit Data Settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1 + (Rb/Ra)	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.4

Figure 11. shows V0 voltage measured by adjusting internal regulator register ratio(Rb/Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25°C.

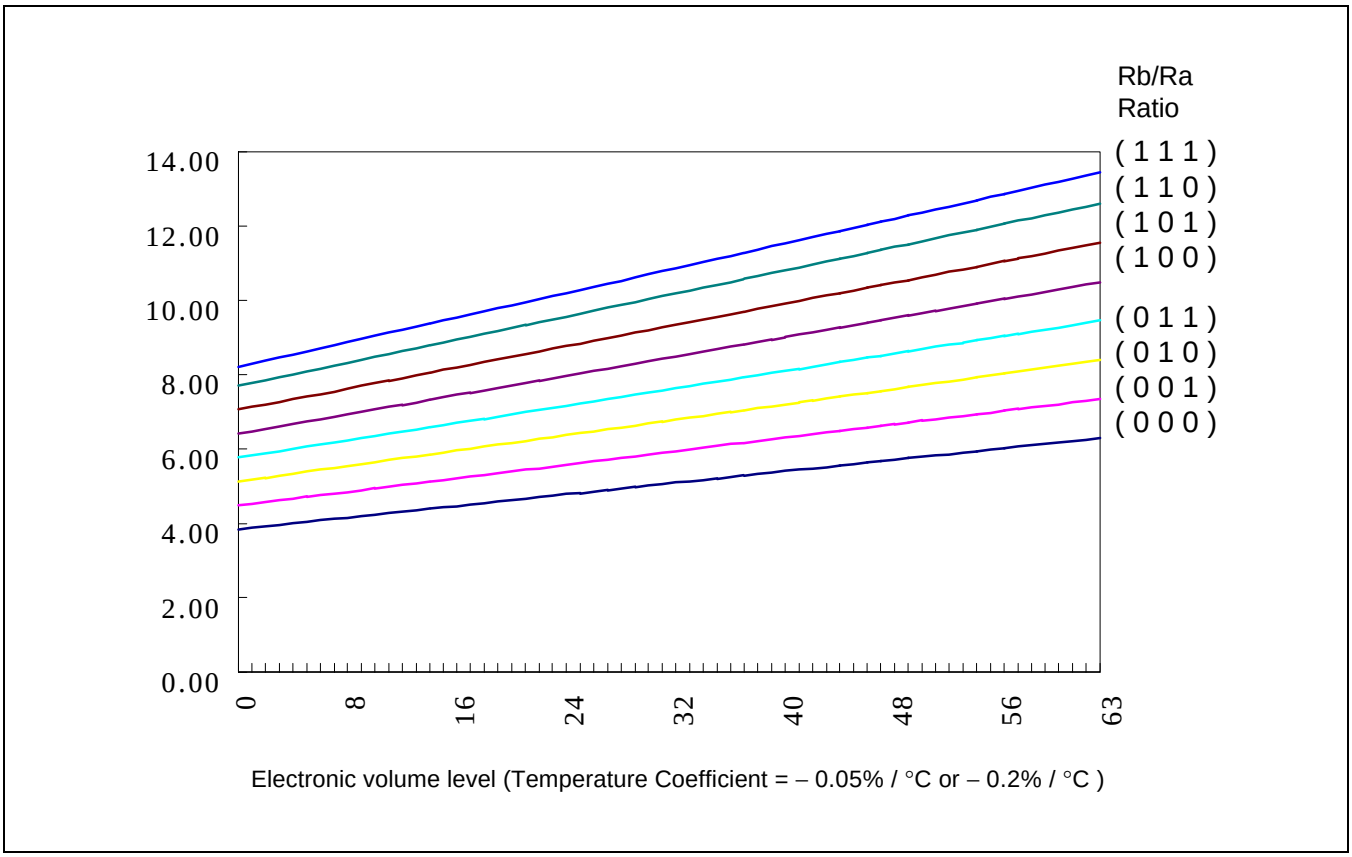


Figure 11. V0 Voltage

2) Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is low, it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements.

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1μA

<Equation 3> From Equation 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \text{ [V]}$$

<Equation 4> From Equation 1

$$V_{EV} = \left(1 - \frac{(63 - 32)}{162}\right) \times 2.1 = 1.698 \text{ [V]}$$

<Equation 5> From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \text{ [μA]}$$

From equations Equation 3, 4 and 5:

Ra = 1.69 [Ω]

Rb = 8.31 [Ω]

Table 13. shows the range of V0 depending on the above requirements.

Table 13. The Range of V0 Depending

	Electronic Volume Level				
	0	.....	32	.....	63
V0	7.59	.....	10.00	.....	12.43

VOLTAGE FOLLOWER CIRCUITS

V_{LCD} voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower for increasing drive capability. Table 14. shows the relationship between V1–V4 level and each duty ratio.

Table 14. The Relationship Between V1 - V4 Level and Each Duty Ratio

Duty Ratio	DUTY Pin	LCD Bias	V1	V2	V3	V4
1/55	1	1/8	7/8 × V0	6/8 × V0	2/8 × V0	1/8 × V0
		1/6	5/6 × V0	4/6 × V0	2/6 × V0	1/6 × V0
1/34	0	1/6	5/6 × V0	4/6 × V0	2/6 × V0	1/6 × V0
		1/5	4/5 × V0	3/5 × V0	2/5 × V0	1/5 × V0

REFERENCED POWER SUPPLY CIRCUIT FOR DRIVING LCD PANEL

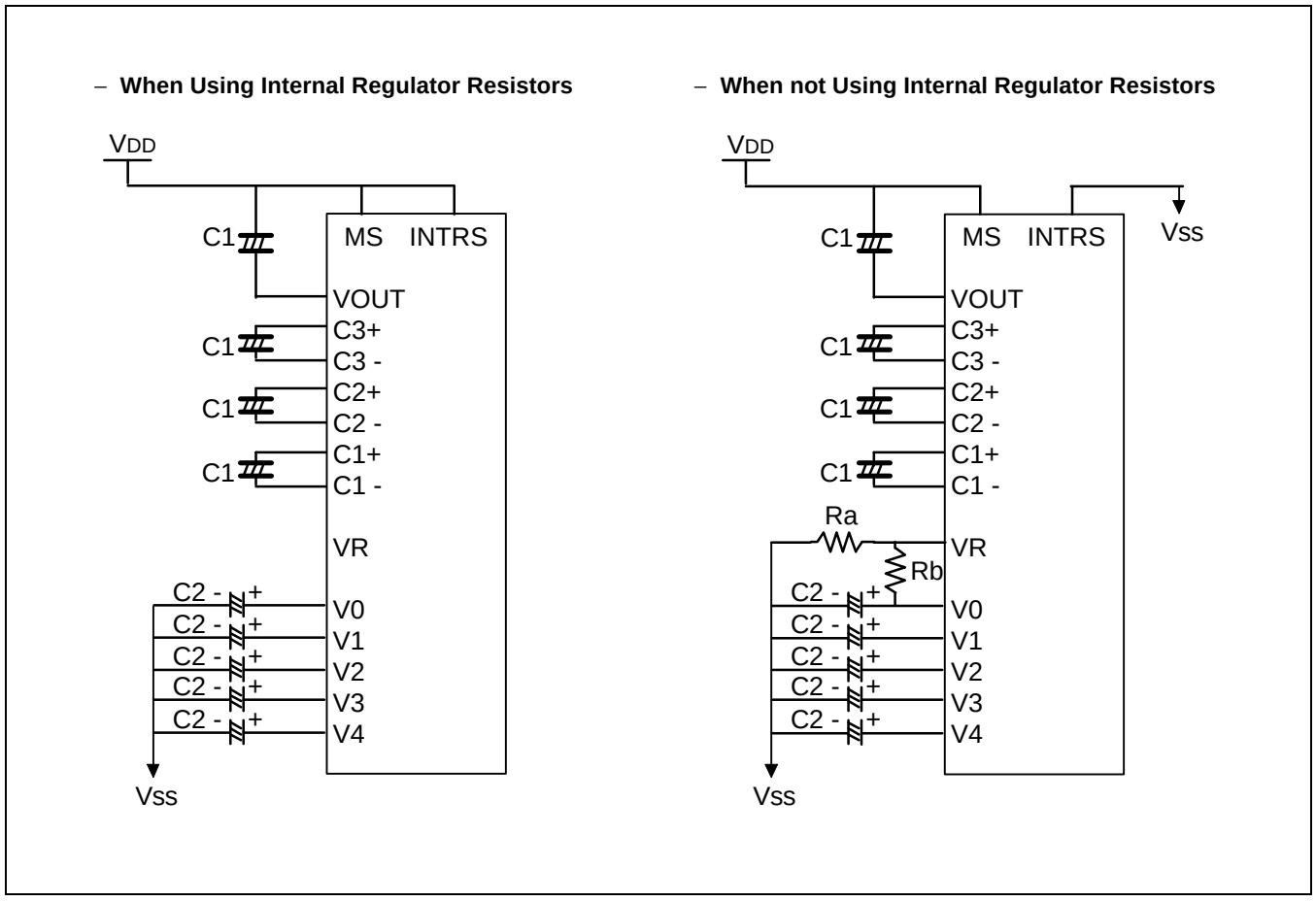


Figure 12. When Using All LCD Power Circuits (4-Times VC: On, V/R: On, V/F: On)

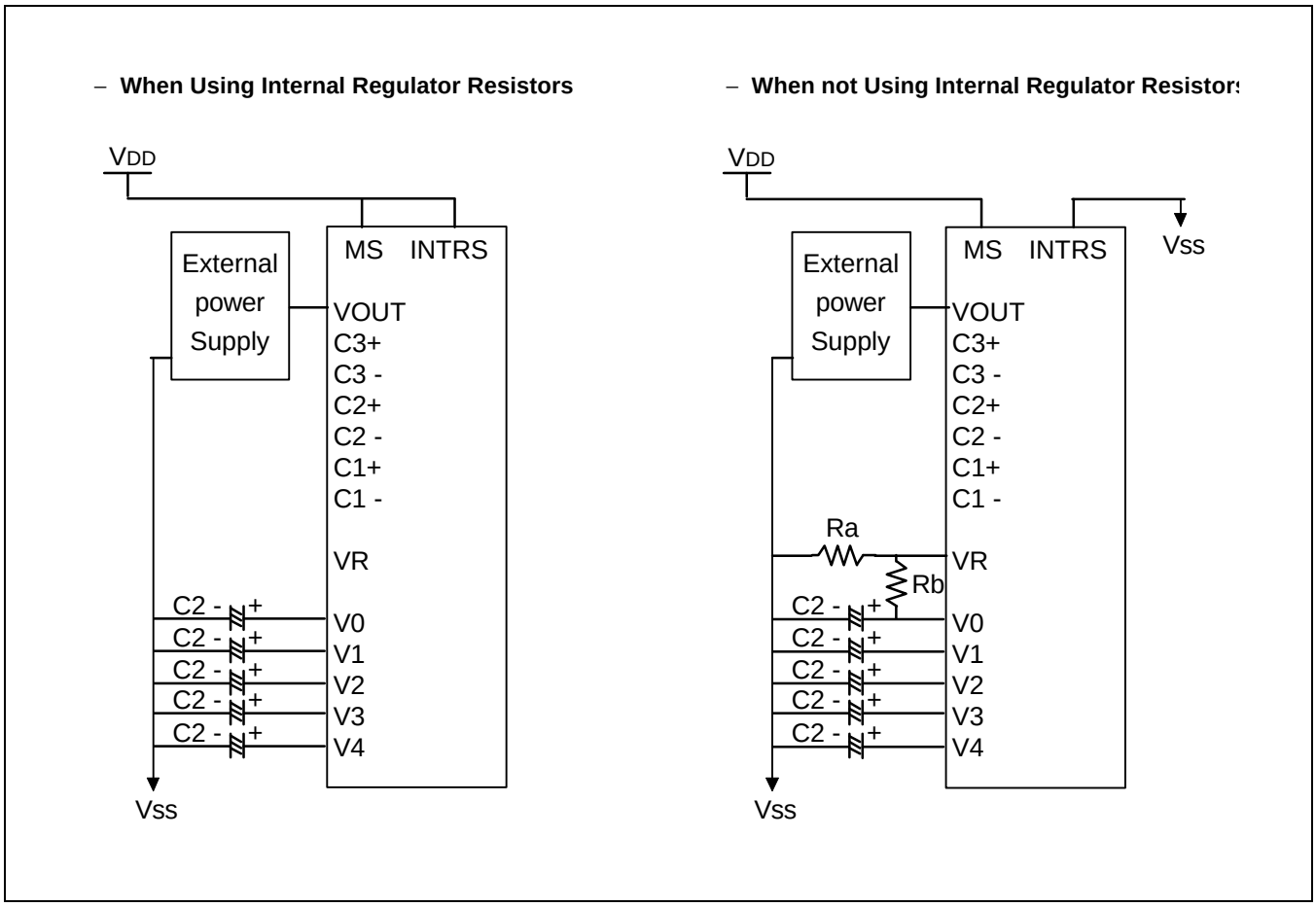


Figure 13. When Using Some LCD Power Circuits (V/C: Off, V/R: On, V/F: On)

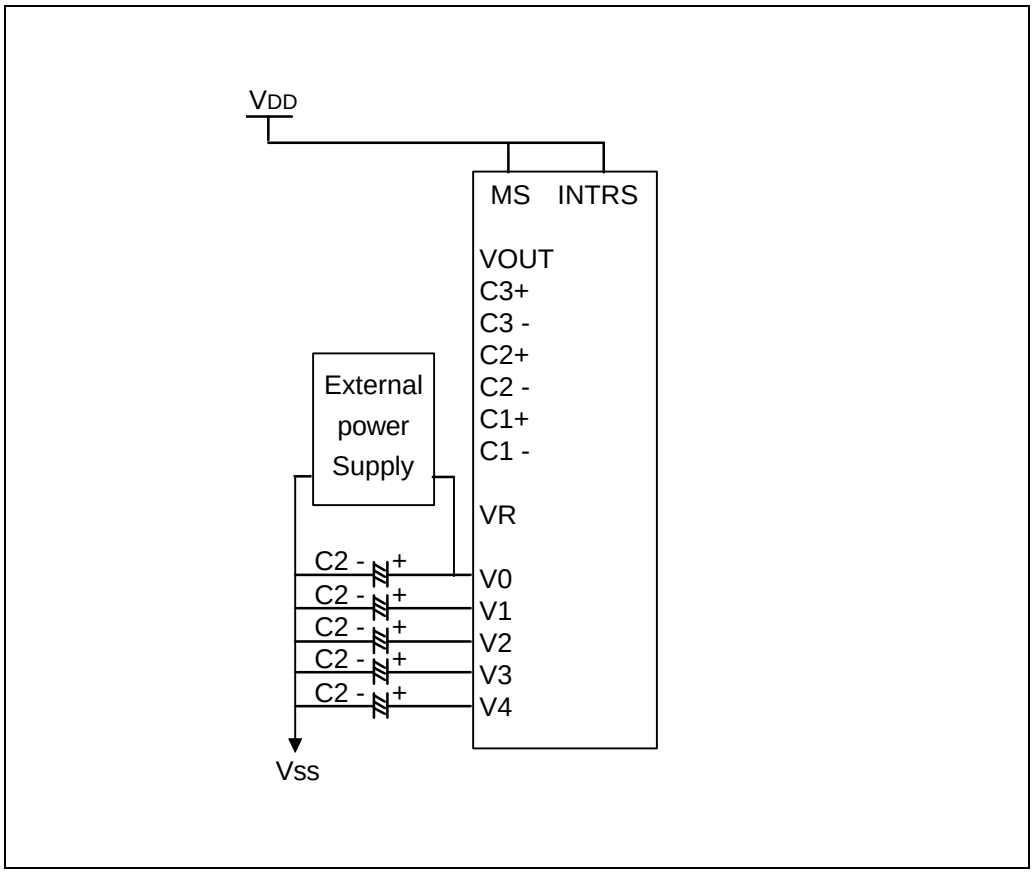


Figure 14. When Using Some LCD Power Circuits (V/C: Off, V/R: Off, V/F: On)

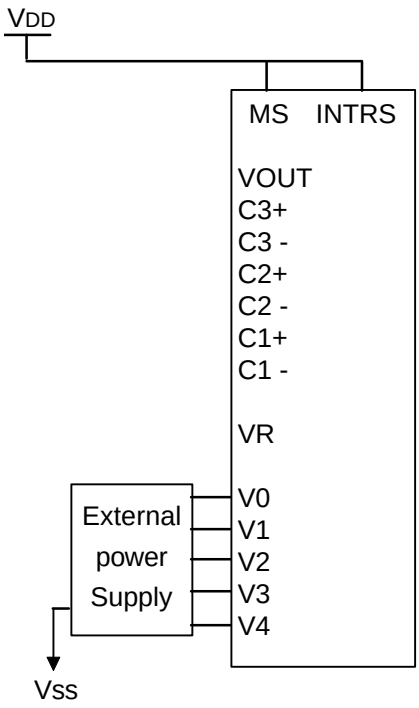


Table 15. Value of External Capacitance

Item	Value	Unit
C1	1.0 to 4.7	μF
C2	0.47 to 1.0	

Figure 15. When Not Using Any Internal LCD Power Circuits (V/C: Off, V/R: Off, V/F: Off)

RESET CIRCUIT

Internal function can be initialized by setting RESETB to low or Reset instruction.

When RESETB becomes low, following procedure occurs.

- Display ON/OFF:OFF
- Entire display ON/OFF: OFF (Normal)
- ADC select: OFF (Normal)
- Reverse display ON/OFF: OFF (Normal)
- Power control register (VC, VR, VF) = (0, 0, 0)
- LCD bias ratio: 1/8 (1/55 Duty), 1/6 (1/34 Duty)
- Modify-read: OFF
- SHL select: 0
- Static indicator mode: OFF
  Static indicator register: (S1, S0) = (0, 0)
- Display start line: 0 (First)
- Column address: 0
- Page address: 0
- Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
- Reference voltage set: OFF,
  Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

When RESET instruction is issued, following procedure occurs.

- Modify-read: OFF
- Static indicator mode: OFF
  Static indicator register: (S1, S0) = (0, 0)
- SHL select: 0
- Display start line: 0 (First)
- Column address: 0
- Page address: 0
- Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
- Reference voltage set: OFF
  Reference voltage control register (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

While RESETB is low or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes low, any instruction can be accepted.

RESETB pin must be connected to the reset pin of MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB pin is essential before used.

INSTRUCTION DESCRIPTION

Table 16. Instruction Table

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON/ OFF	RESETB	0	0	0	0	Read the internal status
Display ON/OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON/OFF LCD panel When DON=0, display is OFF When DON=1, display is On
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC=0 normal direction (SEG0 → SEG99) When ADC=1 reverse direction (SEG99 → SEG0)
Reverse display ON/ OFF	0	0	1	0	1	0	0	1	1	REV	Select normal/reverse display When REV=0 normal When REV=1 reverse
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	Select normal display / entire display ON When EON=0, normal display When EON=1, entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL=0 normal direction (COM0 → COM53) When SHL=1 reverse direction (COM53 → COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select resistance ratio of the regulator resistor
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode

Table 16. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	–	–	–	–	–	–	–	–	–	–	Compound instruction of display OFF and entire display ON
Test instruction	0	0	1	1	1	1	×	×	×	×	Don't use this instruction

NOTE: "×" = Don't care

READ DISPLAY DATA

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**1**	**Read Data**							

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

WRITE DISPLAY DATA

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**0**	**Write Data**							

8-bit display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

READ STATUS

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**BUSY**	**ADC**	**ON/OFF**	**RESETB**	**0**	**0**	**0**	**0**

Indicates the internal status conditions.

Flag	Description
BUSY	The device is busy when carrying out internal operation or reset. All instructions are rejected until BUSY goes to low. 0: Chip is active, 1: Chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: Reverse direction (SEG99 → SEG0), 1: Normal direction (SEG0 → SEG99)
ON/OFF	Indicates display ON / OFF status. 0: Display ON, 1: Display OFF
RESETB	Indicates initialization is in progress by RESETB signal. 0: Chip is active, 1: Chip is being reset.

DISPLAY ON/OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**DON**

Turns the display ON or OFF

DON	
1	Display ON
0	Display OFF

INITIAL DISPLAY LINE

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**1**	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**

Sets the line address of display RAM to determine the initial display line. The RAM display data is displayed at the top row (COM0) of the LCD panel.

ST5	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**	**Line Address**
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

REFERENCE VOLTAGE SELECT

Set reference voltage mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Set reference voltage register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**´**	**´**	**SV5**	**SV4**	**SV3**	**SV2**	**SV1**	**SV0**

Consists of two bytes instruction. The first byte sets reference voltage mode, the second one updates the contents of reference voltage register. After second instruction reference voltage mode is released.

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

SET PAGE ADDRESS

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**1**	**P3**	**P2**	**P1**	**P0**

Sets the page address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the column address, the page address defines the address of the display RAM to write or read display data. changing the page address doesn't affect the display status.

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

SET COLUMN ADDRESS

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**1**	**0**	**Y6**	**Y5**	**Y4**

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**0**	**Y3**	**Y2**	**Y1**	**Y0**

Sets the column address of the display RAM from the microprocessor into the column address register. The column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased, starting with the address stored in the column address register and continuously rotating right.

Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99

ADC SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**ADC**

Changes the relationship between the RAM column address and segment driver. The direction of the segment driver output pins can be reversed by software. This makes the IC layout flexible in the LCD module assembly.

ADC	
0	Normal direction (SEG0 → SEG99)
1	Reverse direction (SEG99 → SEG0)

NORMAL / REVERSE DISPLAY

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**REV**

Reverses the display status on the LCD panel without rewriting the contents of the display data RAM.

REV	RAM Bit Data = “1”	RAM Bit Data = “0”
0 (Normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (Reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

ENTIRE DISPLAY ON / OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**EON**

Forces all LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are put on hold. This instruction has priority over the reverse display ON / OFF instruction.

EON	
0	Normal display
1	Entire display on

LCD BIAS SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**BIAS**

Selects the LCD bias ratio of the voltage required for driving the LCD.

Duty Ratio	DUTY	LCD Bias	
		BIAS = 0	BIAS = 1
1/55	1	1/8	1/6
1/34	0	1/6	1/5

SET MODIFY-READ

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data. It reduces the load of the microprocessor when the data of a specific area is repeatedly changed during cursor blinking. This mode is canceled by the reset modify-read instruction.

RESET MODIFY-READ

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This instruction cancels the modify read mode, and makes the column address return to its initial value just before the set modify read instruction starts.

RESET

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This instruction resets the initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply which is initialized by the RESETB pin.

SHL SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**0**	**0**	**SHL**	´	´	´

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

SHL	
0	Normal direction (COM0 → COM53)
1	Reverse direction (COM53 → COM0)

POWER CONTROL

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**1**	**VC**	**VR**	**VF**

Selects one out of eight power circuit functions by using a 3-bit register. An external power supply and a part of internal power supply functions can be used simultaneously.

VC, VR, VF	
0	Off
1	On

REGULATOR RESISTOR SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**0**	**R2**	**R1**	**R0**

Selects resistance ratio of the resistor used in the Voltage Regulator. See Voltage Regulator section in Power Supply Circuit.

R2	**R2**	**R2**	**[Rb/Ra] Ratio**
0	0	0	Small
0	0	1	:
:	:	:	:
1	1	0	:
1	1	1	Large

SET STATIC INDICATOR STATE

Set Static Indicator Mode (On / Off)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**SM**

SM	
0	Static Indicator Off
1	Static Indicator On

Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	×	×	×	×	×	×	**S1**	**S0**

This instruction sets the static indicator ON / OFF. When it is on, the static indicator operates and blinks at an interval of approximately one second.

S1	**S0**	**Status of Static Indicator Output**
0	0	OFF
0	1	ON (About 1 second blinking)
1	0	ON (About 0.5 second blinking)
1	1	ON (Always ON)

POWER SAVE (COMPOUND INSTRUCTION)

If the entire display ON / OFF instruction is issued during the display OFF state, KS0717 enters the power save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one mode of sleep and standby mode. When static indicator mode is ON, standby mode is issued. When OFF, sleep mode is issued. Power save mode is released by the display ON & entire display OFF instruction.

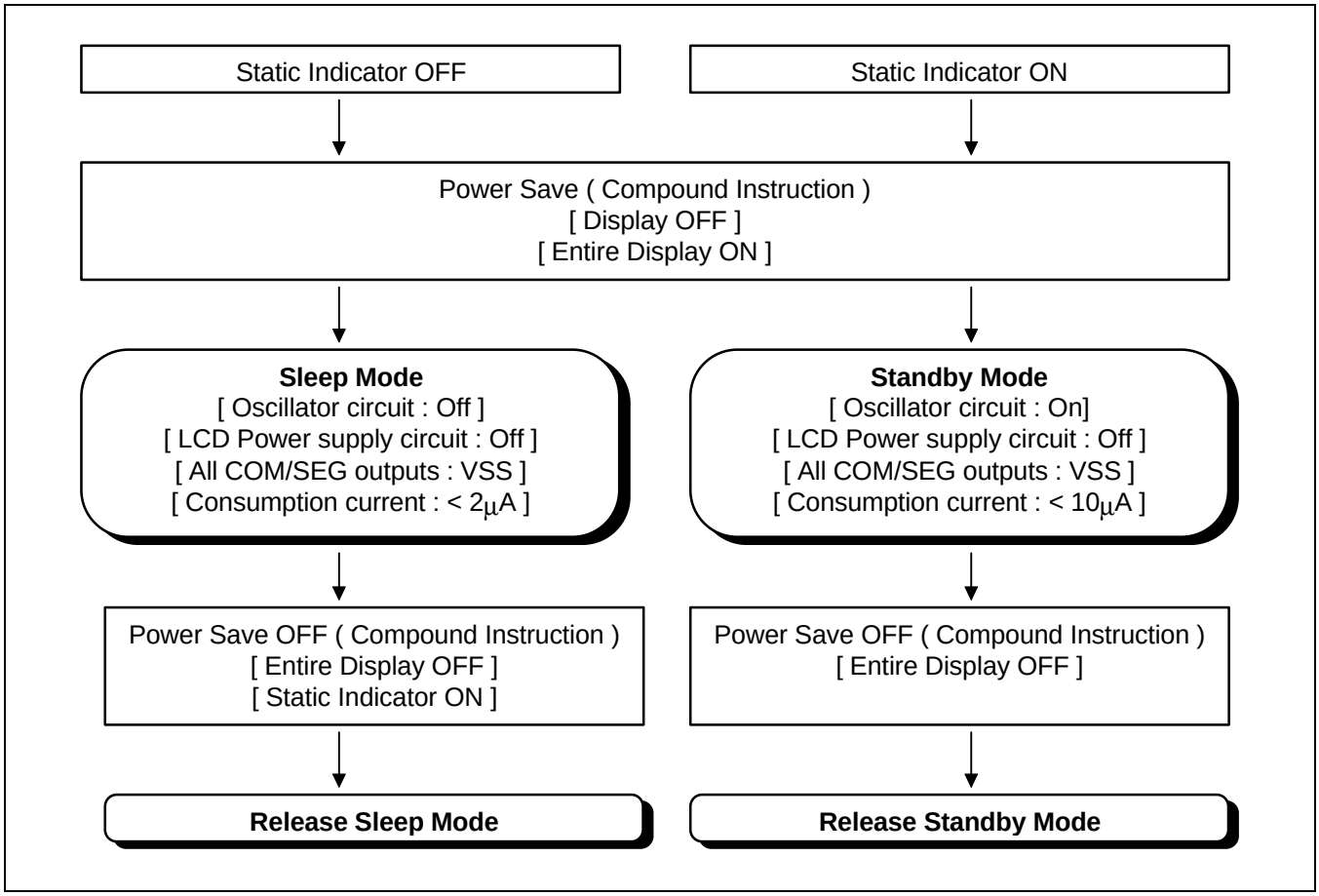


Figure 16. Power Save (Compound Instruction)

REFERENTIAL INSTRUCTION SETUP FLOW

— Initializing with the built-in power supply circuits

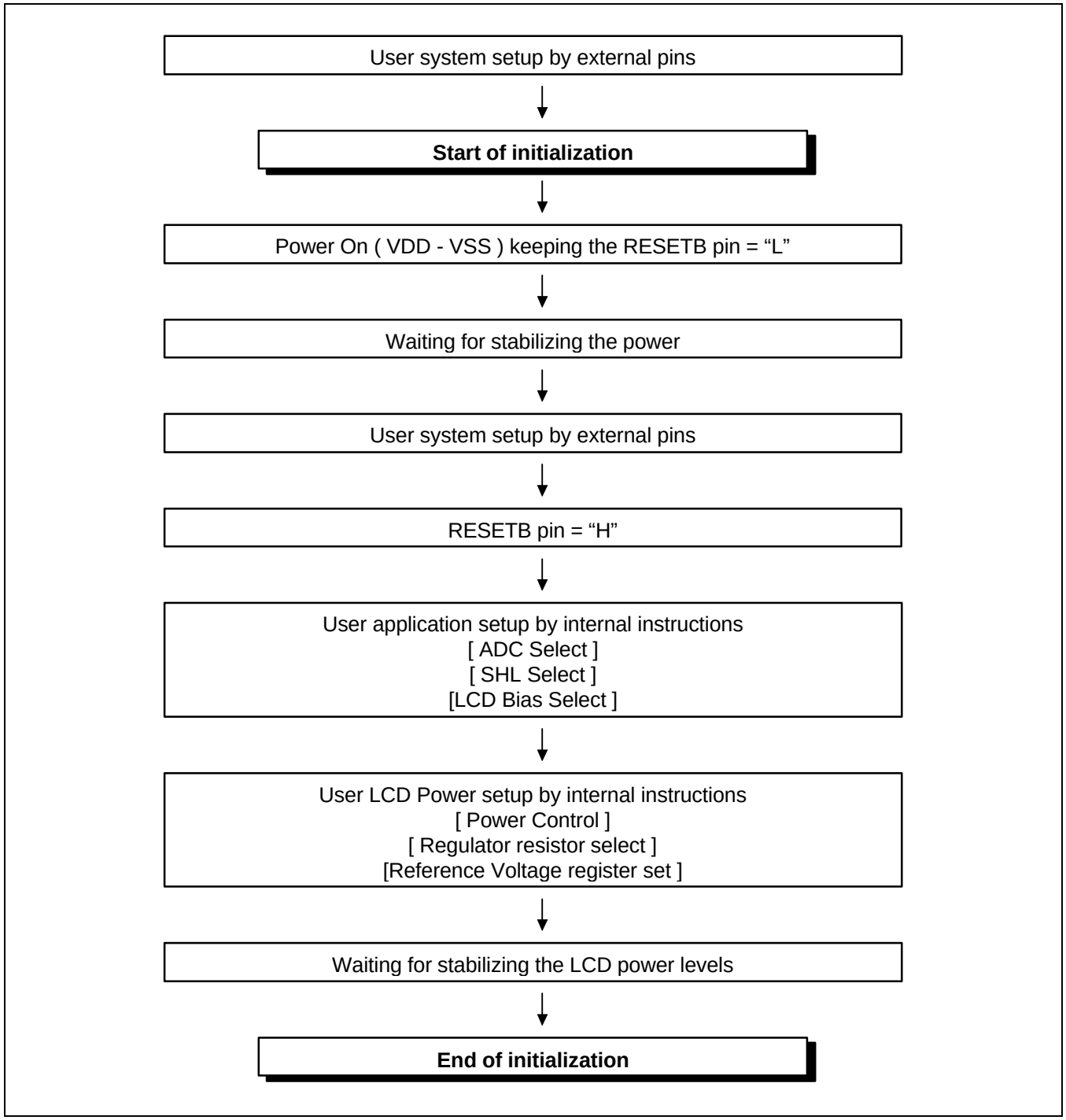


Figure 17. Initializing With The Built-in Power Supply Circuits

— Initializing without the built-in power supply circuits

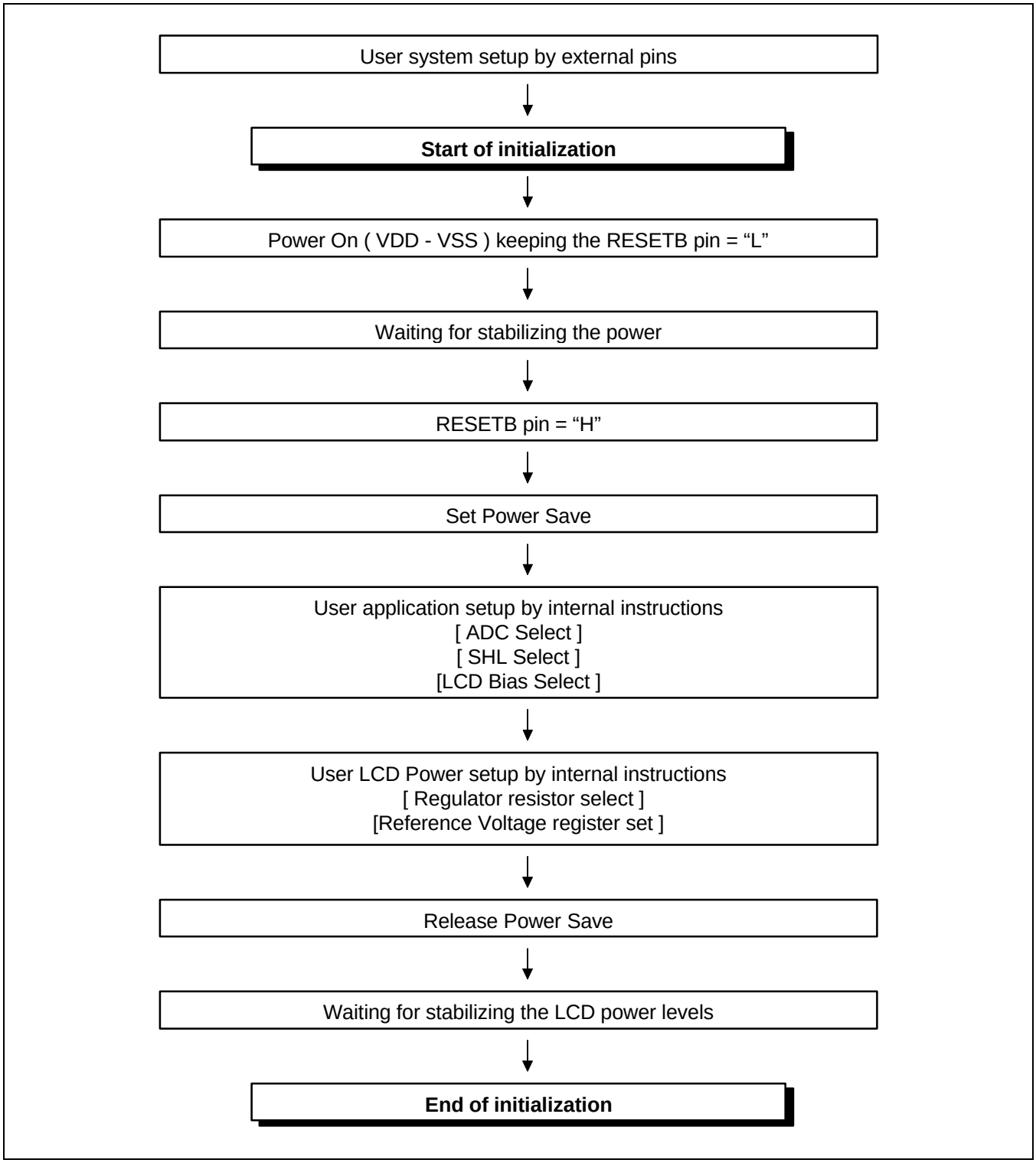


Figure 18. Initializing Without the Built-In Power Supply Circuits

— Data displaying

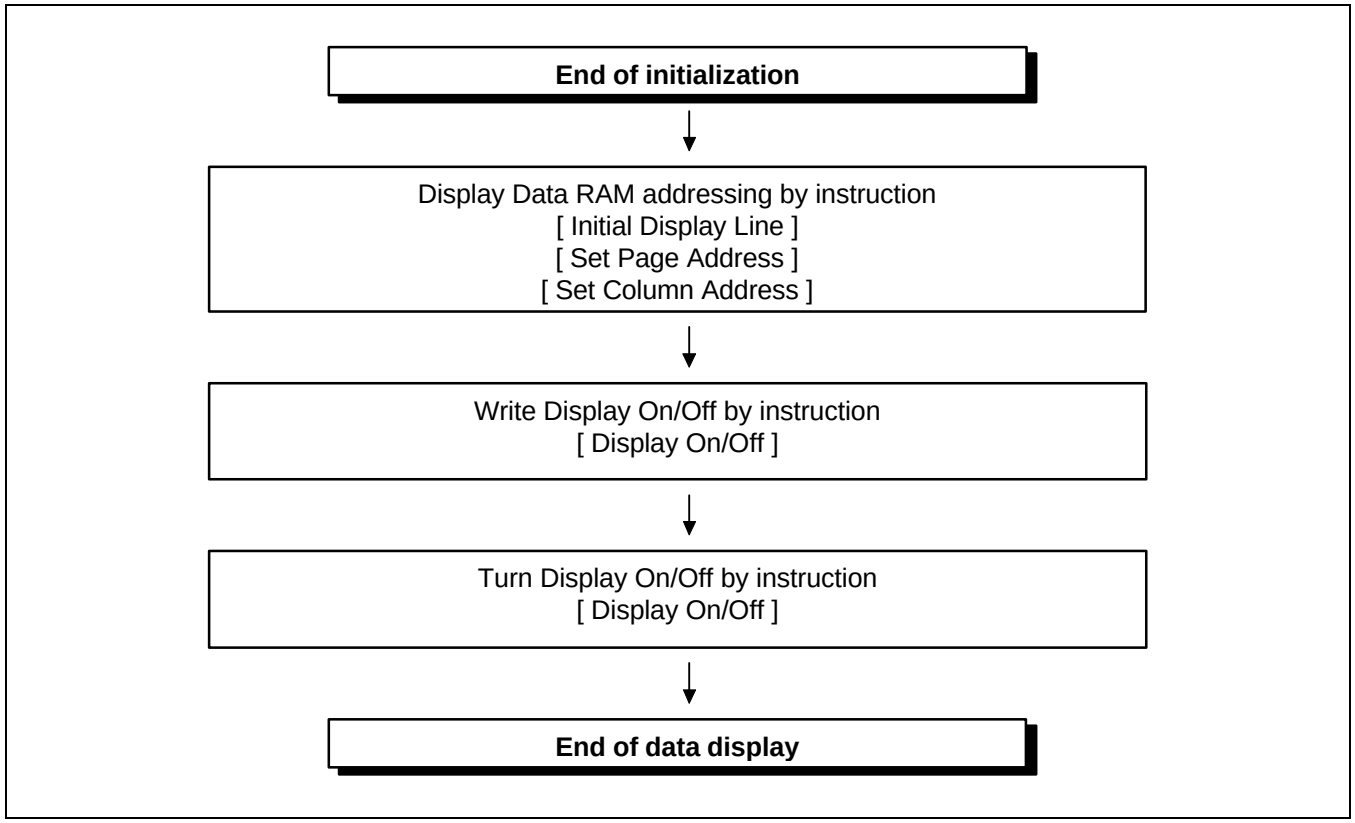


Figure 19. Data Displaying

— Power Off

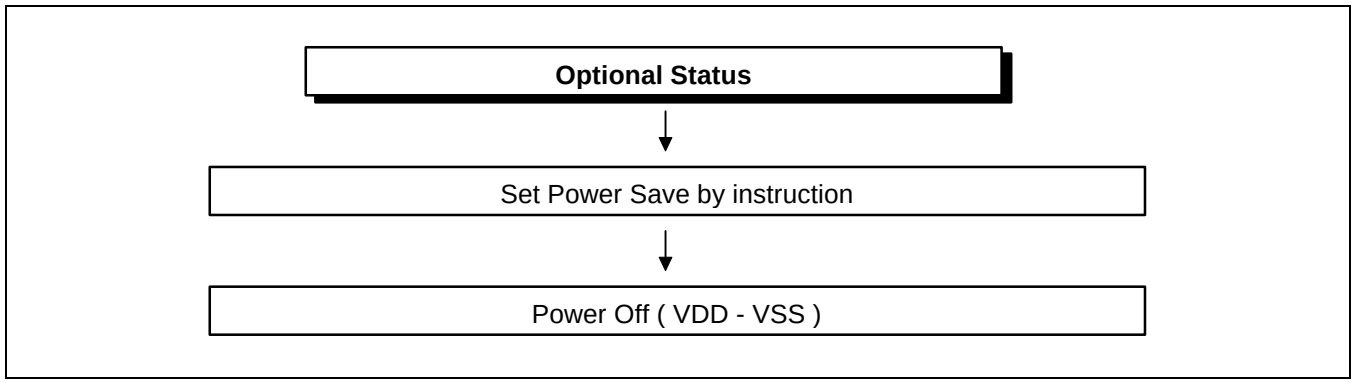


Figure 20. Power Off

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 17. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	– 0.3 to + 7.0	V
	V_{LCD}	+ 0.3 to + 17.0	
Input voltage range	V_{IN}	– 0.3 to V_{DD} + 0.3	
Operating temperature range	T_{OPR}	– 40 to + 85	°C
Storage temperature range	T_{STR}	– 55 to + 125	

NOTES:
1. V_{DD} and V_{LCD} are based on V_{SS} = 0 V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS} must always be satisfied (V_{LCD} = V0 – V_{SS}).
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 18. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Pin Used
Operating voltage (1)		V_{DD}	–	2.4	–	5.5	V	V_{DD} (1)
Operating voltage (2)		V0	–	4.0	–	15.0		V0 (2)
Input voltage	High	V_{IH}	–	0.8 V_{DD}	–	V_{DD}		(3)
	Low	V_{IL}	–	V_{SS}	–	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = – 0.5mA	0.8 V_{DD}	–	V_{DD}		(4)
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	–	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	– 1.0	–	+ 1.0	µA	(5)
Output Leakage Current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	– 3.0	–	+ 3.0		(6)
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	–	2.0	3.0	kΩ	SEGn COMn (7)
Oscillator frequency (1)	Internal	f_{OSC}	Ta = 25°C, Duty ratio = 1/55	11.2	14	16.8	kHz	CL (8)
	External	f_{CL}		3.73	4.67	5.61		
Oscillator frequency (2)	Internal	f_{OSC}	Ta = 25°C, Duty ratio = 1/34	11.2	14	16.8		CL (8)
	External	f_{CL}		2.24	2.80	3.36		

Table 18. DC Characteristics (Continued)

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item	Symbol	Condition		Min	Typ	Max	Unit	Pin Used
Voltage Converter / Regulator / Follower								
Voltage converter input voltage	V_{DD}	×2		2.4	–	5.5	V	V_{DD}
		×3		2.4	–	5.0		
		×4		2.4	–	3.75		
		×5		2.4	–	3.0		
Voltage converter output voltage	VOUT	×2/×3/×4/×5 voltage conversion (no-load)		95	99	–	%	VOUT
Voltage regulator operating voltage	VOUT	–		4.0	–	15.0	V	VOUT
Voltage follower operating voltage	V0	–		4.0	–	15.0		V0 (9)
Reference voltage	V_{REF0}	T_a = 25°C	– 0.05%/°C	2.04	2.10	2.16		(10)
	V_{REF1}		– 0.2%/°C	2.04	2.10	2.16		(10)
Dynamic Current Consumption (1): When the built-In circuits is OFF (At Operate Mode).								
Dynamic current consumption (1)	I_{DD1}	VDD = 3.0V, V0 – VSS = 11.0V, 1/55 duty ratio, checker pattern		–	–	50	µA	(11)
Dynamic Current Consumption (2): When the built-in circuits is ON (At Operate Mode).								
Dynamic current consumption (2)	I_{DD2}	VDD = 3.0V, quad boosting, V0 – VSS = 11.0V, 1/55 duty ratio, checker pattern, normal power mode		–	–	100	µA	(11)
Dynamic Current Consumption (3): When the built-in power is OFF (At Access Mode).								
Dynamic current consumption (3)	I_{DD3}	VDD = 3.0V, V0 – VSS = 11.0V, f_{cyc} = 1MHz		–	–	1	mA	
Current Consumption During Power Save Mode								
Sleep mode current	I_{DDS1}	During sleep		–	–	2.0	µA	
Standby mode current	I_{DDS2}	During standby		–	–	10.0	µA	

NOTES:

1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from MPU.
2. In case of external power supply is applied.
3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, C68, PS, INTRS, HPMB, TEMPS, VREFS, DCDC5B, CLS, CL, M, DISP pins
4. DB0 to DB7, M, FRS, DISP, CL pins
5. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, C68, PS, INTRS, HPMB, TEMPS, VREFS, DCDC5B, CLS,

CL, M, DISP pins

6. Applies when the DB0 to DB7, M, DISP, and CL pins are in high impedance.
7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
   R_{ON} = Δ V / 0.1 [kΩ] (Δ V: voltage change when ± 0.1[mA] is applied in the ON status.)
8. See Table 19. for the relationship between oscillation frequency and frame frequency.
9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
11. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU. The current consumption, when the built-in power supply circuit is on or off. The current flowing through voltage regulation resistors (Rb and Ra) is not included. It does not include the current of the LCD panel capacity, wiring capacity, etc.

Table 19. The Relationship Between Oscillation Frequency and Frame Frequency

DUTY Ratio	Item	f_{CL}	f_M	Remark
1/55	On-chip oscillator circuit is used	$\frac{f_{OSC}}{3}$	$\frac{f_{OSC}}{6 \times 55}$	• f_{OSC} = oscillation frequency • f_{CL} = display clock frequency • f_M = LCD AC signal frequency
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 55}$	
1/34	On-chip oscillator circuit is used	$\frac{f_{OSC}}{5}$	$\frac{f_{OSC}}{10 \times 34}$	
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 34}$	

AC CHARACTERISTICS

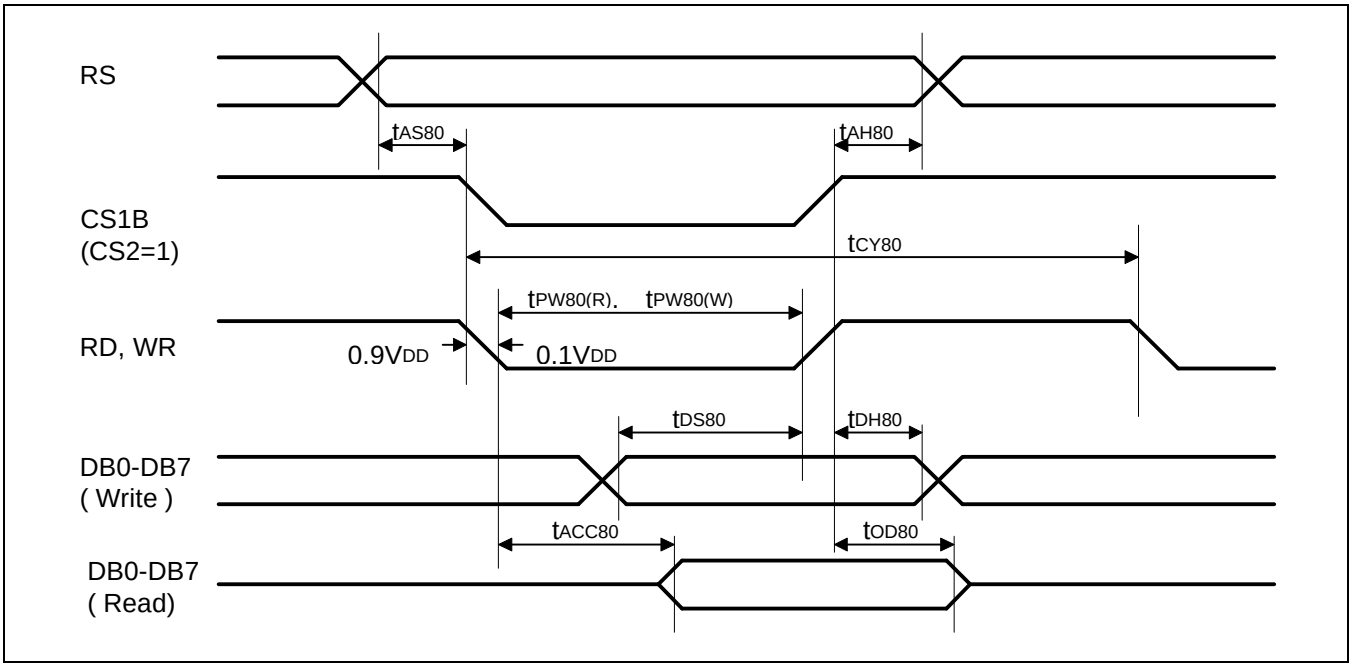


Figure 21. Read/Write Characteristics (8080-Series Microprocessor)

(V_{DD} = 2.4V to 3.3V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	13 17	–	–	ns	–
System cycle time	RS	t_{CY80}	400	–	–	ns	–
Pulse width (WR)	RW_WR	$t_{PW80(W)}$	55	–	–	ns	–
Pulse width (RD)	E_RD	$t_{PW80(R)}$	125	–	–	ns	–
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}	35 13	–	–	ns	–
Read access time Output disable time		t_{ACC80} t_{OD80}	– 10	– –	125 90	ns ns	C_L = 100pF

(V_{DD} = 4.5V to 5.5V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	10 10	–	–	ns	–
System cycle time	RS	t_{CY80}	150	–	–	ns	–
Pulse width (WR)	RW_WR	$t_{PW80(W)}$	25	–	–	ns	–
Pulse width (RD)	E_RD	$t_{PW80(R)}$	65	–	–	ns	–
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}	18 10	–	–	ns	–
Read access time Output disable time		t_{ACC80} t_{OD80}	– 10	– –	65 45	ns ns	C_L = 100pF

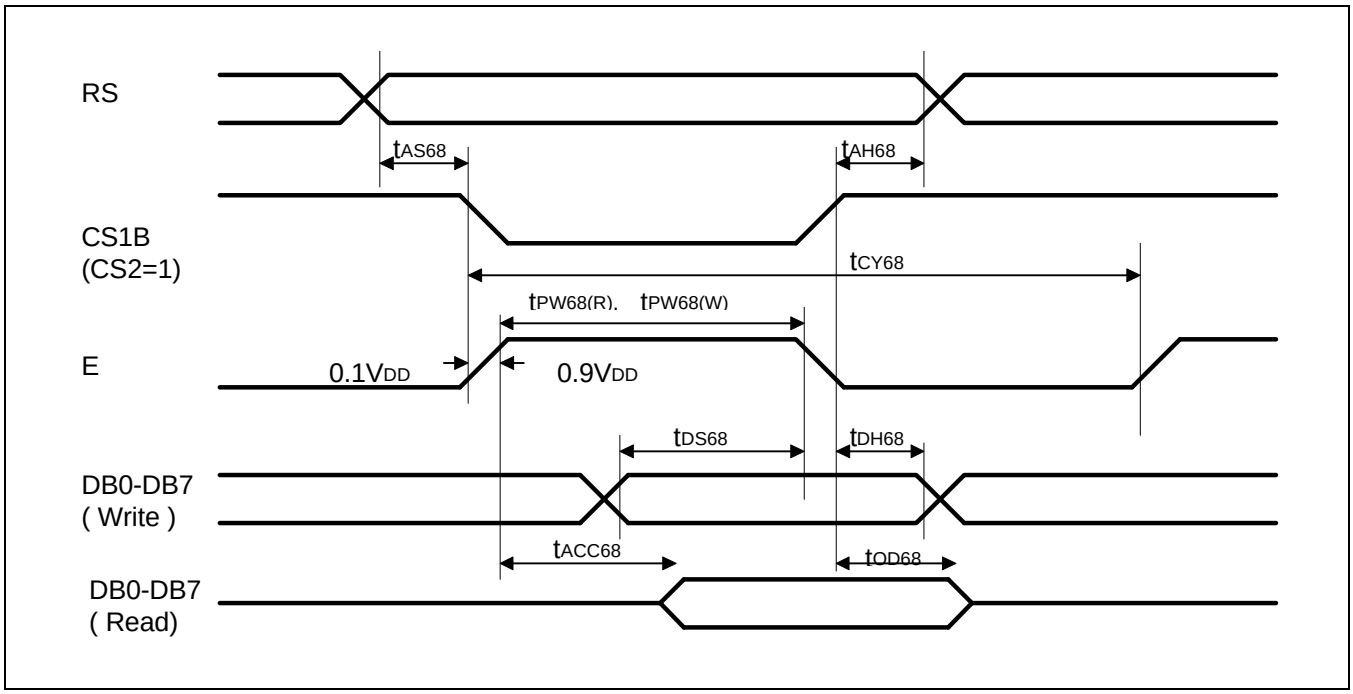


Figure 22. Read/Write Characteristics (6800-Series Microprocessor)

(V_{DD} = 2.4V to 3.3V, Ta = – 40 to + 85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	13 17	–	–	ns	–
System cycle time		RS	t_{CY68}	400	–	–	ns	–
Data setup time Data hold time		DB0 to DB7	t_{DS68} t_{DH68}	35 13	–	–	ns	–
Access time Output disable time		–	t_{ACC68} t_{OD68}	– 10	– –	125 90	ns	C_L = 100pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	125 55	–	–	–	–

(V_{DD} = 4.5V to 5.5V, Ta = – 40 to + 85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	10 10	–	–	ns	–
System cycle time		RS	t_{CY68}	150	–	–	ns	–
Data setup time Data hold time		DB0 to DB7	t_{DS68} t_{DH68}	18 10	–	–	ns	–
Access time Output disable time			t_{ACC68} t_{OD68}	– 10	– –	65 45	ns ns	C_L = 100pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	65 25	–	–	–	–

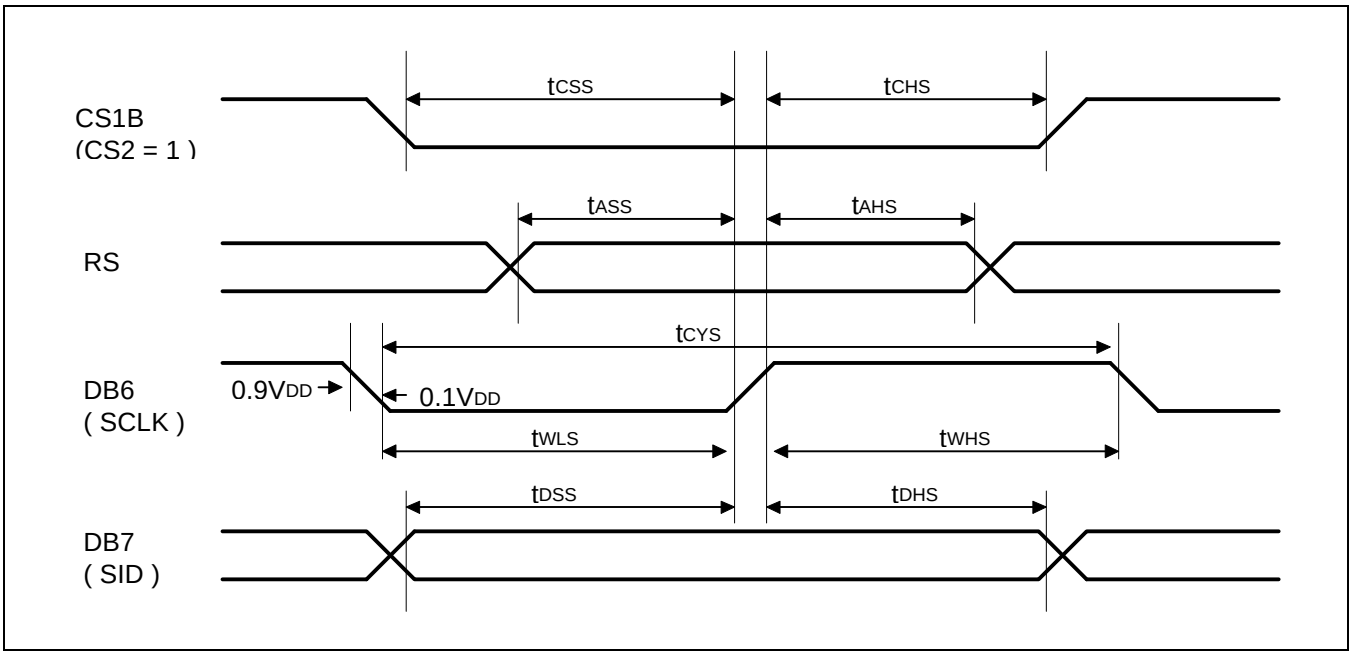


Figure 23. Serial Interface Characteristics

(V_{DD} = 2.4 V to 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	450 180 135	–	–	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	90 360	–	–	ns
Data setup time Data hold time	DB7(SID)	t_{DSS} t_{DHS}	90 90	–	–	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	55 180	–	–	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	225 90 70	–	–	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	45 180	–	–	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	45 45	–	–	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	25 90	–	–	ns

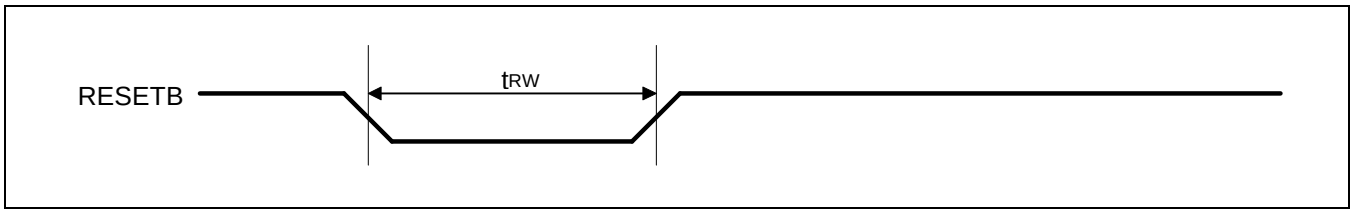


Figure 24. Reset Input Timing

(V_{DD} = 2.4 V to 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}	900	–	–	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}	450	–	–	ns

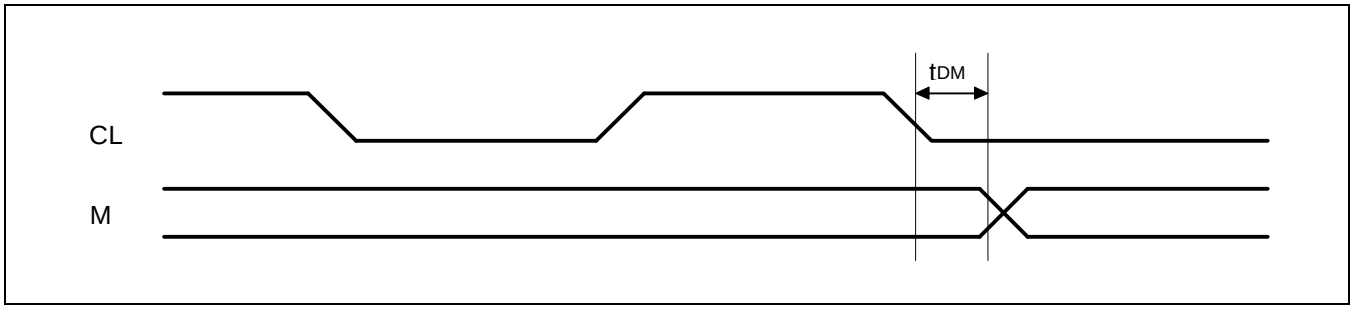


Figure 25. Display Control Output Timing

(V_{DD} = 2.4 V to 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
M delay time	M	t_{DM}	–	13	70	ns

(V_{DD} = 4.5 V to 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
M delay time	M	t_{DM}	–	10	35	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

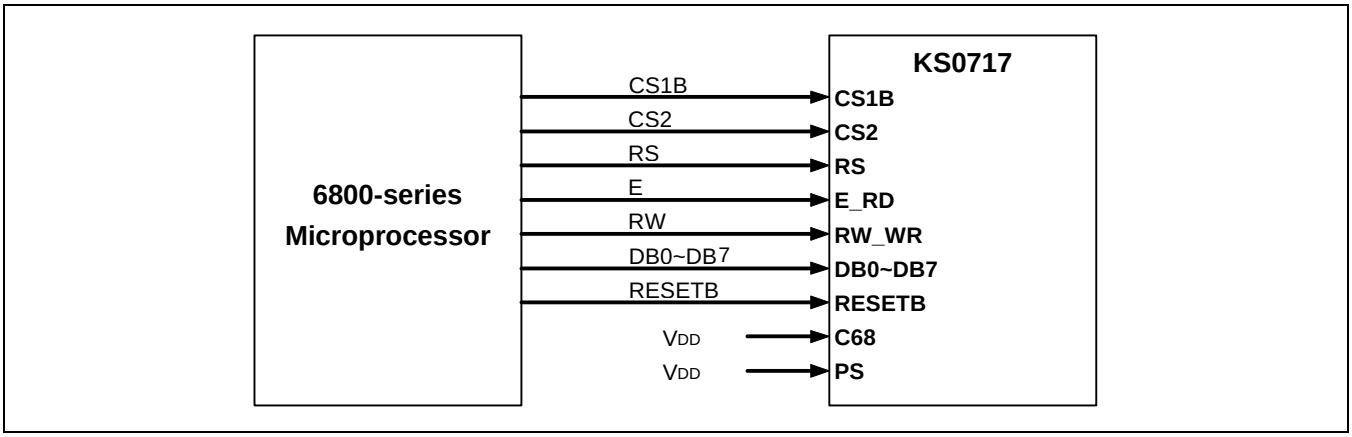


Figure 26. In Case of Interfacing with the 6800_Series (PS = “H”, C68 = “H”)

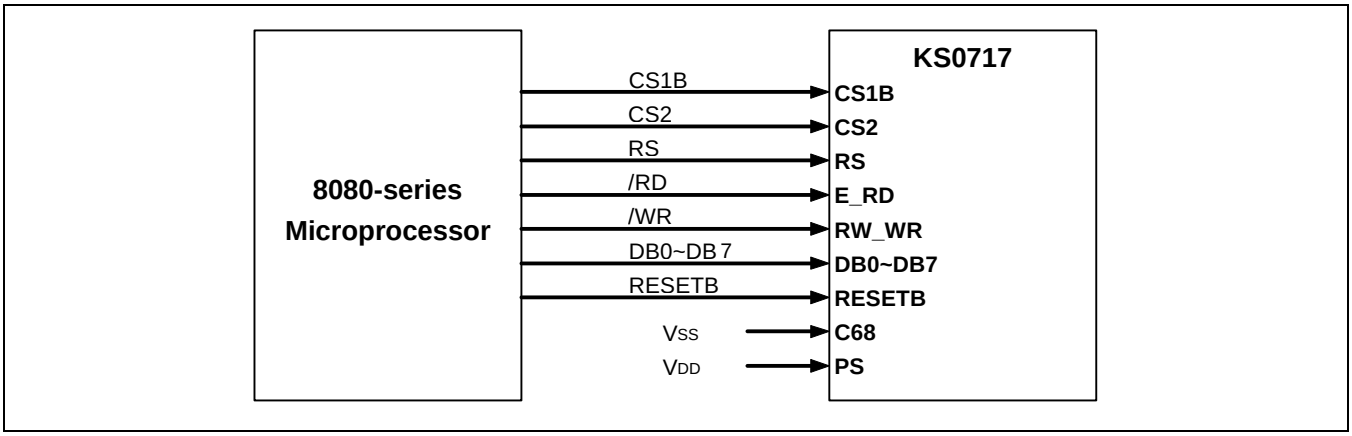


Figure 27. In Case of Interfacing with the 8080-Series (PS = “H”, C68 = “L”)

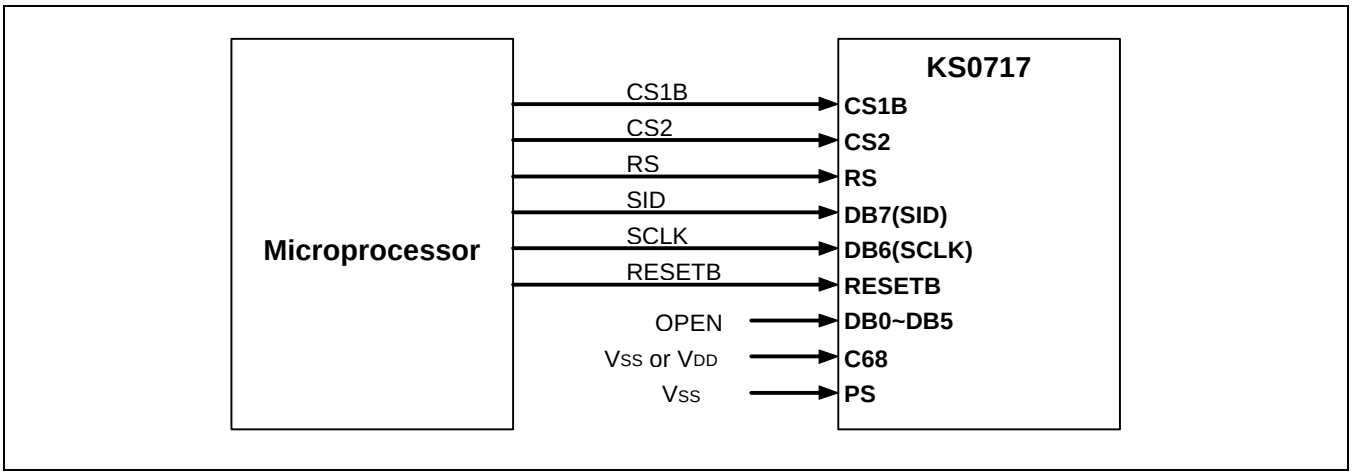
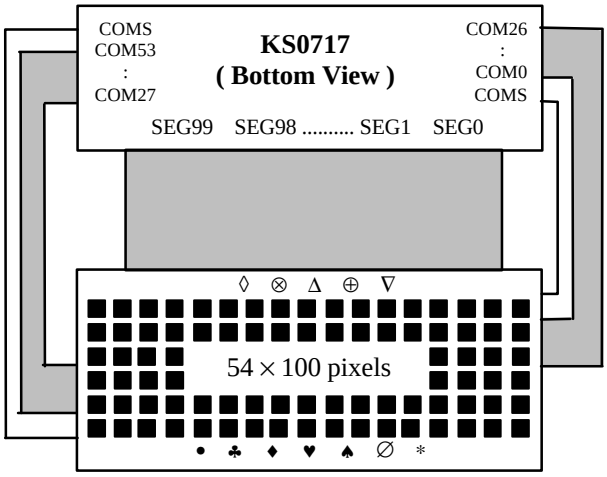


Figure 28. In Case of Serial Interface (PS = “L”, C68 = “H/L”)

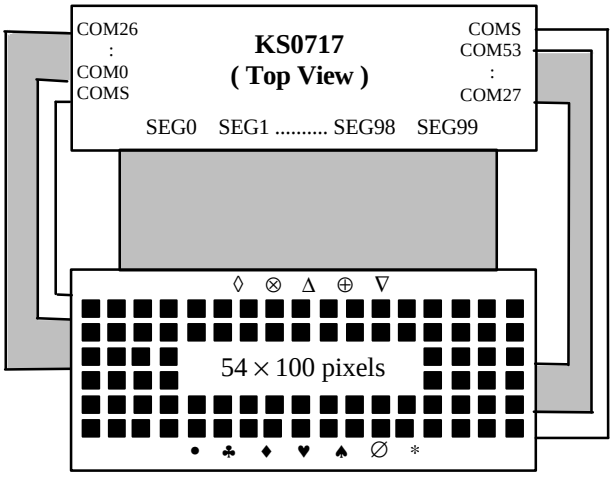
CONNECTIONS BETWEEN KS0717 AND LCD PANEL

Single-Chip Structure (1/55 Duty Configurations)

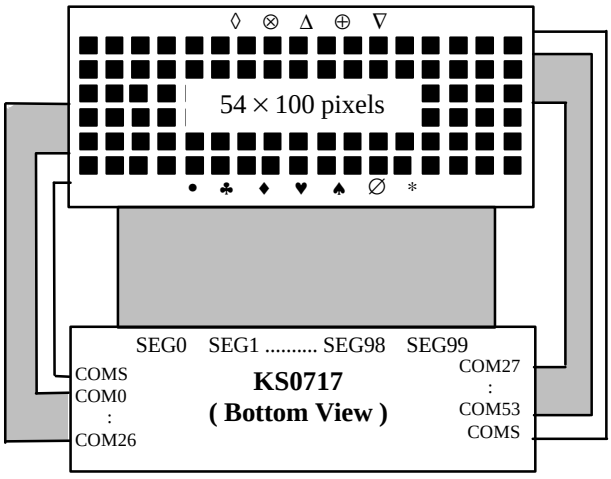
¨ **SHL = 0, ADC = 0**



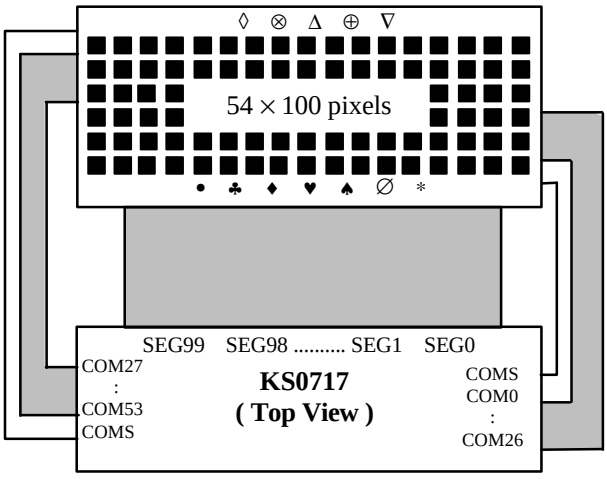
¨ **SHL = 0, ADC = 1**



¨ **SHL = 1, ADC = 0**

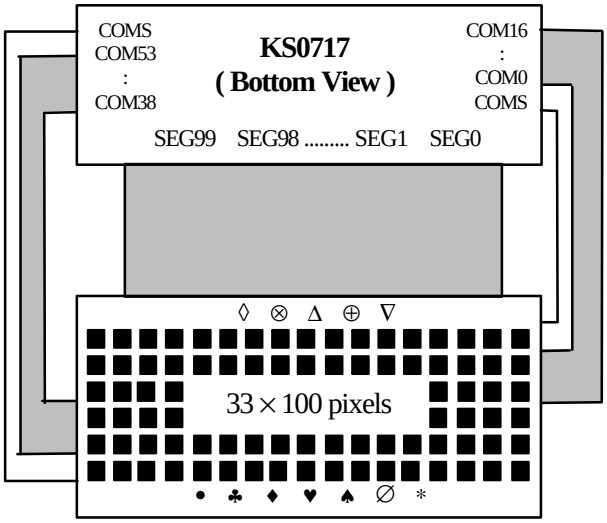


¨ **SHL = 1, ADC = 1**

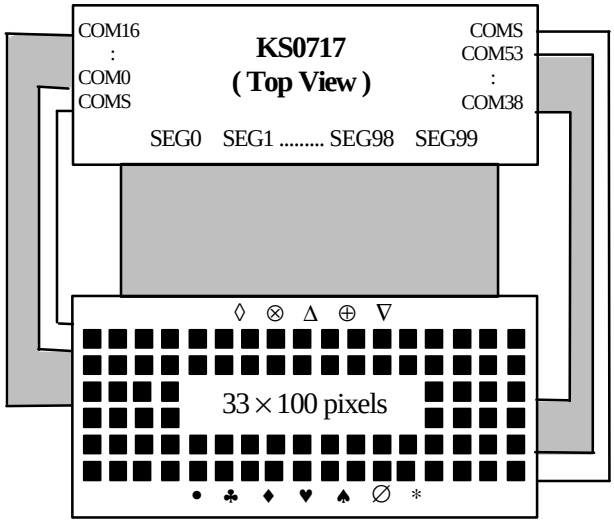


Single-Chip Structure (1/34 Duty Configurations)

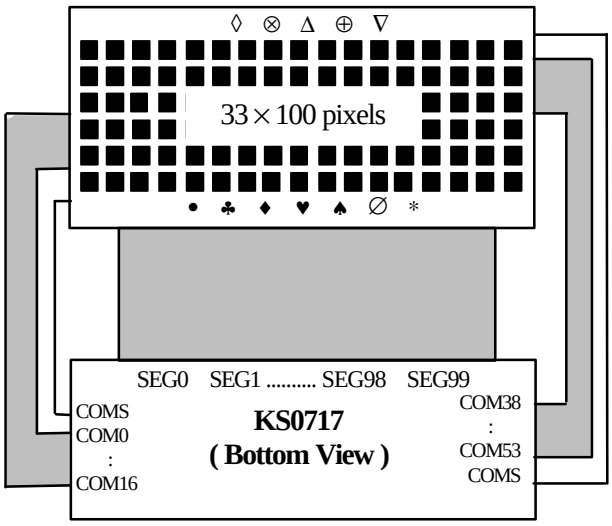
¨ **SHL = 0, ADC = 0**



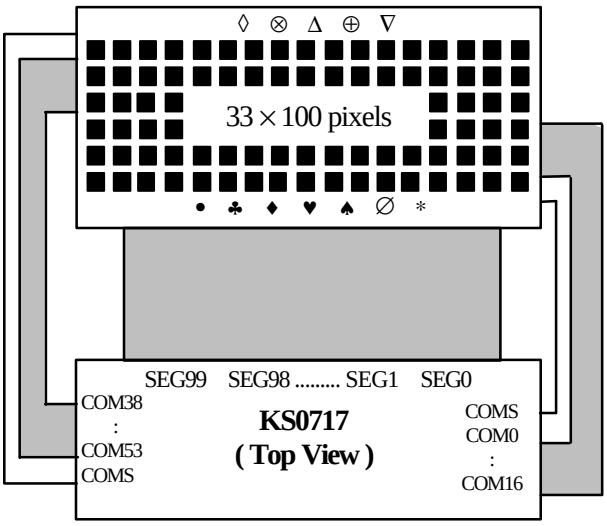
¨ **SHL = 0, ADC = 1**



¨ **SHL = 1, ADC = 0**

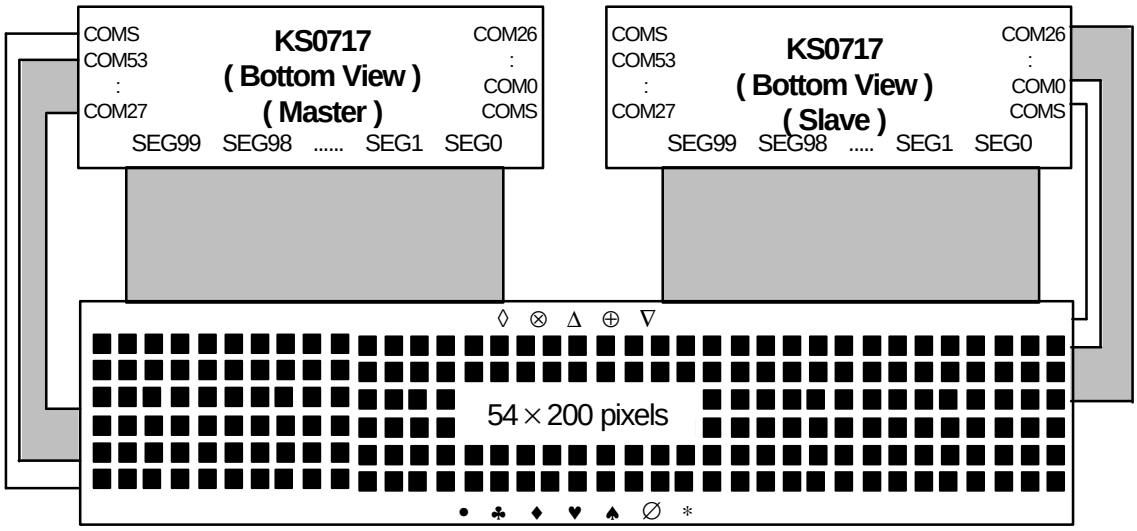


¨ **SHL = 1, ADC = 1**



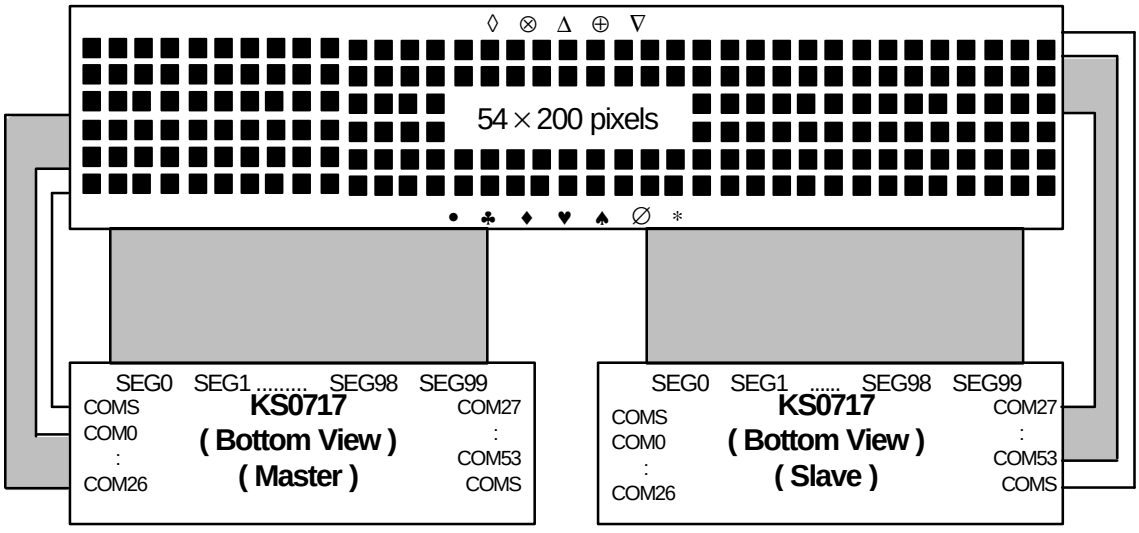
Multi-Chip Structure

¨ **SHL = 0, ADC = 1**



- Connect the following Pins of two chips each other :
  - Clock Pins : CL, M, DISP
  - LCD Power : V0, V1, V2, V3, V4

¨ **SHL = 1, ADC = 0**



KS0717 TCP PIN LAYOUT (SAMPLE)