INTRODUCTION

The KS0713 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It contains 65 common and 132 segment driver circuits. This chip is connected directly to a microprocessor, accepts 8-bit serial or parallel display data, and stores an on-chip display data RAM of 65 × 132 bits. It provides a highly-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. Furthermore, the chip performs display data RAM read/write operation with no external operating clock to minimize power consumption. Because KS0713 contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

- **Driver output circuits**
  - — 65 common outputs / 132 segment outputs
- **On-chip display data RAM**
  - — Capacity: 65 × 132 = 8,580 bits
- **Multi-chip operation**
  - — Master, Slave available
- **Applicable duty-ratios**

Duty Ratio	Applicable LCD Bias	Maximum Display Area
1/65	1/7 or 1/9	65 × 132
1/49	1/6 or 1/8	49 × 132
1/33	1/5 or 1/6	33 × 132

- **Microprocessor Interface**
  - — 8-bit parallel bidirectional interface with 6800-series or 8080-series
  - — Serial interface (only write operation) available
- **Function Set**
  - — Various Instruction Set: Power control, ADC, SHL, Entire Display ON/OFF, Sleep mode, Standby mode, ... etc.
  - — H/W, S/W Reset capable
- **Built-in Analog Circuit**
  - — Built-in Oscillator Circuit
  - — Voltage Converter (×2 / ×3 / ×4 / ×5)
  - — Voltage Regulator (Temperature coefficient: –0.05%/°C, –0.2%/°C)
  - — Voltage Follower
  - — Electronic contrast control functions (64 steps)

- **Operating voltage range**
  - — Supply voltage (V_{DD}): 2.4 to 5.5 V
  - — LCD driving voltage ($V_{LCD} = V0 - V_{SS}$): 4.0 to 15.0 V
- **Low power consumption**
  - — 80 µA Typ. (V_{DD} = 3V, × 4 boosting, V0 = 11V, Internal power supply ON)
  - — 10 µA Max. (Standby Mode)
- **Package Type**
  - — Slim chip for COG, and TCP available.

BLOCK DIAGRAM

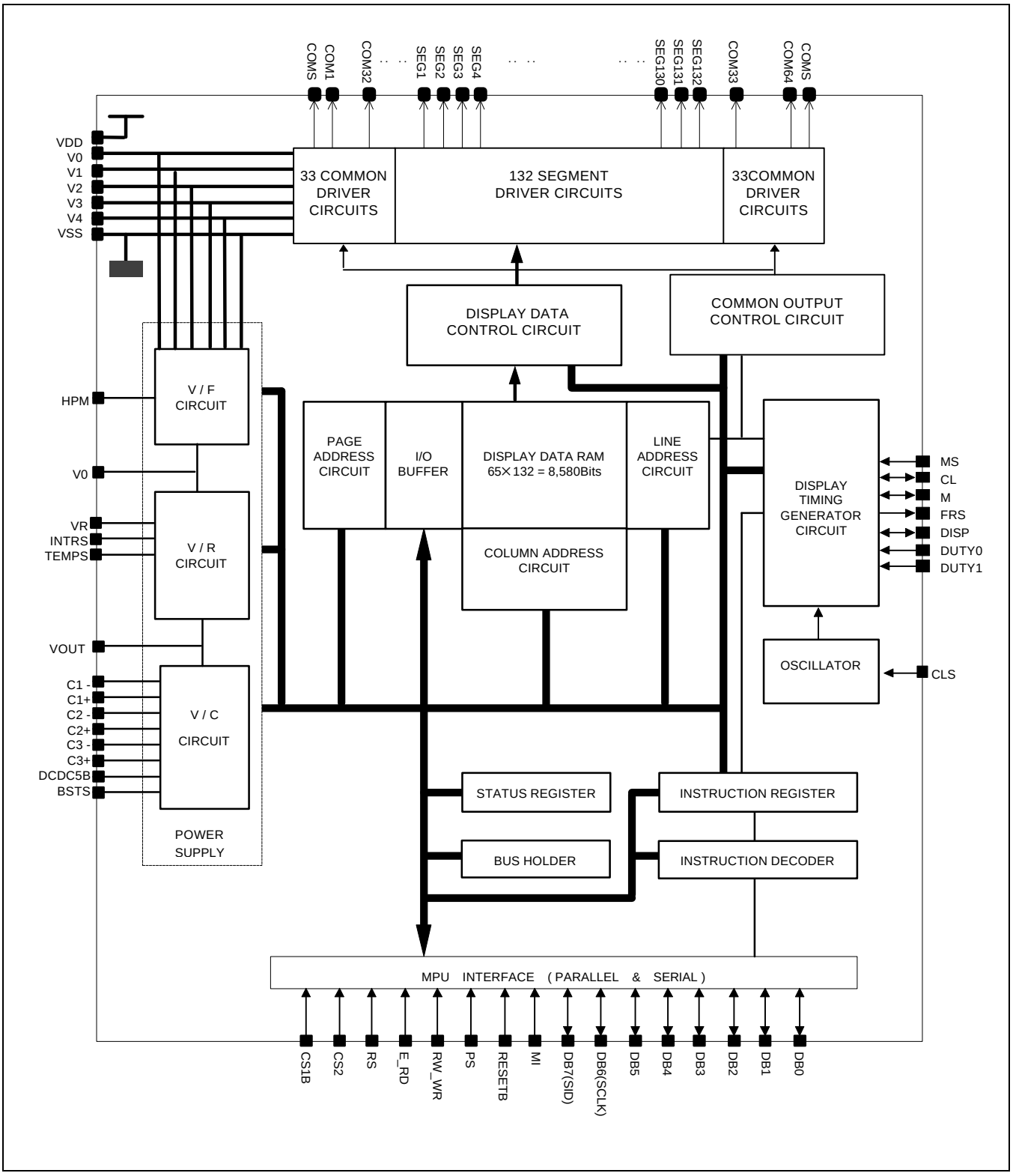


Figure 1. Block Diagram

PAD CONFIGURATION

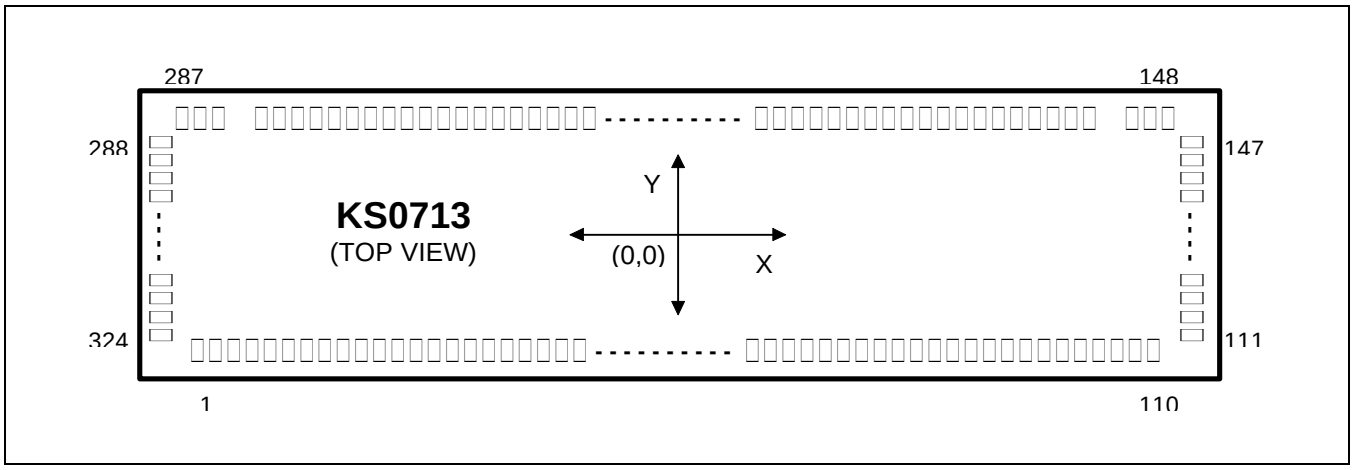


Figure 2. Pad Configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	–	10860	2920	µm
Pad pitch	1 – 110	90		
	111 – 324	70		
Bumped pad size	1 – 110	56	114	
	111 – 147	108	50	
	148 – 287	50	108	
	288 – 324	108	50	
Bumped pad height	1 – 324	17 (TYP)		

PAD CENTER COORDINATES

Table 1. Pad Location

[unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	DUMMY	-4905	-1316	51	VDD	-405	-1316	101	BSTS	4095	-1316
2	DUMMY	-4815	-1316	52	VDD	-315	-1316	102	DCDC5B	4185	-1316
3	FRS	-4725	-1316	53	VDD	-225	-1316	103	VDD	4275	-1316
4	M	-4635	-1316	54	VDD	-135	-1316	104	HPM	4365	-1316
5	CL	-4545	-1316	55	VDD	-45	-1316	105	INTRS	4455	-1316
6	DISP	-4455	-1316	56	VDD	45	-1316	106	VSS	4545	-1316
7	VSS	-4365	-1316	57	VOUT	135	-1316	107	TEMPS	4635	-1316
8	CS1B	-4275	-1316	58	VOUT	225	-1316	108	VDD	4725	-1316
9	CS2	-4185	-1316	59	VOUT	315	-1316	109	DUMMY	4815	-1316
10	VDD	-4095	-1316	60	VOUT	405	-1316	110	DUMMY	4905	-1316
11	RESETB	-4005	-1316	61	C3+	495	-1316	111	DUMMY	5271	-1260
12	RS	-3915	-1316	62	C3+	585	-1316	112	DUMMY	5271	-1190
13	VSS	-3825	-1316	63	C3+	675	-1316	113	COMS	5271	-1120
14	RW_WR	-3735	-1316	64	C3+	765	-1316	114	COM1	5271	-1050
15	E_RD	-3645	-1316	65	C3-	855	-1316	115	COM2	5271	-980
16	VDD	-3555	-1316	66	C3-	945	-1316	116	COM3	5271	-910
17	DB0	-3465	-1316	67	C3-	1035	-1316	117	COM4	5271	-840
18	DB1	-3375	-1316	68	C3-	1125	-1316	118	COM5	5271	-770
19	DB2	-3285	-1316	69	C1+	1215	-1316	119	COM6	5271	-700
20	DB3	-3195	-1316	70	C1+	1305	-1316	120	COM7	5271	-630
21	DB4	-3105	-1316	71	C1+	1395	-1316	121	COM8	5271	-560
22	DB5	-3015	-1316	72	C1+	1485	-1316	122	COM9	5271	-490
23	DB6	-2925	-1316	73	C1-	1575	-1316	123	COM10	5271	-420
24	DB7	-2835	-1316	74	C1-	1665	-1316	124	COM11	5271	-350
25	VSS	-2745	-1316	75	C1-	1755	-1316	125	COM12	5271	-280
26	VDD	-2655	-1316	76	C1-	1845	-1316	126	COM13	5271	-210
27	VDD	-2565	-1316	77	C2+	1935	-1316	127	COM14	5271	-140
28	VDD	-2475	-1316	78	C2+	2025	-1316	128	COM15	5271	-70
29	DUTY0	-2385	-1316	79	C2+	2115	-1316	129	COM16	5271	0
30	DUTY1	-2295	-1316	80	C2+	2205	-1316	130	COM17	5271	70
31	VSS	-2205	-1316	81	C2-	2295	-1316	131	COM18	5271	140
32	MS	-2115	-1316	82	C2-	2385	-1316	132	COM19	5271	210
33	CLS	-2025	-1316	83	C2-	2475	-1316	133	COM20	5271	280
34	VDD	-1935	-1316	84	C2-	2565	-1316	134	COM21	5271	350
35	MI	-1845	-1316	85	VSS	2655	-1316	135	COM22	5271	420
36	PS	-1755	-1316	86	VSS	2745	-1316	136	COM23	5271	490
37	VSS	-1665	-1316	87	VR	2835	-1316	137	COM24	5271	560
38	VSS	-1575	-1316	88	VR	2925	-1316	138	COM25	5271	630
39	VSS	-1485	-1316	89	V0	3015	-1316	139	COM26	5271	700
40	VSS	-1395	-1316	90	V0	3105	-1316	140	COM27	5271	770
41	VSS	-1305	-1316	91	V1	3195	-1316	141	COM28	5271	840
42	VSS	-1215	-1316	92	V1	3285	-1316	142	COM29	5271	910
43	VSS	-1125	-1316	93	V2	3375	-1316	143	COM30	5271	980
44	VSS	-1035	-1316	94	V2	3465	-1316	144	COM31	5271	1050
45	VSS	-945	-1316	95	V3	3555	-1316	145	COM32	5271	1120
46	VSS	-855	-1316	96	V3	3645	-1316	146	DUMMY	5271	1190
47	VDD	-765	-1316	97	V4	3735	-1316	147	DUMMY	5271	1260
48	VDD	-675	-1316	98	V4	3825	-1316	148	DUMMY	4865	1321
49	VDD	-585	-1316	99	VSS	3915	-1316	149	DUMMY	4795	1321
50	VDD	-495	-1316	100	VSS	4005	-1316	150	DUMMY	4725	1321

Table 1. Pad Location (Continued)

[unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
151	DUMMY	4655	1321	201	SEG50	1155	1321	251	SEG100	-2345	1321
152	SEG1	4585	1321	202	SEG51	1085	1321	252	SEG101	-2415	1321
153	SEG2	4515	1321	203	SEG52	1015	1321	253	SEG102	-2485	1321
154	SEG3	4445	1321	204	SEG53	945	1321	254	SEG103	-2555	1321
155	SEG4	4375	1321	205	SEG54	875	1321	255	SEG104	-2625	1321
156	SEG5	4305	1321	206	SEG55	805	1321	256	SEG105	-2695	1321
157	SEG6	4235	1321	207	SEG56	735	1321	257	SEG106	-2765	1321
158	SEG7	4165	1321	208	SEG57	665	1321	258	SEG107	-2835	1321
159	SEG8	4095	1321	209	SEG58	595	1321	259	SEG108	-2905	1321
160	SEG9	4025	1321	210	SEG59	525	1321	260	SEG109	-2975	1321
161	SEG10	3955	1321	211	SEG60	455	1321	261	SEG110	-3045	1321
162	SEG11	3885	1321	212	SEG61	385	1321	262	SEG111	-3115	1321
163	SEG12	3815	1321	213	SEG62	315	1321	263	SEG112	-3185	1321
164	SEG13	3745	1321	214	SEG63	245	1321	264	SEG113	-3255	1321
165	SEG14	3675	1321	215	SEG64	175	1321	265	SEG114	-3325	1321
166	SEG15	3605	1321	216	SEG65	105	1321	266	SEG115	-3395	1321
167	SEG16	3535	1321	217	SEG66	35	1321	267	SEG116	-3465	1321
168	SEG17	3465	1321	218	SEG67	-35	1321	268	SEG117	-3535	1321
169	SEG18	3395	1321	219	SEG68	-105	1321	269	SEG118	-3605	1321
170	SEG19	3325	1321	220	SEG69	-175	1321	270	SEG119	-3675	1321
171	SEG20	3255	1321	221	SEG70	-245	1321	271	SEG120	-3745	1321
172	SEG21	3185	1321	222	SEG71	-315	1321	272	SEG121	-3815	1321
173	SEG22	3115	1321	223	SEG72	-385	1321	273	SEG122	-3885	1321
174	SEG23	3045	1321	224	SEG73	-455	1321	274	SEG123	-3955	1321
175	SEG24	2975	1321	225	SEG74	-525	1321	275	SEG124	-4025	1321
176	SEG25	2905	1321	226	SEG75	-595	1321	276	SEG125	-4095	1321
177	SEG26	2835	1321	227	SEG76	-665	1321	277	SEG126	-4165	1321
178	SEG27	2765	1321	228	SEG77	-735	1321	278	SEG127	-4235	1321
179	SEG28	2695	1321	229	SEG78	-805	1321	279	SEG128	-4305	1321
180	SEG29	2625	1321	230	SEG79	-875	1321	280	SEG129	-4375	1321
181	SEG30	2555	1321	231	SEG80	-945	1321	281	SEG130	-4445	1321
182	SEG31	2485	1321	232	SEG81	-1015	1321	282	SEG131	-4515	1321
183	SEG32	2415	1321	233	SEG82	-1085	1321	283	SEG132	-4585	1321
184	SEG33	2345	1321	234	SEG83	-1155	1321	284	DUMMY	-4655	1321
185	SEG34	2275	1321	235	SEG84	-1225	1321	285	DUMMY	-4725	1321
186	SEG35	2205	1321	236	SEG85	-1295	1321	286	DUMMY	-4795	1321
187	SEG36	2135	1321	237	SEG86	-1365	1321	287	DUMMY	-4865	1321
188	SEG37	2065	1321	238	SEG87	-1435	1321	288	DUMMY	-5271	1260
189	SEG38	1995	1321	239	SEG88	-1505	1321	289	DUMMY	-5271	1190
190	SEG39	1925	1321	240	SEG89	-1575	1321	290	COMS	-5271	1120
191	SEG40	1855	1321	241	SEG90	-1645	1321	291	COM64	-5271	1050
192	SEG41	1785	1321	242	SEG91	-1715	1321	292	COM63	-5271	980
193	SEG42	1715	1321	243	SEG92	-1785	1321	293	COM62	-5271	910
194	SEG43	1645	1321	244	SEG93	-1855	1321	294	COM61	-5271	840
195	SEG44	1575	1321	245	SEG94	-1925	1321	295	COM60	-5271	770
196	SEG45	1505	1321	246	SEG95	-1995	1321	296	COM59	-5271	700
197	SEG46	1435	1321	247	SEG96	-2065	1321	297	COM58	-5271	630
198	SEG47	1365	1321	248	SEG97	-2135	1321	298	COM57	-5271	560
199	SEG48	1295	1321	249	SEG98	-2205	1321	299	COM56	-5271	490
200	SEG49	1225	1321	250	SEG99	-2275	1321	300	COM55	-5271	420

Table 1. Pad Location (Continued)

[unit: μm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
301	COM54	-5271	350								
302	COM53	-5271	280								
303	COM52	-5271	210								
304	COM51	-5271	140								
305	COM50	-5271	70								
306	COM49	-5271	0								
307	COM48	-5271	-70								
308	COM47	-5271	-140								
309	COM46	-5271	-210								
310	COM45	-5271	-280								
311	COM44	-5271	-350								
312	COM43	-5271	-420								
313	COM42	-5271	-490								
314	COM41	-5271	-560								
315	COM40	-5271	-630								
316	COM39	-5271	-700								
317	COM38	-5271	-770								
318	COM37	-5271	-840								
319	COM36	-5271	-910								
320	COM35	-5271	-980								
321	COM34	-5271	-1050								
322	COM33	-5271	-1120								
323	DUMMY	-5271	-1190								
324	DUMMY	-5271	-1260								

PIN DESCRIPTION

Table 2. Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Power Supply</td></tr>
<tr><td>VDD</td><td rowspan="2">Power</td><td>Power supply
Connect to MPU power supply pin.</td></tr>
<tr><td>VSS</td><td>0 V (GND)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>The voltage determined by the LCD pixel is impedance-converted for application by an operational amplifier. Voltages have the following relationship:
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the on-chip power circuit is active, these voltages are generated according to the state of LCD bias, as shown in the table below.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/9 Bias</td><td>(8/9) × V0</td><td>(7/9) × V0</td><td>(2/9) × V0</td><td>(1/9) × V0</td></tr>
<tr><td>1/8 Bias</td><td>(7/8) × V0</td><td>(6/8) × V0</td><td>(2/8) × V0</td><td>(1/8) × V0</td></tr>
<tr><td>1/7 Bias</td><td>(6/7) × V0</td><td>(5/7) × V0</td><td>(2/7) × V0</td><td>(1/7) × V0</td></tr>
<tr><td>1/6 Bias</td><td>(5/6) × V0</td><td>(4/6) × V0</td><td>(2/6) × V0</td><td>(1/6) × V0</td></tr>
<tr><td>1/5 Bias</td><td>(4/5) × V0</td><td>(3/5) × V0</td><td>(2/5) × V0</td><td>(1/5) × V0</td></tr>
</table></td></tr>
<tr><td colspan="3">LCD Driver Supply</td></tr>
<tr><td>C1+</td><td rowspan="6">O</td><td>Capacitor1+ connect for the internal voltage converter</td></tr>
<tr><td>C1–</td><td>Capacitor1– connect for the internal voltage converter</td></tr>
<tr><td>C2+</td><td>Capacitor2+ connect for the internal voltage converter</td></tr>
<tr><td>C2–</td><td>Capacitor2– connect for the internal voltage converter</td></tr>
<tr><td>C3+</td><td>Capacitor3+ connect for the internal voltage converter</td></tr>
<tr><td>C3–</td><td>Capacitor3– connect for the internal voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>Voltage converter output</td></tr>
<tr><td>DCDC5B</td><td>I</td><td>5 times boosting circuit enable input pin. When this pin is low in 4 times boosting circuit, the 5 times boosted voltage appears at VOUT.</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjustment pin, valid only when using external resistors (INTRS = “L”)</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">System Control</td></tr>
<tr><td>MS</td><td>I</td><td>Master/slave mode select input. Master makes some signals for display, and slave receives them. This is for display synchronization.
MS = “H”: Master mode
MS = “L”: Slave mode
<table>
<tr><th>MS</th><th>CLS</th><th>OSC Circuit</th><th>Power Supply</th><th>CL</th><th>M</th><th>FRS</th><th>DISP</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disable</td><td>Enable</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>–</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin.
CLS = “H”: Enable
CLS = “L”: Disable (External display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output. When KS0713 is used in master/slave mode (multi-chip), the CL pins must be connected to each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input/output. When KS0713 is used in master/slave mode(multi-chip), the M pins must be connected to each other.
MS = “H”: Output
MS = “L”: Input.</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver output. This pin is used together with the M pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input/output. When KS0713 is used in master/slave mode (multi-chip), the DISP pins must be connected to each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal Resistor Select.
This pin selects the resistors for adjusting V0 voltage level and is available only in master mode.
INTRS = “H”: using built-in resistors,
INTRS = “L”: not using built-in resistors. V0 voltage is controlled by VR pin and external resistive divider.</td></tr>
<tr><td>HPM</td><td>I</td><td>Power control pin of the power supply circuit for LCD driver.
HPM = “H”: High power mode
HPM = “L”: Normal mode
This pin is available only in master mode.</td></tr>
<tr><td>TEMPS</td><td>I</td><td>Selects temperature coefficient of the reference voltage
TEMPS = “L”: –0.05%/°C
TEMPS = “H”: –0.2%/°C</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>BSTS</td><td>I</td><td>Selects input voltages of the built-in Voltage converter
<table>
<tr><th>BSTS</th><th>Voltage Converter Input Voltage</th><th>Remarks</th></tr>
<tr><td rowspan="2">L</td><td>4 V</td><td>V_{DD} > 4V</td></tr>
<tr><td>V_{DD}</td><td>$V_{DD} \leq$ 4V</td></tr>
<tr><td>H</td><td>V_{DD}</td><td>2.4 $\leq V_{DD} \leq$ 5.5V</td></tr>
</table></td></tr>
<tr><td>DUTY1
DUTY0</td><td>I</td><td>The LCD driver duty ratio depends on the following table.
<table>
<tr><th>DUTY1</th><th>DUTY0</th><th>DUTY Ratio</th></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L/H</td><td>1/65</td></tr>
</table></td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">MPU Interface</td></tr>
<tr><td>RESETB</td><td>I</td><td>Hardware reset input.
Initialization is performed by edge sensing (rising or falling) of the RESET signal.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / serial data select input.
<table>
<tr><th>PS</th><th>Operating Mode</th><th>Chip Select</th><th>Data / Instruction</th><th>Data I/O</th><th>Read / Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB[7:0]</td><td>E_RD, RW_WR</td><td>–</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>DB7 (SID)</td><td>Write only</td><td>DB6 (SCLK)</td></tr>
</table>
Note: In serial mode, it is impossible to read data from the on-chip RAM.
DB[5:0] is high impedance and E_RD and RW_WR must be fixed on high or low.</td></tr>
<tr><td>MI</td><td>I</td><td>Microprocessor Interface select input in parallel mode.
MI = “H”: 6800 series MPU interface
MI = “L”: 8080 series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip Select inputs.
Data input / output is enabled only when CS1B is low and CS2 is high. When chip select is non-active, DB[7:0] will be High Impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register Select input.
RS = “H”: the data on DB[7:0] is display data
RS = “L”: the data on DB[7:0] is control data</td></tr>
<tr><td>RW_WR</td><td>I</td><td>When interfacing to a 6800-series MPU, Read/Write is enabled at;
RW_WR = “H”: Read.
RW_WR = “L”: Write.
When interfacing to an 8080-series MPU, RW_WR is enabled at low.</td></tr>
<tr><td>E_RD</td><td>I</td><td>When interfacing to a 6800-series MPU: Active High.
This is used as an enable clock input pin of the 6800-series MPU.
When interfacing to an 8080-series MPU: Active Low.
This input connects the RD signal of the 8080-series MPU. While this signal is Low, KS0713 data bus output is enabled.</td></tr>
<tr><td>DB7 to DB0</td><td>I/O</td><td>8-bit bidirectional data bus. It is connected to the standard 8-bit microprocessor data bus.
When the serial interface selected (PS = “Low”);
DB7: Serial input data (SID)
DB6: Serial input clock (SCLK)
DB5 to DB0: High impedance.
When Chip select is not active, DB7 to DB0 will be high impedance.</td></tr>
</table>

Table 2. Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">LCD Driver Output</td></tr>
<tr><td>SEG1 to SEG132</td><td>O</td><td>LCD driver output for segment. The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">M</th><th colspan="2">SEGs Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power Save Mode</td><td colspan="2">Vss</td></tr>
</table></td></tr>
<tr><td>COM1 to COM64</td><td>O</td><td>LCD driver output for common. The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan Data</th><th>M</th><th>COMs Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>Vss</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>Vss</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common signal output for the icons. The output signals of two pins are the same. When not used, these pins should be left open. In multi-chip (master/slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

CHIP SELECT INPUT

There are CS1B and CS2 pins for chip selection. The KS0713 can interface with a microprocessor only when CS1B is low and CS2 is high. When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB7 to DB0 are set to high impedance. For the serial interface, the internal shift register and the counter are reset.

PARALLEL / SERIAL INTERFACE

The KS0713 has three types of interface with MPU: one serial and two parallel interface. This parallel or serial interface is determined by PS pin as shown in Table 3.

Table 3. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	MI	Interface Mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	–	Serial-mode

NOTE: "–" Don't care

Parallel Interface (PS = "H")

The 8-bit bidirectional data bus is used in parallel interface and the type of MPU is selected by MI as shown in Table 4. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in Table 5.

.

Table 4. Microprocessor Selection for Parallel Interface

MI	CS1B	CS2	RS	E_RD	RW_WR	DB7 to DB0	MPU Bus
H	CS1B	CS2	RS	E	RW	DB7 to DB0	6800-series
L	CS1B	CS2	RS	RD	WR	DB7 to DB0	8080-series

Table 5. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (RD)	RW_WR (WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (Instruction)

Serial interface (PS = “L”)

When KS0713 is active (CS1B = “L”, CS2 = “H”), serial data (DB7) and serial clock (DB6) inputs are enabled. When not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal[DB6] is easily affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

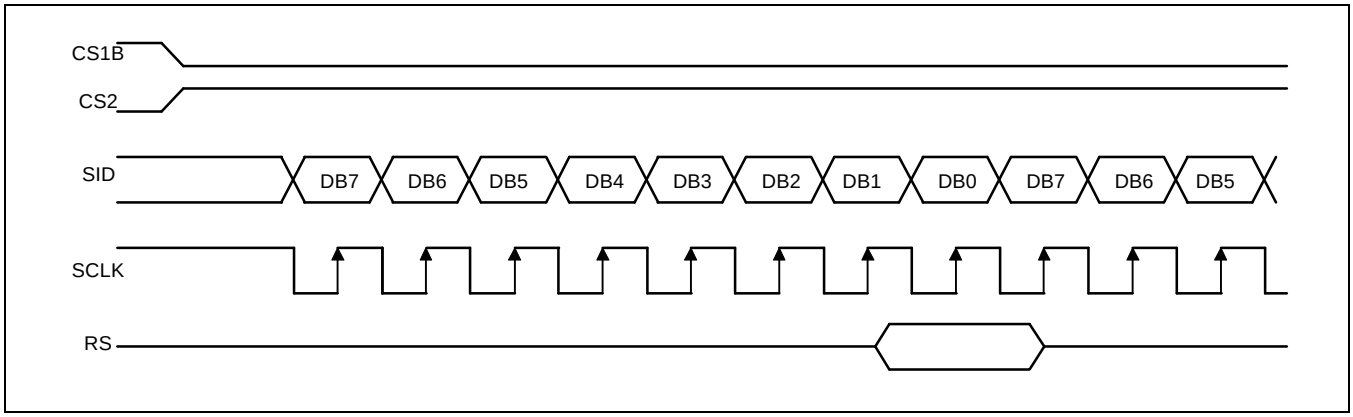


Figure 3. Serial Interface Timing

BUSY FLAG

The busy flag indicates whether the KS0713 is operating or not. When DB7 is HIGH in Read Status operation, this device is in busy status and will accept only Read Status instruction. If the cycle time is correct, the microprocessor does not need to check this flag before each instruction, which improves the microprocessor performance.

DATA TRANSFER

The KS0713 uses a bus holder and an internal data bus for data transfer with MPU. When writing data from the MPU to an on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Figure 2. When reading data from an on-chip RAM to MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and MPU reads this stored data from bus holder for the next data read cycle as shown in Figure 6.3. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the Read Display Data instruction right after the address sets, but can be output at the second read of data.

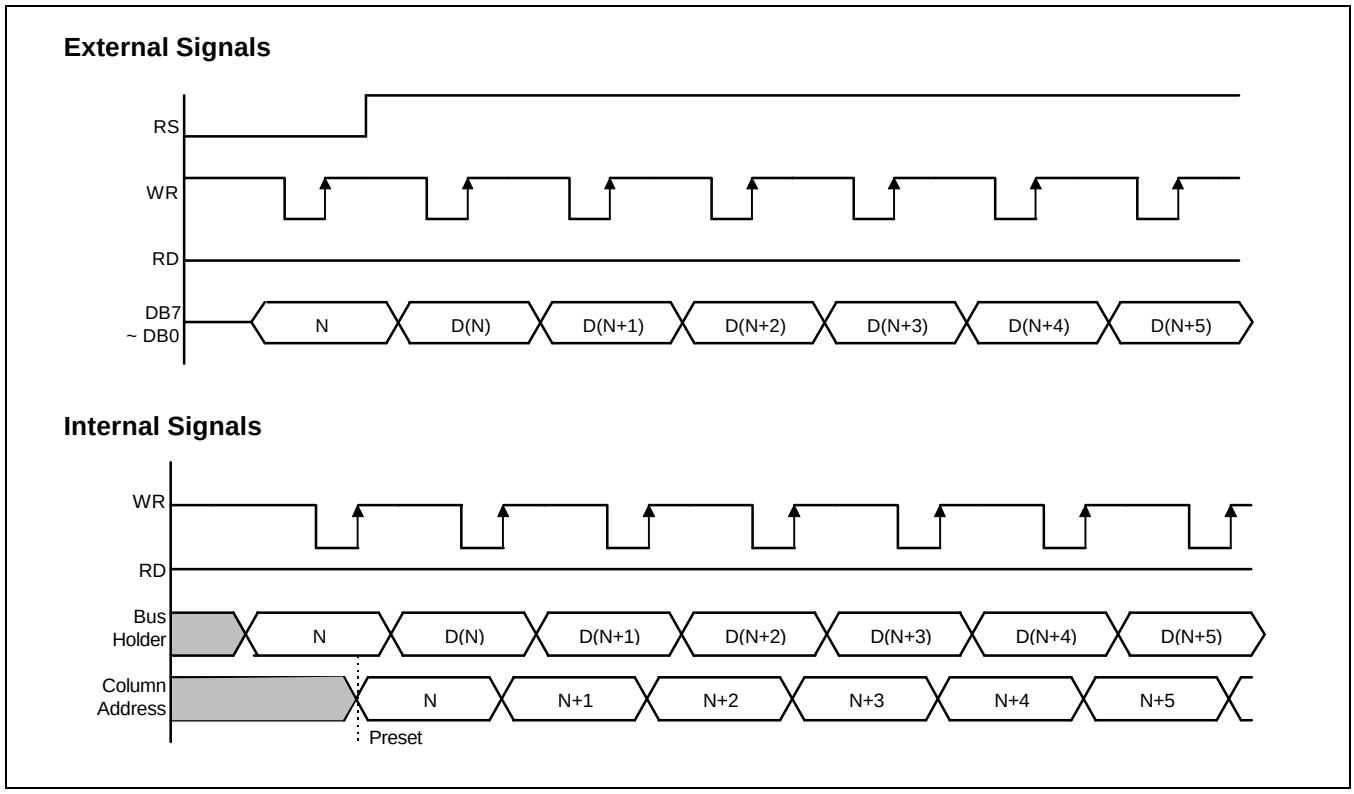


Figure 4. Write Timing

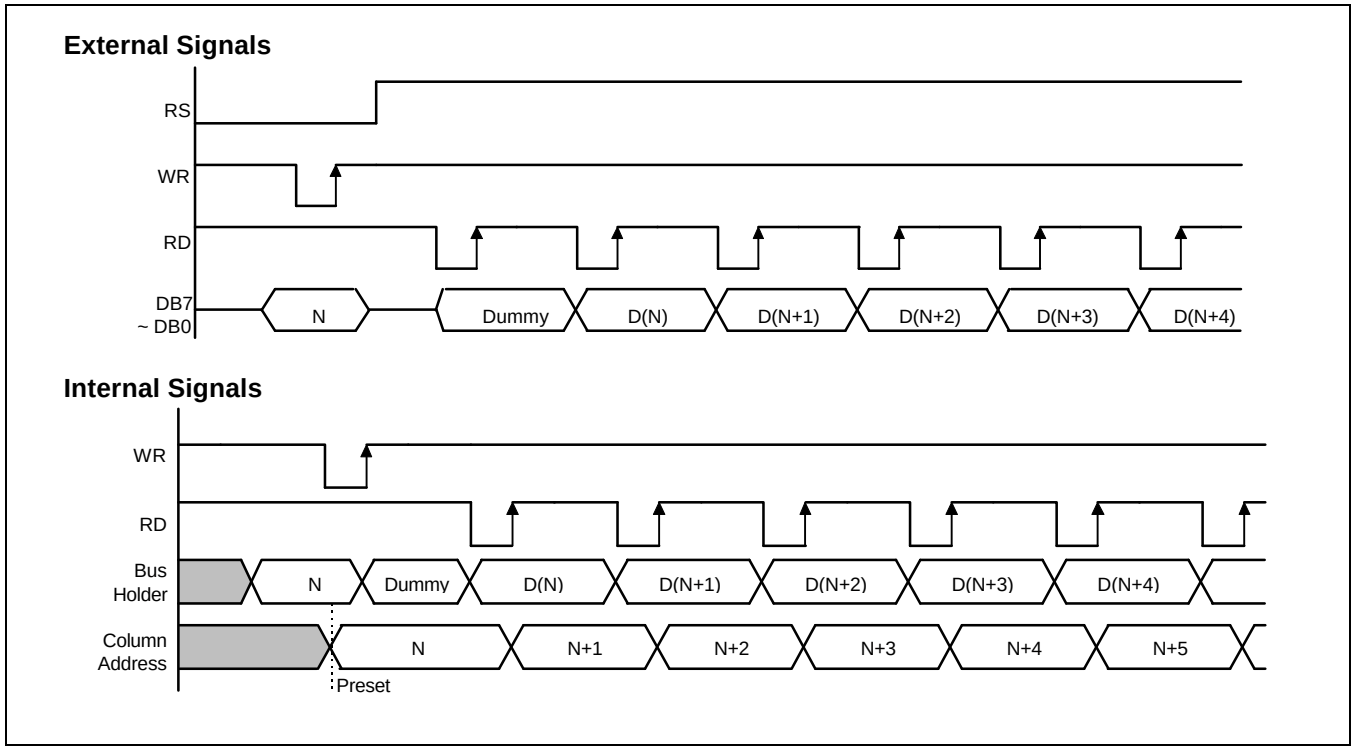


Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The display data RAM stores pixel data for the LCD. It is a 65-row ((8 page by 8-bit) + 1) by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the ninth page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in Figure 6.

The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is displayed without causing the LCD to flicker.

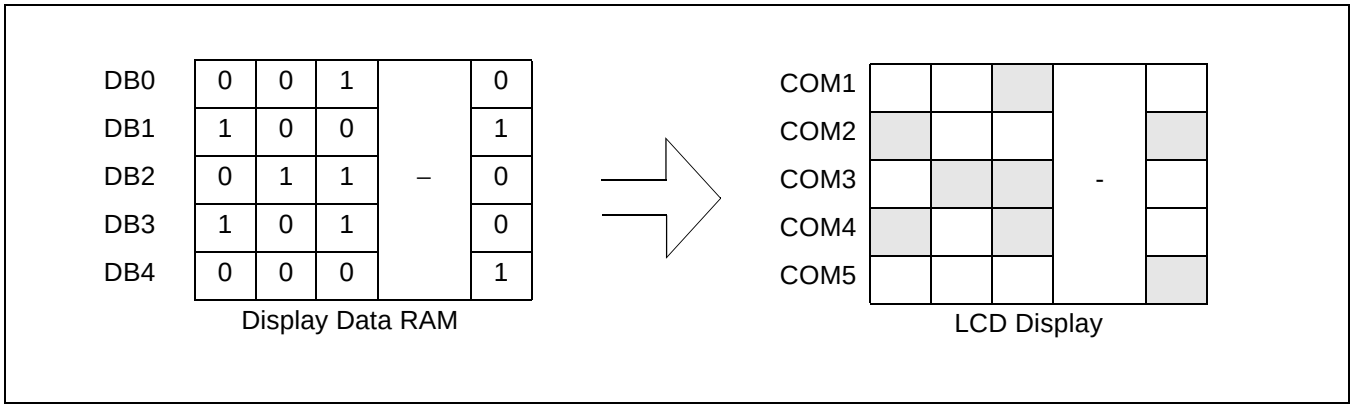


Figure 6. RAM-to-LCD Data Transfer

PAGE ADDRESS CIRCUIT

The function of this circuit is to provide a page address to the display data RAM shown in Table 7. It incorporates a 4-bit page address register changed only by the set page instruction. Page address 8 (DB3 is high, but DB2, DB1 and DB0 are low) is a special RAM area for icons, and only display data DB0 is valid. When page address is above 8, it is impossible to access the on-chip RAM.

LINE ADDRESS CIRCUIT

This circuit assigns DDRAM a line address corresponding to the first line (COM1) of the display. Therefore, by setting the line address repeatedly, it is possible to scroll the screen and switch the page without changing the contents of the on-chip RAM (refer to Table 7). It incorporates a 6-bit Line Address register which can only be changed by the Initial display line instruction and a 6-bit counter circuit. At the beginning of each LCD frame, the contents of a register are copied to the line counter which is increased by the CL signal, and generates the line address for transferring the 132-bit RAM data to the 100 display data latch circuit. However, display data of icons are not scrolled because the microprocessor cannot access the line address of icons.

COLUMN ADDRESS CIRCUIT

Column address circuit has a 8-bit preset counter that provides column address to the display data RAM (shown in Table 7). When Set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. Since this address is increased by 1 each time there is a Read or Write Data instruction, the microprocessor can access the display data continuously. However, the counter is not increased and it is locked at a non-existing address above 84H. It is unlocked if a column address is set again by Set Column Address MSB/LSB instruction. The column address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. Refer to the following Table 6.

Table 6. Segment Output Direction According to ADC

SEG Output	SEG 1	SEG 2	SEG 3	SEG 4	.....	SEG 129	SEG 130	SEG 131	SEG 132
Column address [Y7:Y0]	00H	01H	02H	03H	.....	80H	81H	82H	83H
Display data	1	0	1	0		1	1	0	0
LCD panel display (ADC = 0)	■		■		.....	■	■		
LCD panel display (ADC = 1)			■	■	.....		■		■

Table 7. Display Data RAM Addressing

Page Address P3,P2,P1,P0				Data	Column Address												Line Address (HEX)	Common Output (1/65)	Common Output (1/49)	Common Output (1/33)
0	0	0	0	DB0							Page0							00	COM37	COM37	–
				DB1														01	COM38	COM38	–
				DB2														02	COM39	COM39	–
				DB3														03	COM40	COM40	–
				DB4														04	COM41	COM41	–
				DB5														05	COM42	COM42	–
				DB6														06	COM43	COM43	–
				DB7														07	COM44	COM44	–
0	0	0	1	DB0							Page1							08	COM45	COM45	–
				DB1														09	COM46	COM46	–
				DB2														0A	COM47	COM47	–
				DB3														0B	COM48	COM48	–
				DB4														0C	COM49	–	–
				DB5														0D	COM50	–	–
				DB6														0E	COM51	–	–
				DB7														0F	COM52	–	–
0	0	1	0	DB0							Page2							10	COM53	–	–
				DB1														11	COM54	–	–
				DB2														12	COM55	–	–
				DB3														13	COM56	–	–
				DB4														14	COM57	–	–
				DB5														15	COM58	–	–
				DB6														16	COM59	–	–
				DB7														17	COM60	–	–
0	0	1	1	DB0							Page3							18	COM61	–	–
				DB1														18	COM62	–	–
				DB2														1A	COM63	–	–
				DB3														1B	COM64	–	–
				DB4														1C	COM1	COM1	COM1
				DB5														1D	COM2	COM2	COM2
				DB6														1E	COM3	COM3	COM3
				DB7														1F	COM4	COM4	COM4
0	1	0	0	DB0							Page4							20	COM5	COM5	COM5
				DB1														21	COM6	COM6	COM6
				DB2														22	COM7	COM7	COM7
				DB3														23	COM8	COM8	COM8
				DB4														24	COM9	COM9	COM9
				DB5														25	COM10	COM10	COM10
				DB6														26	COM11	COM11	COM11
				DB7														27	COM12	COM12	COM12
0	1	0	1	DB0							Page5							28	COM13	COM13	COM13
				DB1														29	COM14	COM14	COM14
				DB2														2A	COM15	COM15	COM15
				DB3														2B	COM16	COM16	COM16
				DB4														2C	COM17	COM17	COM17
				DB5														2D	COM18	COM18	COM18
				DB6														2E	COM19	COM19	COM19
				DB7														2F	COM20	COM20	COM20

Table 7. Display Data RAM Addressing (Continued)

Page Address P3,P2,P1,P0				Data	Column Address													Line Address (HEX)	Common Output (1/65)	Common Output (1/49)	Common Output (1/33)
0	1	1	0	DB0							Page6							30	COM21	COM21	COM21
				DB1														31	COM22	COM22	COM22
				DB2														32	COM23	COM23	COM23
				DB3														33	COM24	COM24	COM24
				DB4														34	COM25	COM25	COM25
				DB5														35	COM26	COM26	COM26
				DB6														36	COM27	COM27	COM27
				DB7														37	COM28	COM28	COM28
0	1	1	1	DB0							Page7							38	COM29	COM29	COM29
				DB1														39	COM30	COM30	COM30
				DB2														3A	COM31	COM31	COM31
				DB3														3B	COM32	COM32	COM32
				DB4														3C	COM33	COM33	–
				DB5														3D	COM34	COM34	–
				DB6														3E	COM35	COM35	–
				DB7														3F	COM36	COM36	–
1	0	0	0	DB0							Page8								COMS	COMS	COMS
Column Address [HEX]				ADC = 0	00	01	02	03	04	05	- - - - - -	7E	7F	80	81	82	83				
				ADC = 1	83	82	81	80	7F	7E	- - - - - -	05	04	03	02	01	00				
LCD Output					SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	- - - - - -	SEG127	SEF128	SEG129	SEG130	SEG131	SEG132				

NOTE: When the initial display line address is 1CH.

LCD DISPLAY CIRCUITS

OSCILLATOR

This is a completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

DISPLAY TIMING GENERATOR CIRCUIT

This circuit generates some signals to be used to display LCD. The display clock (CL) generated by the oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of the on-chip RAM is generated in synchronization with the display clock (CL). While the 132-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor.

The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Two-frame AC driver waveforms and internal timing signal are shown in Figure 7. When this KS0713 is used for a multi-chip, the slave chip must receive the M, CL, DISP signals from the master. Table 8 shows the M, CL, and DISP status.

Table 8. Master and Slave Signal Status

Operation Mode	Oscillator ON / OFF	M	CL	DISP
MASTER	ON (internal clock used)	Output	Output	Output
	OFF (external clock used)	Output	Input	Output
SLAVE	–	Input	Input	Input

DISPLAY DATA LATCH CIRCUIT

This latch circuit temporarily stores the output display data from the display data RAM to the LCD driver in each instruction period. This latch circuit is controlled by the Display ON/OFF, Reverse Display ON/OFF and Entire Display ON/OFF instructions, and the data in the display data RAM remains unchanged.

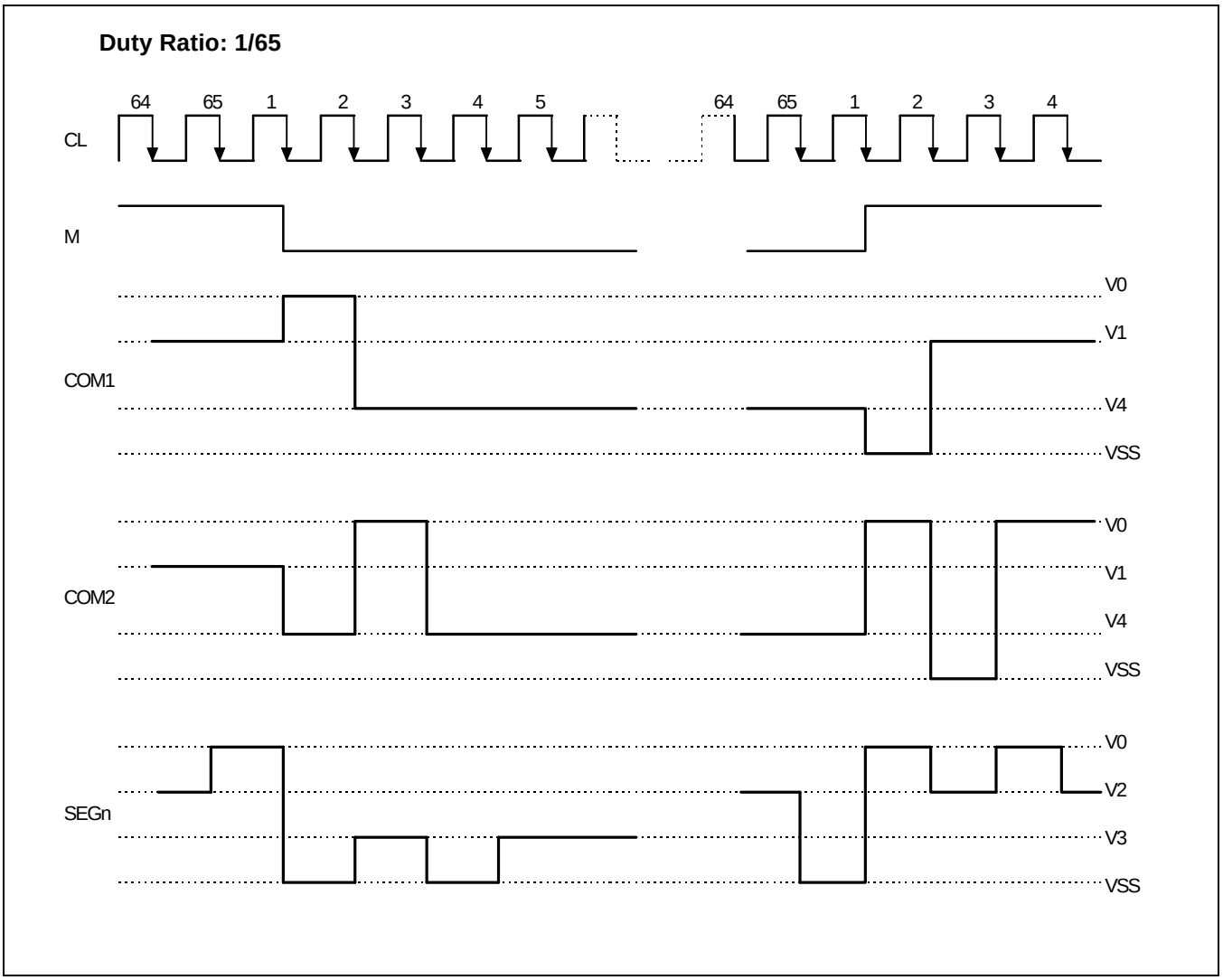


Figure 7. 2-Frame AC Driving Waveform

COMMON OUTPUT CONTROL CIRCUIT

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select instruction specifies the scanning direction of the common output pins.

Table 9. The Relationship Between Duty Ratio and Common Output

Duty	SHL	Common Output Pins					
		COM[1:16]	**COM[17:24]**	**COM[25:40]**	**COM[41:48]**	**COM[49:64]**	**COMS**
1/33	0	COM[1:16]	No connection	No connection	No connection	COM[17:32]	COMS
	1	COM[32:17]	No connection	No connection	No connection	COM[15:0]	COMS
1/49	0	COM[1:24]		No connection	COM[25:48]		COMS
	1	COM[48:25]		No connection	COM[24:1]		COMS
1/65	0	COM[1:64]					COMS
	1	COM[64:1]					COMS

LCD DRIVER CIRCUIT

This driver circuit is configured by a 66-channel common driver and a 132-channel segment driver. This LCD panel driver voltage depends on the combination of display data and M signal.

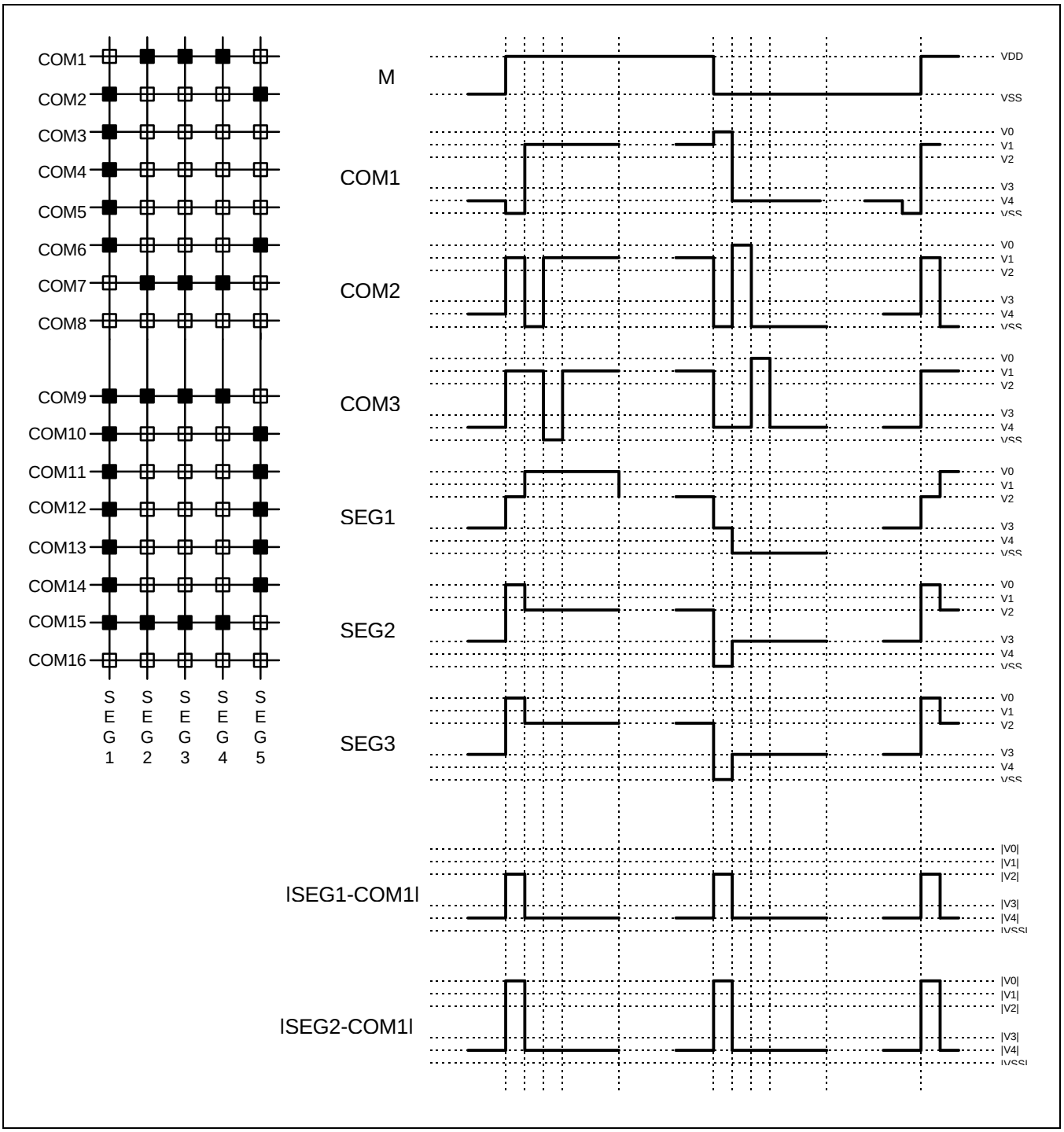


Figure 8. Segment and Common Timing

POWER SUPPLY CIRCUITS

The power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by Power Control instruction. For details, refers to “Instruction Description”. Table 10 shows the referenced combinations in using power supply circuits.

Table 10. Recommended Power Supply Combinations

User Setup	Power Control Register (VC VR VF)	V/C Circuits	V/R Circuits	V/F Circuits	VOUT Pin	V0 Pin	V1–V4 Pin
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External input	External input

VOLTAGE CONVERTER CIRCUITS

These circuits boost up the electric potential between V_{DD} and V_{SS} 2, 3, 4, or 5 times toward positive side, Boosted voltage is then output from the V_{OUT} pin.

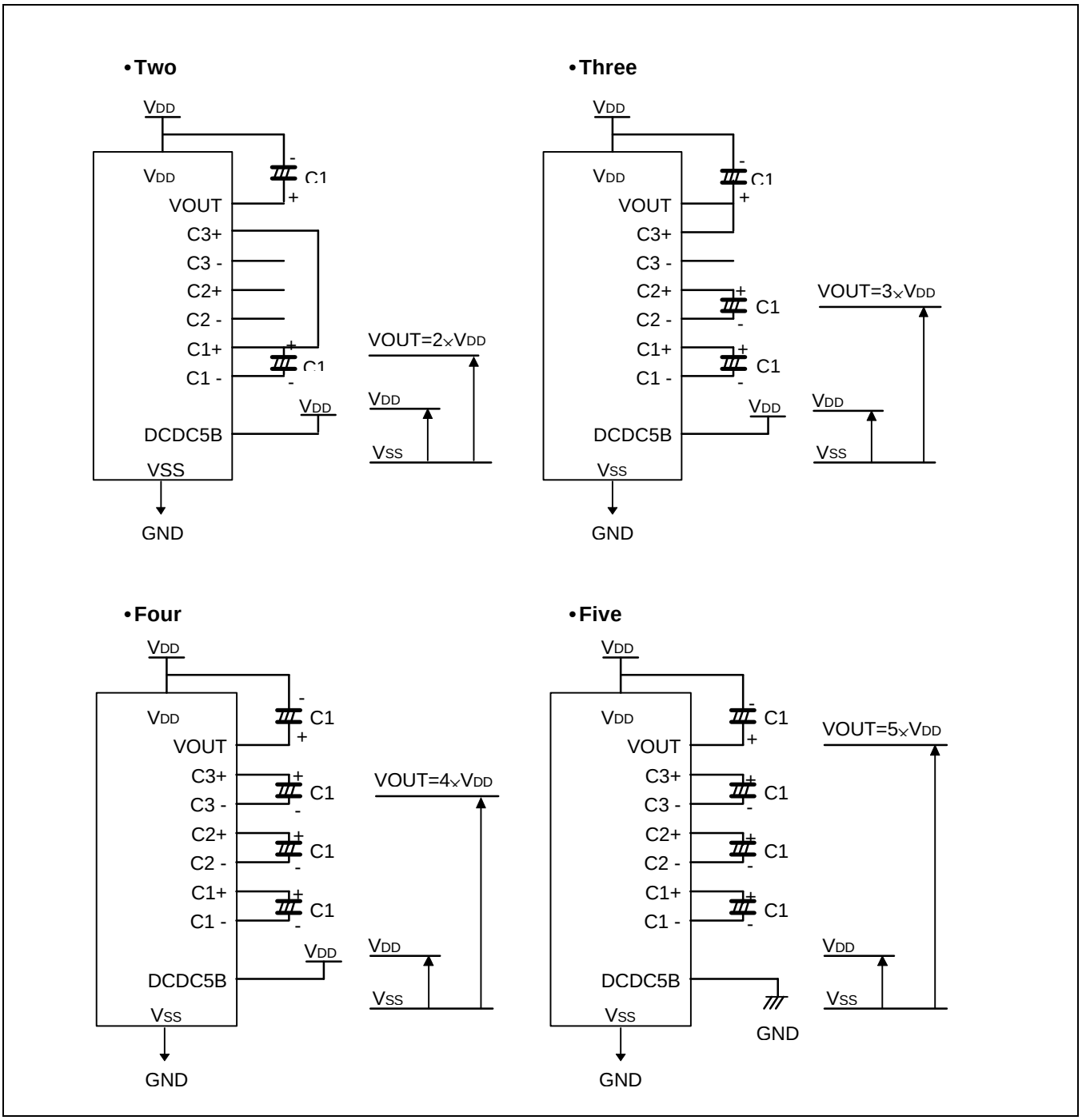


Figure 9. Boosting Two/Three/Four/Five Times Circuit

VOLTAGE REGULATOR CIRCUITS

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure. 10, it is necessary to be applied internally or externally.

For the Equation 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by INTRS pin. Voltage of electronic volume (V_{EV}) is determined by Equation 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in Table 11.

<Equation 1>

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V]$$

<Equation 2>

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{300}\right) \times V_{REF} \quad [V]$$

Table 11. V_{REF} Voltage at Ta = 25°C

TEMPS	Temp. Coefficient	VREF [V]
0	– 0.05% / °C	2.0
1	– 0.2% / °C	2.0

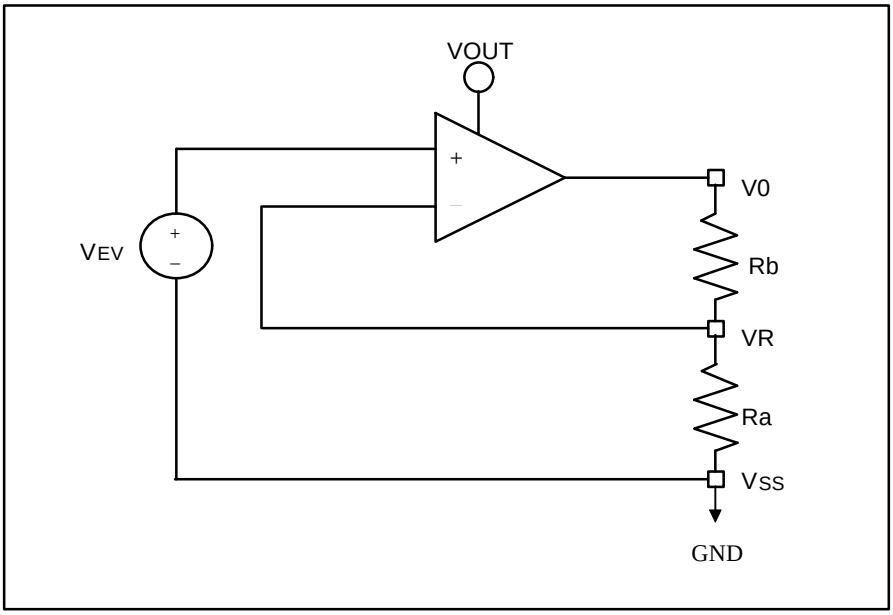


Figure 10. Internal Voltage Regulator Circuit

1) Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is high, resistor Ra is connected internally between VR pin and V_{SS}, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 12. Internal Rb/Ra Ratio Depending on 3-Bit Data (R2 R1 R0)

	3-Bit Data Settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1 + (Rb/Ra)	1.90	2.19	2.55	3.02	3.61	4.35	5.29	6.48

Figure 11. and 12. shows V0 voltage measured by adjusting the internal regulator register ratio (Rb/Ra), 6-bit electronic volume registers for each temperature coefficient at Ta = 25°C.

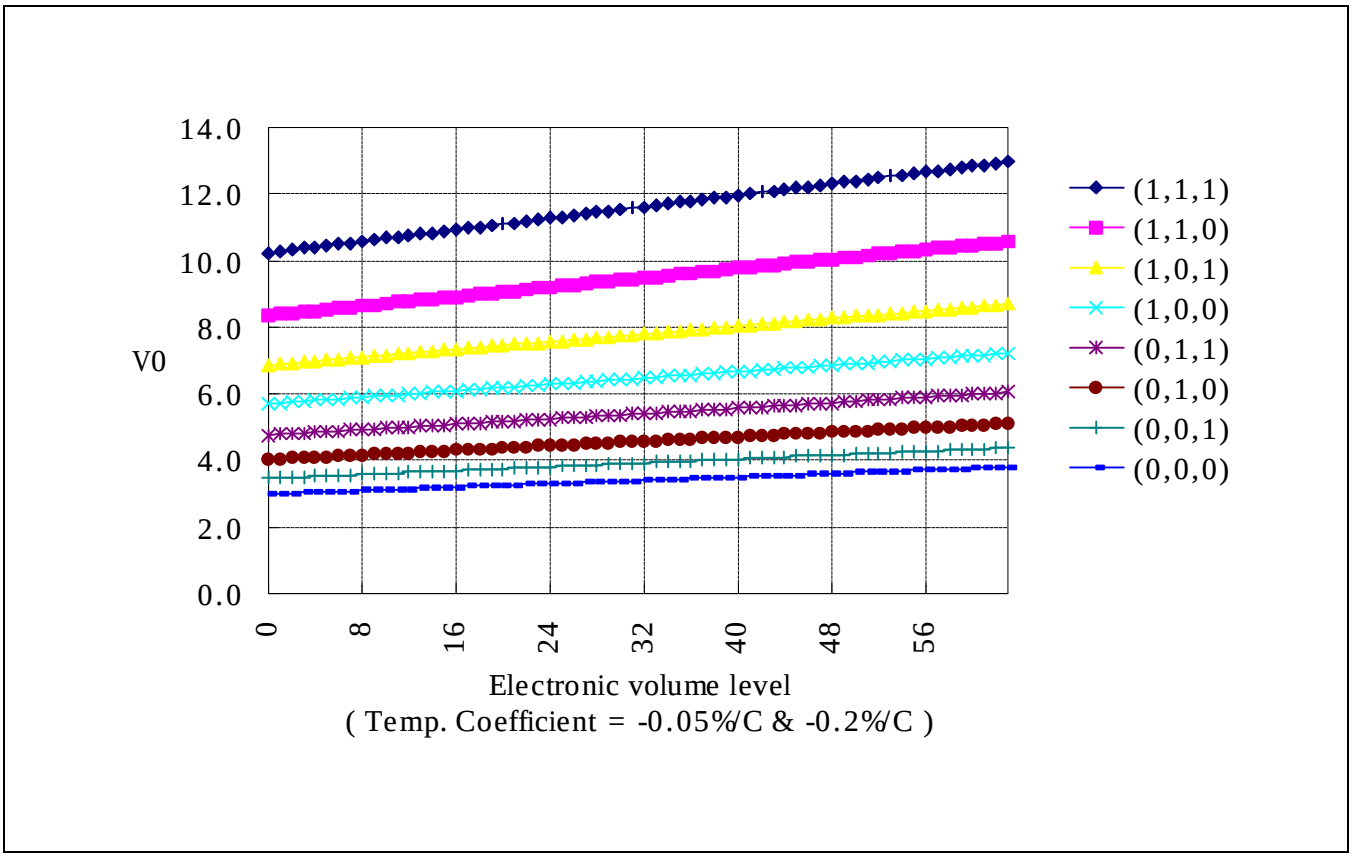


Figure 11. V0 Voltage

2) Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is low, it is necessary to connect external regulator resistor Ra between VR and V_{SS}, and Rb between V0 and VR.

Example: For the following requirements.

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1,0,0,0,0,0)
3. Maximum current flowing Ra, Rb = 1μA

<Equation 3> From Equation 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V]$$

<Equation 4> From Equation 1

$$V_{EV} = \left(1 - \frac{(63 - 32)}{300}\right) \times 2.0 \cong 1.79 \ [V]$$

<Equation 5> From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \ [\mu A]$$

From equations Equation 3, 4 and 5:

Ra = 1.79 [Ω]

Rb = 8.21 [Ω]

Table 13 shows the range of V0 depending on the above requirements.

Table 13. The Range of V0 Depending

	Electronic Volume Level				
	0	.....	32	.....	63
V0	8.83	.....	10.00	.....	11.17

VOLTAGE FOLLOWER CIRCUITS

V_{LCD} voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower to increase drive capability. Table 14 shows the relationship between V1 – V4 level and each duty ratio.

Table 14. The Relationship Between V1- V4 Level and Each Duty Ratio

Duty Ratio	DUTY 1	DUTY 0	LCD Bias	V1	V2	V3	V4
1/33	L	L	1/5	4/5 × V0	3/5 × V0	2/5 × V0	1/5 × V0
			1/6	5/6 × V0	4/6 × V0	2/6 × V0	1/6 × V0
1/49	L	H	1/6	5/6 × V0	4/6 × V0	2/6 × V0	1/6 × V0
			1/8	7/8 × V0	6/8 × V0	2/8 × V0	1/8 × V0
1/65	H	L/H	1/7	6/7 × V0	5/7 × V0	2/7 × V0	1/7 × V0
			1/9	8/9 × V0	7/9 × V0	2/9 × V0	1/9 × V0

REFERENCED POWER SUPPLY CIRCUIT FOR DRIVING LCD PANEL

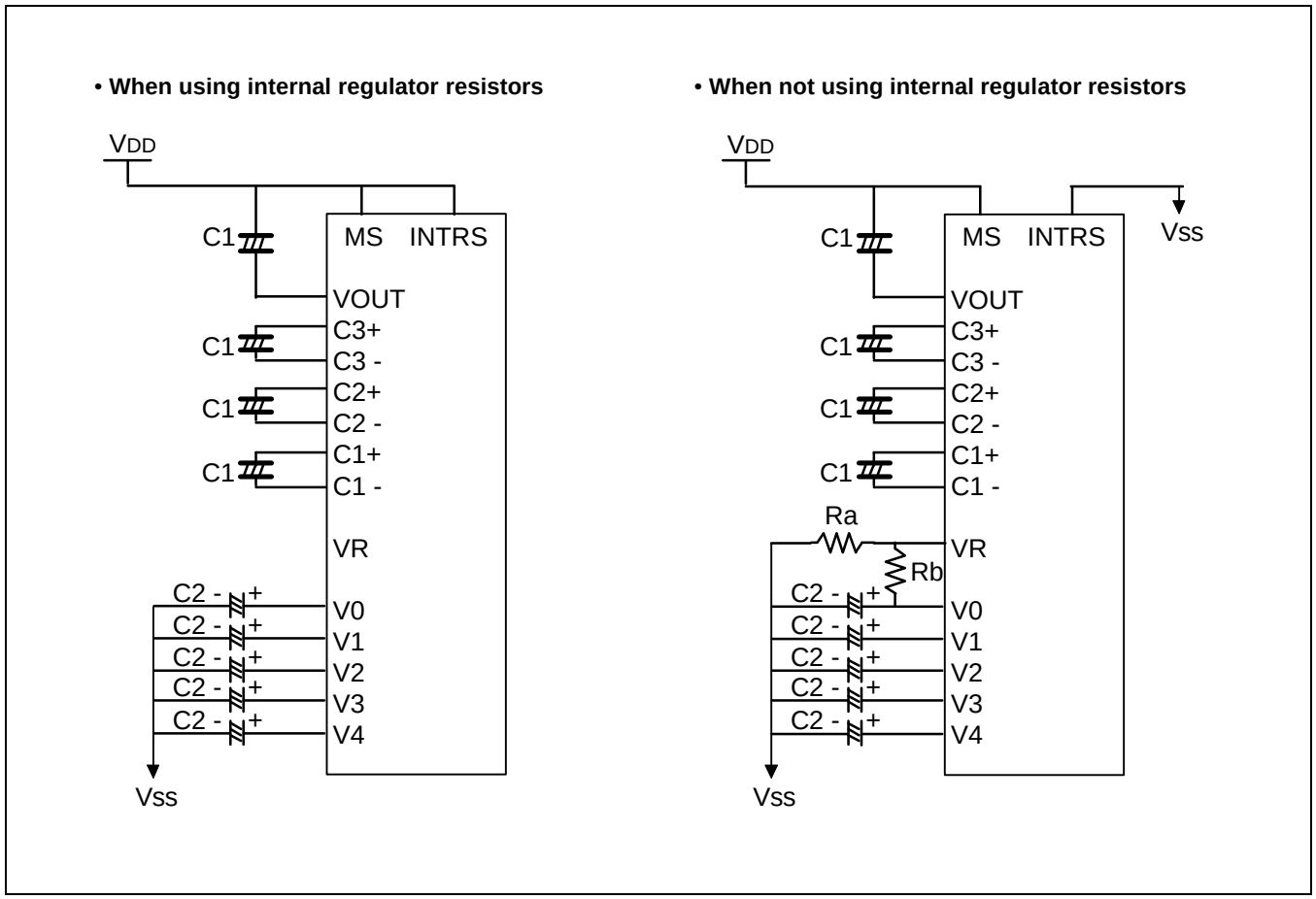


Figure 12. When Using All LCD Power Circuits (4-Times, VC: On, V/R: On, V/F: On)

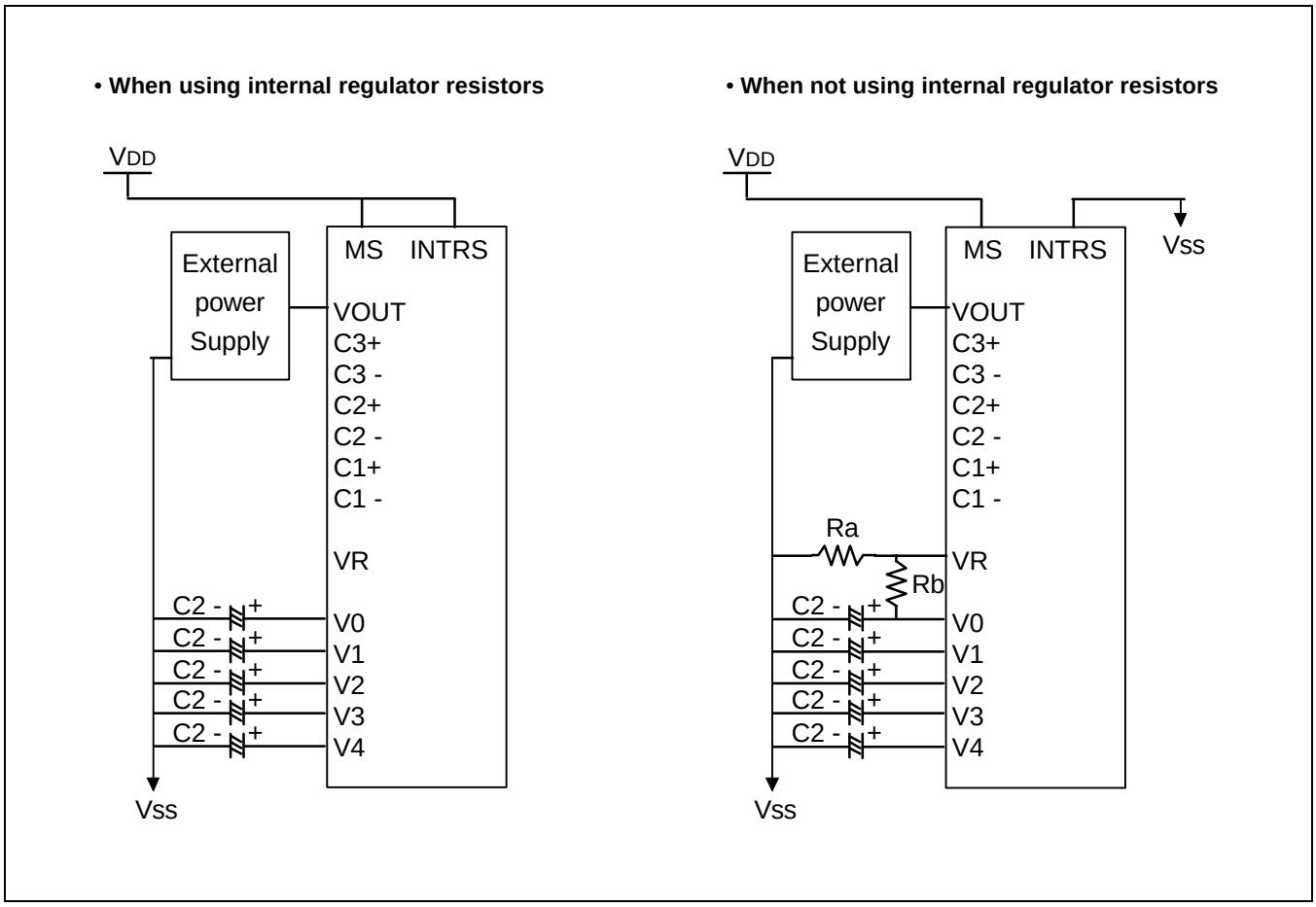


Figure 13. When Using Some LCD Power Circuits (V/C: Off, V/R: On, V/F: On)

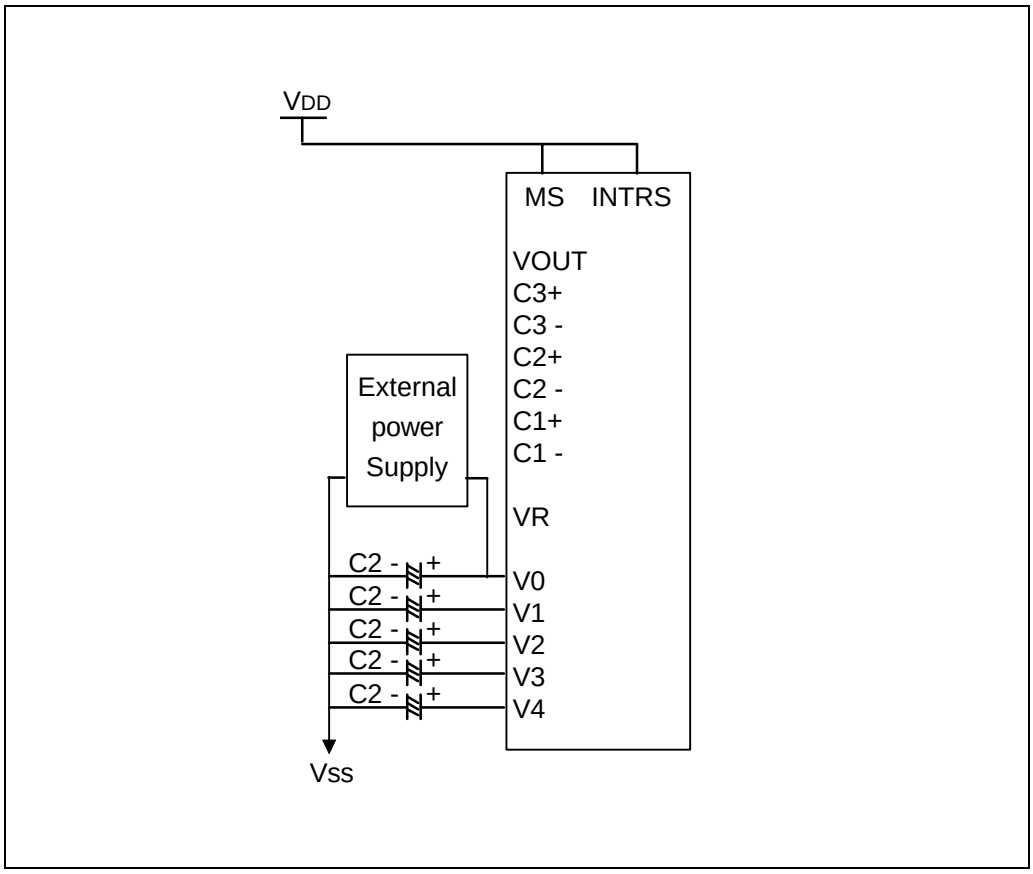
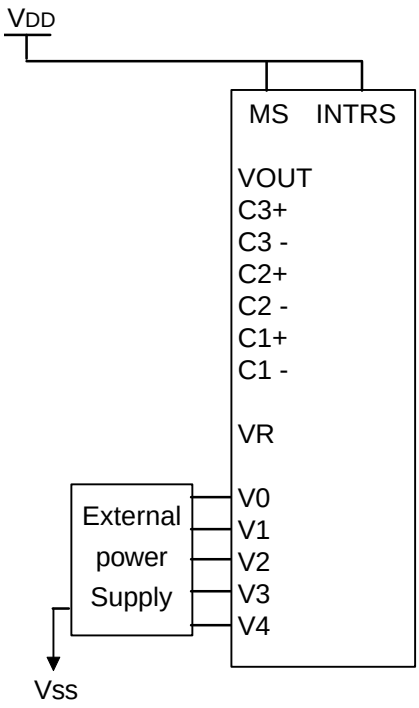


Figure 14. When Using Some LCD Power Circuits (V/C: Off, V/R: Off, V/F: On)



Value of External Capacitance

Item	Value	Unit
C1	1.0 – 4.7	μF
C2	0.47– 1.0	

Figure 15. When Not Using Any Internal LCD Power Circuits (V/C: Off, V/R: Off, V/F: Off)

RESET CIRCUIT

Internal function can be initialized by setting RESETB to low or Reset instruction.

When RESETB becomes low, following procedure occurs.

- Display ON/OFF:OFF
- Entire display ON/OFF: OFF (Normal)
- ADC select: OFF (Normal)
- Reverse display ON/OFF : OFF (Normal)
- Power control register (VC, VR, VF) = (0, 0, 0)
- LCD bias ratio: 1/7 (1/65 Duty), 1/6 (1/49 Duty), 1/5 (1/33) Duty
- Read-Modify-write: OFF
- SHL select: 0
- Static indicator mode: OFF
  Static indicator register: (S1, S0) = (0, 0)
- Display start line: 0 (First)
- Column address: 0
- Page address: 0
- Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
- Reference voltage set: OFF,
  Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

When RESET instruction is issued, following procedure occurs.

- Read-Modify-write: OFF
- Static indicator mode: OFF
  Static indicator register: (S1, S0) = (0, 0)
- SHL select: 0
- Display start line: 0 (First)
- Column address: 0
- Page address: 0
- Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
- Reference voltage set: OFF
  Reference voltage control register (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

While RESETB is Low or Reset instruction is executed, no instruction other than read status can be accepted. Reset status appears at DB4. After DB4 becomes low, any instruction can be accepted. RESETB pin must be connected to the reset pin of MPU. Then initialize the MPU and this LSI at the same time. The initialization by RESETB pin is essential before use.

INSTRUCTION DESCRIPTION

Table 15. Instruction Table

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON/ OFF	RESETB	0	0	0	0	Read the internal status
Display ON/OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON/OFF LCD panel When DON=0, display is OFF When DON=0, display is On
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM1
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC=0 normal direction (SEG1→SEG132) When ADC=1 reverse direction (SEG132→SEG1)
Reverse display ON/ OFF	0	0	1	0	1	0	0	1	1	REV	Select normal/reverse display When REV=0 normal When REV=1 reverse
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	Select normal display / entire display ON When EON=0, normal display When EON=1, entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL=0 normal direction (COM1→COM64) When SHL=1 reverse direction (COM64→COM1)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select resistance ratio of the regulator resistor
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	–	–	–	–	–	–	–	–	–	–	Compound instruction of display OFF and entire display ON
Test instruction	0	0	1	1	1	1	×	×	×	×	Don't use this instruction.

NOTE: "×" = Don't care

READ DISPLAY DATA

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**1**	**Read Data**							

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

WRITE DISPLAY DATA

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	**0**	**Write Data**							

8-bit display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

READ STATUS

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**BUSY**	**ADC**	**ON/OFF**	**RESETB**	**0**	**0**	**0**	**0**

Indicates the internal status conditions.

Flag	Description
BUSY	The device is busy when carrying out internal operation or reset. All instructions are rejected until BUSY goes to low. 0: Chip is active, 1: Chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: Reverse direction (SEG132 → SEG1), 1: Normal direction (SEG1 → SEG132)
ON/OFF	Indicates display ON / OFF status. 0: Display ON, 1: Display OFF
RESETB	Indicates initialization is in progress by RESETB signal. 0: Chip is active, 1: Chip is being reset.

DISPLAY ON/OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**DON**

Turns the display ON or OFF

DON	
1	Display ON
0	Display OFF

INITIAL DISPLAY LINE

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**1**	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**

Sets the line address of display RAM to determine the initial display line. The RAM display data is displayed at the top row (COM1 when SHL = L, COM64 when SHL = H) of the LCD panel.

ST5	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**	**Line Address**
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

REFERENCE VOLTAGE SELECT

Set reference voltage mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Set reference voltage register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	×	×	**SV5**	**SV4**	**SV3**	**SV2**	**SV1**	**SV0**

Consists of two bytes instruction. The first byte sets reference voltage mode, the second one updates the contents of reference voltage register. After second instruction reference voltage mode is released.

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

SET PAGE ADDRESS

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**1**	**P3**	**P2**	**P1**	**P0**

Sets the page address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the column address, the page address defines the address of the display RAM to write or read display data. Changing the page address doesn't affect the display status.

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

SET COLUMN ADDRESS

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**1**	**Y7**	**Y6**	**Y5**	**Y4**

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**0**	**Y3**	**Y2**	**Y1**	**Y0**

Sets the column address of the display RAM from the microprocessor into the column address register. The column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased, starting with the address stored in the column address register and continuously rotating right.

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

ADC SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**ADC**

Changes the relationship between the RAM column address and segment driver. The direction of the segment driver output pins can be reversed by software. This makes the IC layout flexible in the LCD module assembly.

ADC	
0	Normal direction (SEG1 → SEG132)
1	Reverse direction (SEG132 → SEG1)

NORMAL / REVERSE DISPLAY

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**REV**

Reverses the display status on the LCD panel without rewriting the contents of the display data RAM.

REV	RAM Bit Data = "1"	RAM Bit Data = "0"
0 (Normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (Reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

ENTIRE DISPLAY ON / OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**EON**

Forces all LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are put on hold. This instruction has priority over the reverse display ON / OFF instruction.

EON	
0	Normal display
1	Entire display on

LCD BIAS SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**BIAS**

Selects the LCD bias ratio of the voltage required for driving the LCD.

Duty Ratio	Duty 1	Duty 0	LCD BIAS	
			BIAS = 0	BIAS = 1
1/33	0	0	1/5	1/6
1/49	0	1	1/6	1/8
1/65	1	0/1	1/7	1/9

SET MODIFY-READ

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data. It reduces the load of the microprocessor when the data of a specific area is repeatedly changed during cursor blinking. This mode is cancelled by the reset modify-read instruction.

RESET MODIFY-READ

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This instruction cancels the modify read mode, and makes the column address return to its initial value just before the set modify read instruction starts.

RESET

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This instruction resets the initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply which is initialized by the RESETB pin.

SHL SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**1**	**0**	**0**	**SHL**	´	´	´

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

SHL	
0	Normal direction (COM1 → COM64)
1	Reverse direction (COM64 → COM1)

POWER CONTROL

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**1**	**VC**	**VR**	**VF**

Selects one out of eight power circuit functions by using a 3-bit register. An external power supply and a part of internal power supply functions can be used simultaneously.

VC, VR, VF	Indicates whether the voltage converter / regulator / follower turns on or not
0	Off
1	On

REGULATOR RESISTOR SELECT

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**0**	**R2**	**R1**	**R0**

Selects resistance ratio of the resistor used in the Voltage Regulator. See Voltage Regulator section in Power Supply Circuit.

R2	**R1**	**R0**	**[Rb/Ra] Ratio**
0	0	0	Small
0	0	1	:
:	:	:	:
1	1	0	:
1	1	1	Large

SET STATIC INDICATOR STATE

Set Static Indicator Mode (On / Off)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**SM**

SM	Static Indicator
0	Static Indicator Off
1	Static Indicator On

Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	×	×	×	×	×	×	**S1**	**S0**

This instruction sets the static indicator ON / OFF. When it is on, the static indicator operates and blinks at an interval of approximately one second.

S1	**S0**	**Status of Static Indicator Output**
0	0	OFF
0	1	ON (About 1 Second Blinking)
1	0	ON (About 0.5 Second Blinking)
1	1	ON (Always ON)

POWER SAVE (COMPOUND INSTRUCTION)

If the Entire Display ON/OFF instruction is issued during the display OFF state, KS0713 enters the power save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one mode of sleep and standby mode. When Static Indicator mode is ON, standby mode is issued. When OFF, sleep mode is issued. Power Save mode is released by the Display ON & Entire Display OFF instruction.

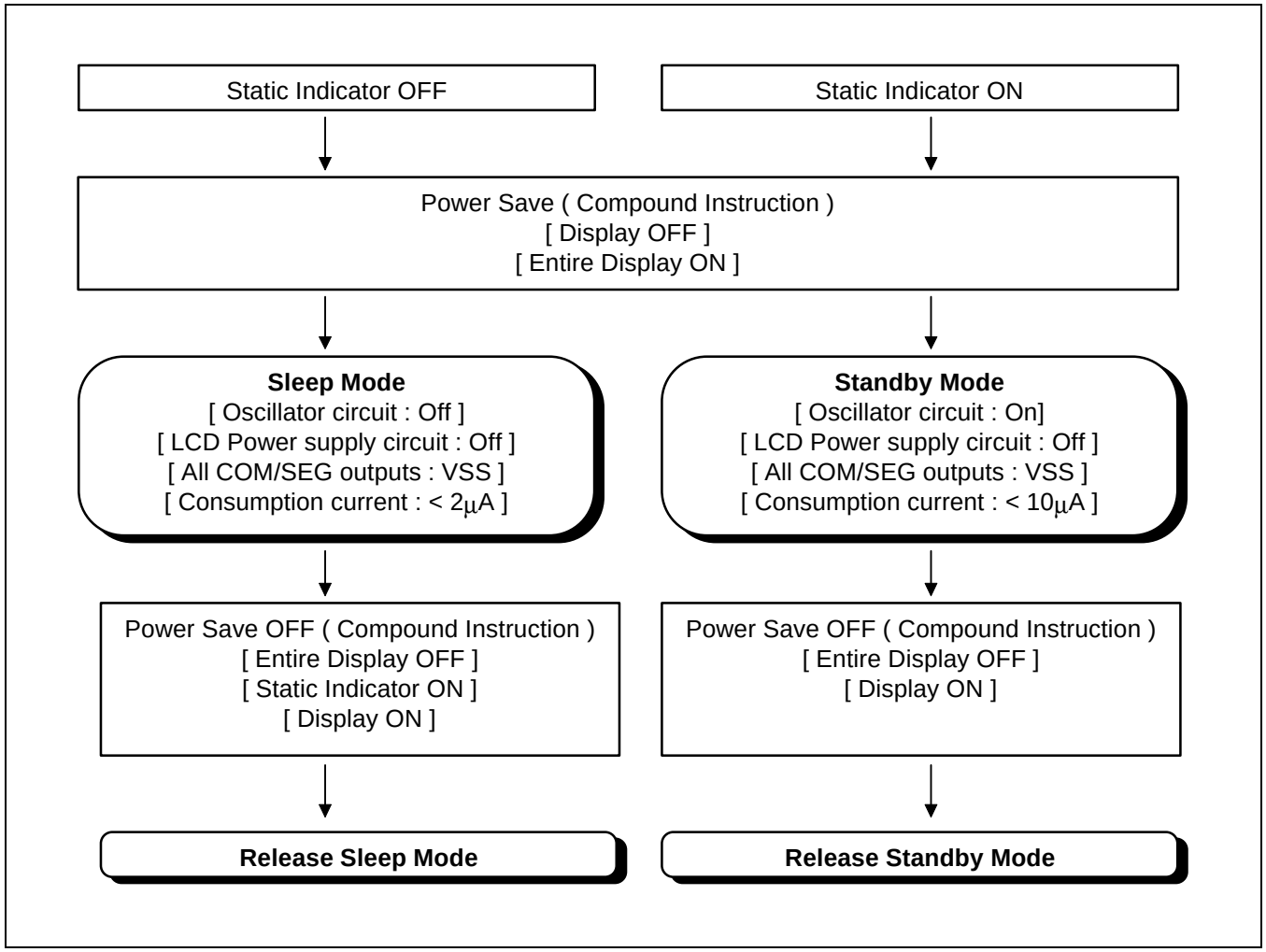


Figure 16. Power Save (Compound Instruction)

REFERENTIAL INSTRUCTION SETUP FLOW

— Initializing with the built-in power supply circuits

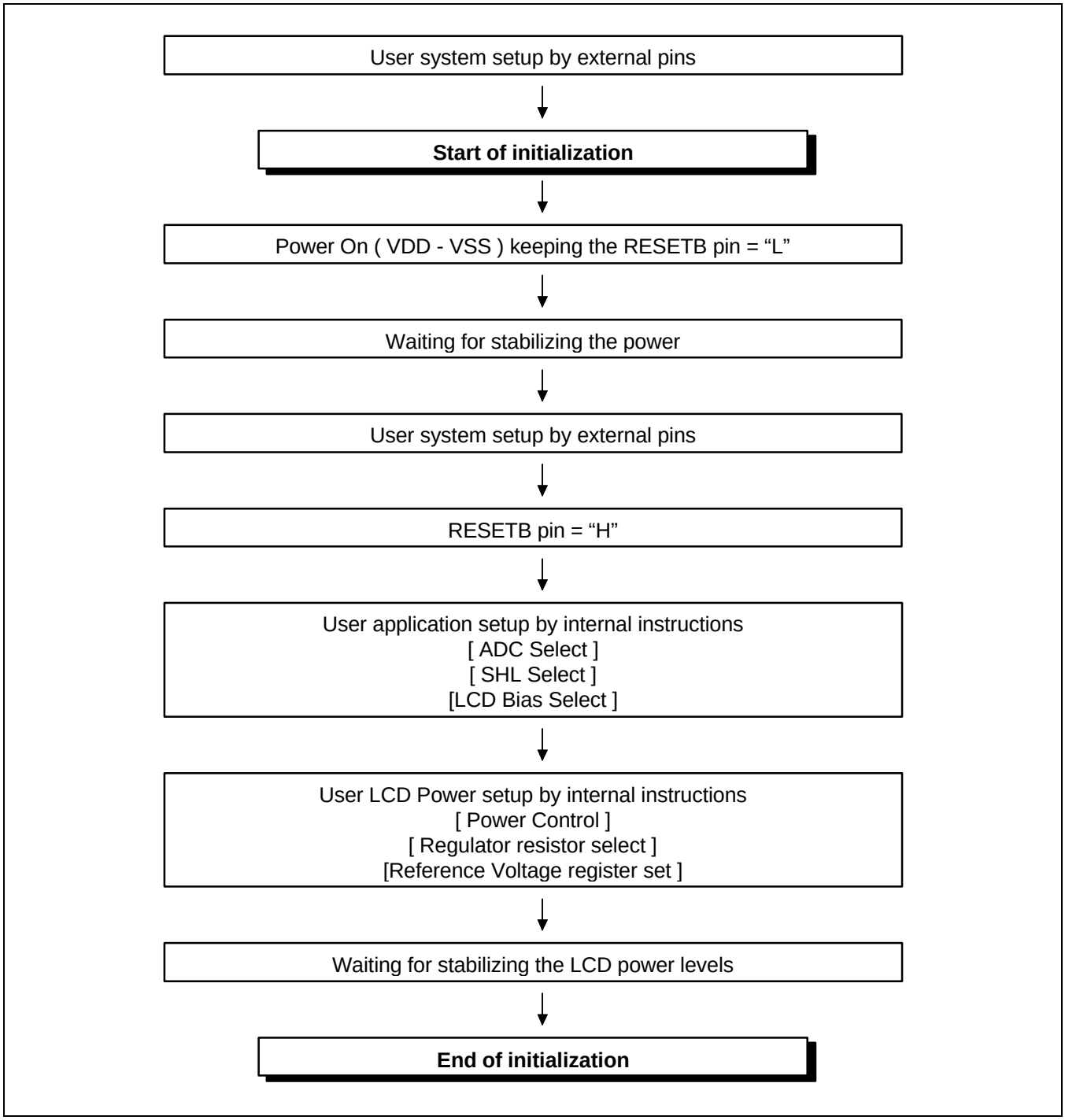


Figure 17. Initializing With The Built-in Power Supply Circuits

— Initializing without the built-in power supply circuits

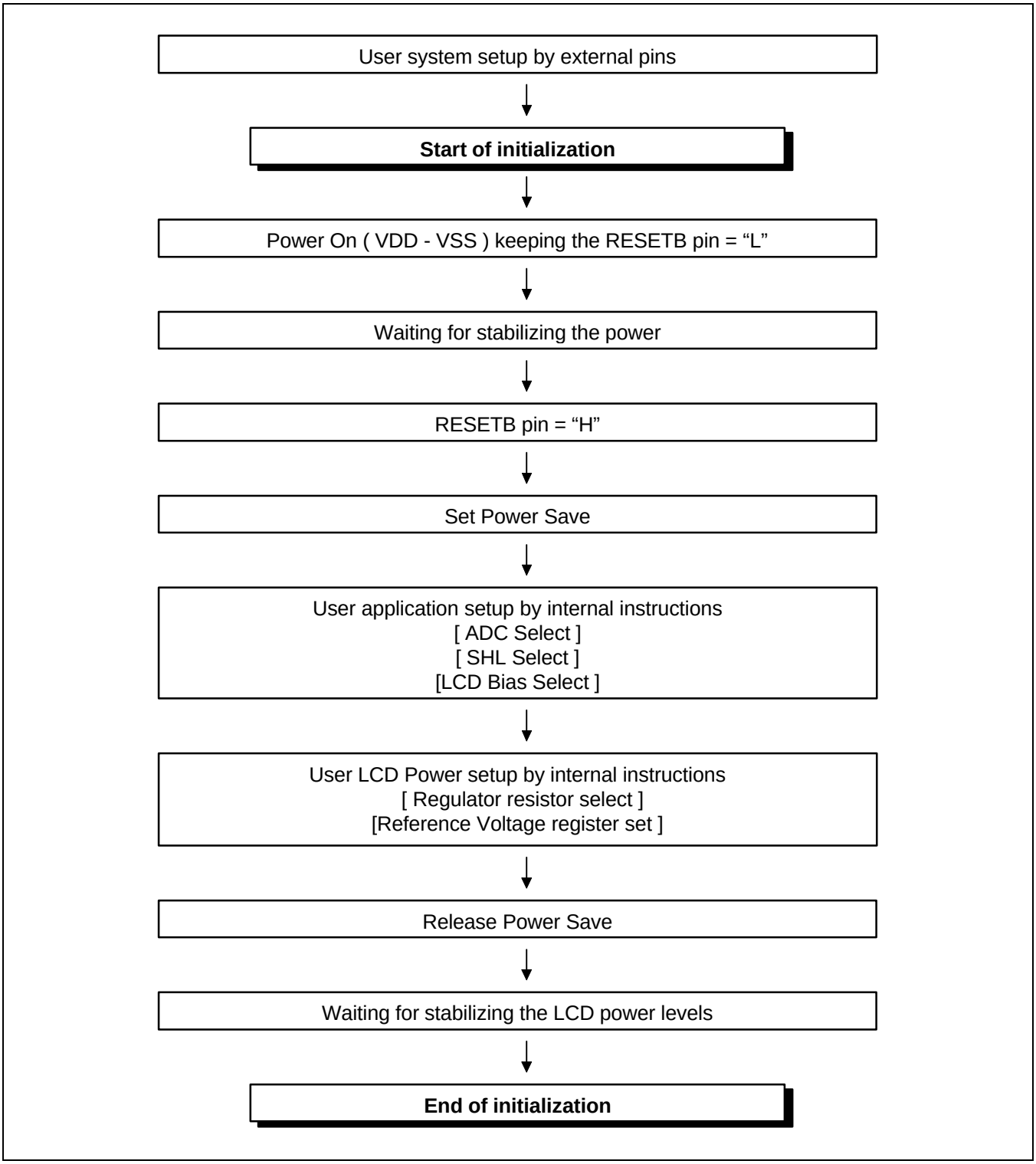


Figure 18. Initializing Without the Built-In Power Supply Circuits

— Data displaying

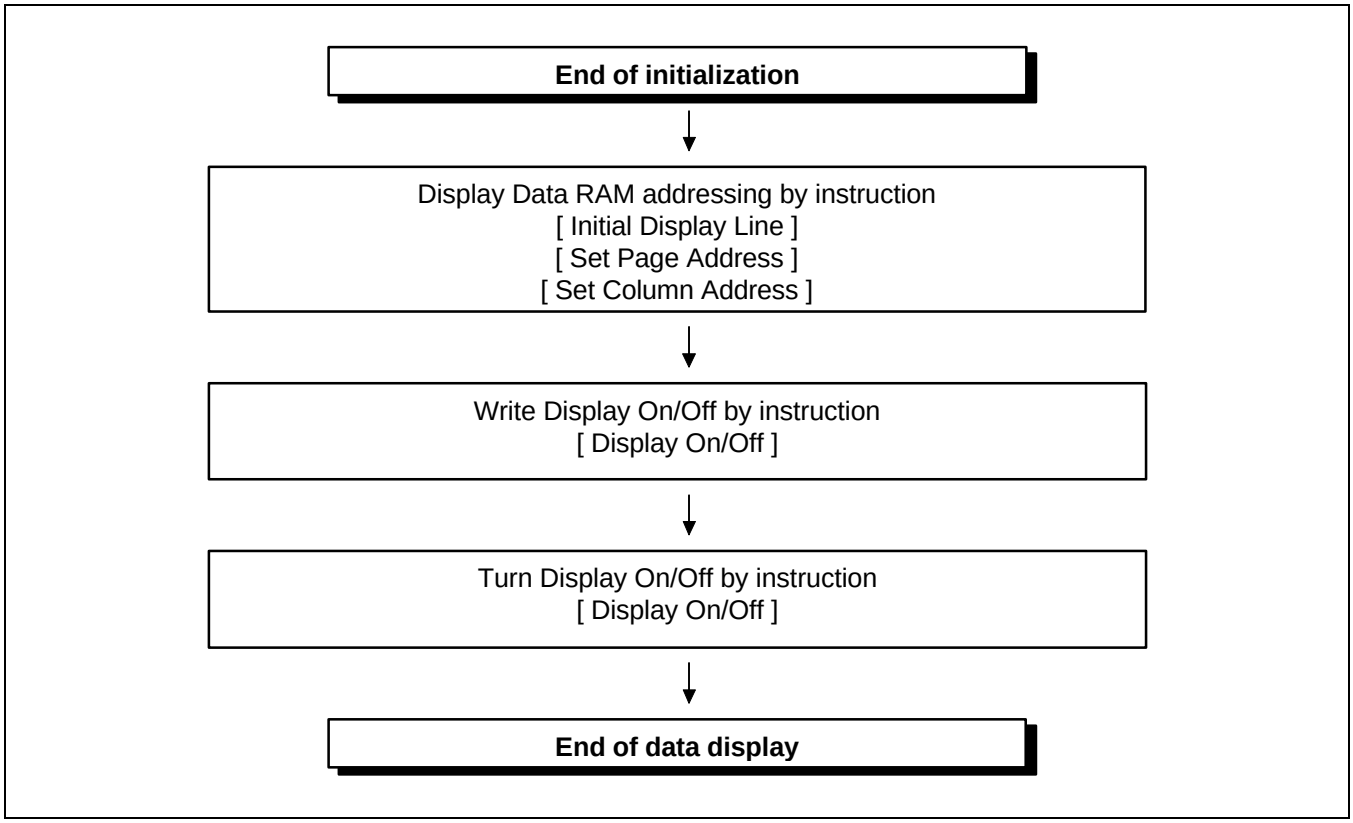


Figure 19. Data Displaying

— Power Off

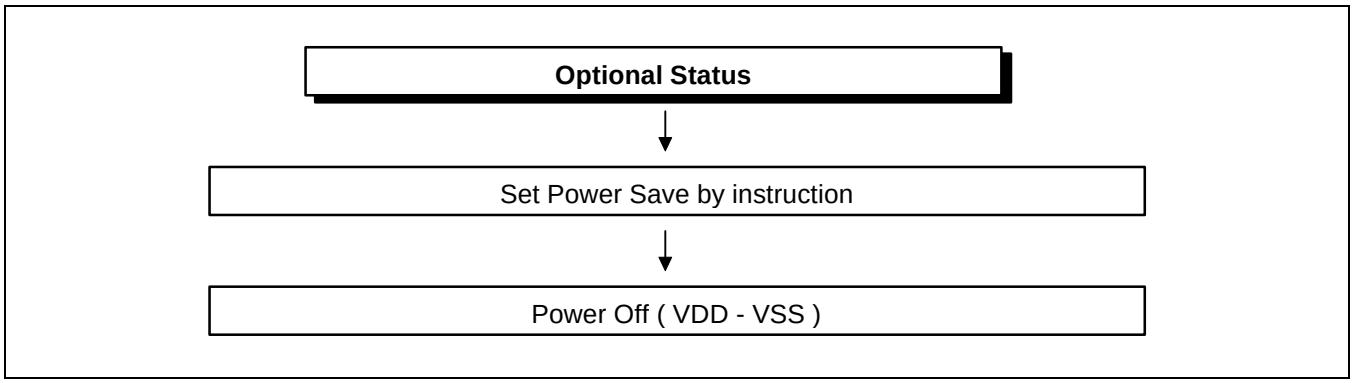


Figure 20. Power Off

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 16. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	– 0.3 to + 7.0	V
	V_{LCD}	+ 0.3 to + 17.0	
Input voltage range	V_{IN}	– 0.3 to V_{DD} + 0.3	
Operating temperature range	T_{OPR}	– 40 to + 85	°C
Storage temperature range	T_{STR}	– 55 to +125	

NOTES:

1. V_{DD} and V_{LCD} are based on V_{SS} = 0 V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS} must always be satisfied (V_{LCD} = V0 – V_{SS}).
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 17. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Operating voltage (1)		V_{DD}		2.4	–	5.5	V	V_{DD} (1)
Operating voltage (2)		V0		4.0	–	15.0		V0 (2)
Input voltage	High	V_{IH}		0.8 V_{DD}	–	V_{DD}		(3)
	Low	V_{IL}		V_{SS}	–	0.2 V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = – 0.5mA	0.8 V_{DD}	–	V_{DD}		(4)
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	–	0.2 V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	– 1.0	–	+ 1.0	µA	(5)
Output Leakage Current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	– 3.0	–	+ 3.0		(6)
LCD driver ON resistance		R_{ON}	Ta= 25 °C,V0 = 8V	–	2.0	3.0	kΩ	SEGn COMn (7)
Oscillator frequency (1)	Internal	f_{OSC}	Ta = 25 °C, Duty ratio = 1/33 or 1/65	17	22	27	kHz	CL (8)
	External	f_{CL}		4.25	5.50	6.75		
Oscillator frequency (2)	Internal	f_{OSC}	Ta = 25 °C, Duty ratio = 1/49	20	25	30		CL (8)
	External	f_{CL}		3.33	4.17	5.00		

Table 17. DC Characteristics (Continued)

(V_{SS} = 0V, V_{DD} = 2.4V to 5.5V, Ta = – 40 to 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Voltage Converter / Regulator / Follower							
Voltage converter input voltage	V_{DD}	× 2	2.4	–	5.5	V	V_{DD}
		× 3	2.4	–	5.0		
		× 4	2.4	–	3.75		
		× 5	2.4	–	3.0		
Voltage converter output voltage	VOUT	× 2/× 3/× 4/× 5 voltage conversion (no-load)	95	99	–	%	VOUT
Voltage regulator operating voltage	VOUT	–	4.0	–	15.0	V	VOUT
Voltage follower operating voltage	V0	–	4.0	–	15.0		V0 (9)
Reference voltage	V_{REF0}	T_a = 25 °C, – 0.05%/ °C	1.94	2.0	2.06		(10)
	V_{REF1}	T_a = 25 °C, – 0.2%/ °C	1.94	2.0	2.06		(10)
Dynamic Current Consumption (1): When the built-In circuits is OFF (At Operate Mode).							
Dynamic current consumption (1)	I_{DD1}	VDD = 3.0V, V0 – VSS = 11.0V, 1/65 duty ratio, display pattern off	–	–	50	µA	(11)
Dynamic Current Consumption (2): When the built-in circuits is ON (At Operate Mode).							
Dynamic current consumption (2)	I_{DD2}	VDD = 3.0V, quad boosting, V0 – VSS = 11.0V, 1/65 duty ratio, display pattern off, normal power mode	–	80	100	µA	(11)
		VDD = 3.0V, quad boosting, V0 – VSS = 11.0V, 1/65 duty ratio, display pattern checker, normal power mode	–	95	160	µA	(11)
Dynamic Current Consumption (3): When the built-in power is OFF (At Access Mode).							
Dynamic current consumption (3)	I_{DD3}	VDD = 3.0V, V0 – VSS = 11.0V, f_{cyc} = 1MHz	–	–	1	mA	
Current Consumption During Power Save Mode							
Sleep mode current	I_{DDS1}	During sleep	–	–	2.0	µA	
Standby mode current	I_{DDS2}	During standby	–	–	10.0	µA	

NOTES:

1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from MPU.
2. In case of external power supply is applied.
3. CS1B, CS2, RS, DB0–DB7, E_RD, RW_WR, RESETB, MS, MI, PS, INTRS, HPM, TEMPS, BSTS, DCDC5B, CLS, CL, M, DISP pins
4. DB0–DB7, M, FRS, DISP, CL pins
5. CS1B, CS2, RS, DB0–DB7, E_RD, RW_WR, RESETB, MS, MI, PS, INTRS, HPM, TEMPS, BSTS, DCDC5B, CLS, CL, M, DISP pins
6. Applies when the DB0–DB7, M, DISP, and CL pins are in high impedance.
7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
   $R_{ON} = \Delta V / 0.1$ [kΩ] (Δ V: voltage change when ± 0.1[mA] is applied in the ON status.)
8. See Table 18 for the relationship between oscillation frequency and frame frequency.
9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
11. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
    The current flowing through voltage regulation resistors (Rb and Ra) is not included. It does not include the current of the LCD panel capacity, wiring capacity, etc.

Table 18. The Relationship Between Oscillation Frequency and Frame Frequency

DUTY Ratio	Item	f_{CL}	f_M	Remark
1/65	On-chip oscillator circuit is used	f_{OSC} / 4	f_{OSC} / (8 × 65)	• f_{OSC} = oscillation frequency • f_{CL} = display clock frequency • f_M = LCD AC signal frequency
	On-chip oscillator circuit is not used	External input (f_{CL})	f_{CL} / (2 × 65)	
1/49	On-chip oscillator circuit is used	f_{OSC} / 6	f_{OSC} / (12 × 49)	
	On-chip oscillator circuit is not used	External input (f_{CL})	f_{CL} / (2 × 49)	
1/34	On-chip oscillator circuit is used	f_{OSC} / 8	f_{OSC} / (16 × 33)	
	On-chip oscillator circuit is not used	External input (f_{CL})	f_{CL} / (2 × 33)	

AC CHARACTERISTICS

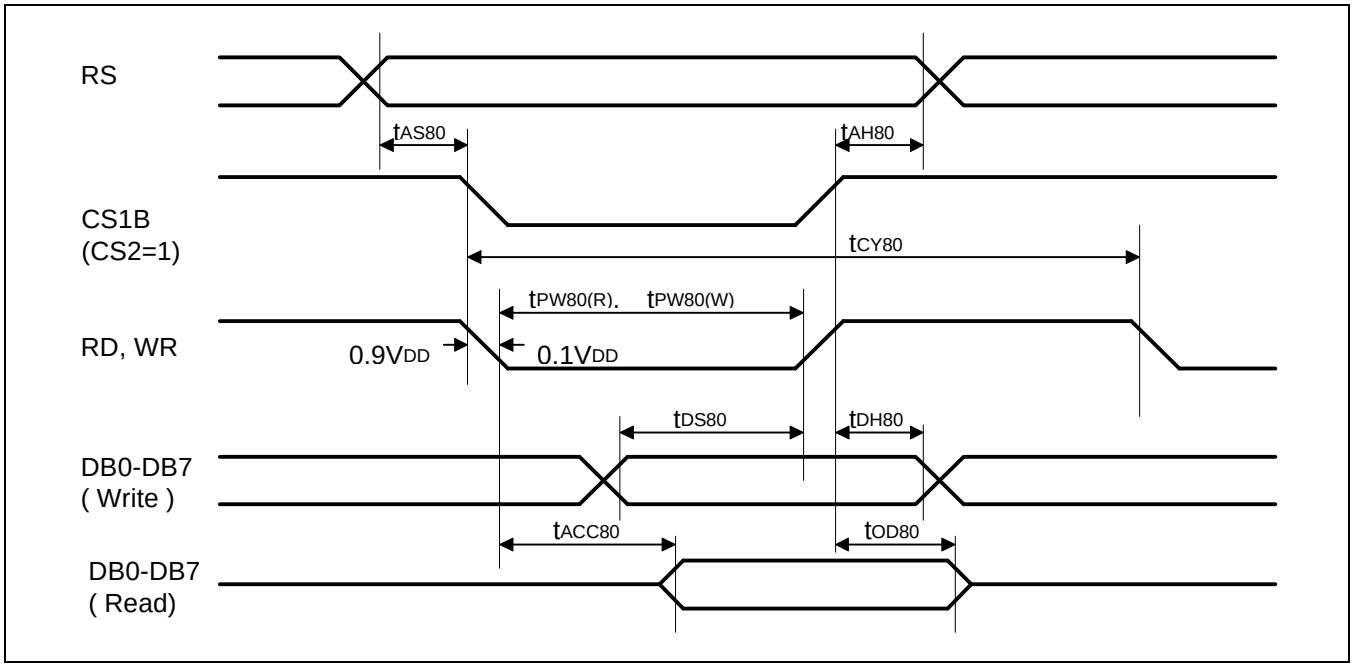


Figure 21. Read/Write Characteristics (8080-Series Microprocessor)

(V_{DD} = 2.4V–3.3V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	13 17	–	–	ns	
System cycle time	RS	t_{CY80}	400	–	–	ns	
Pulse width (WR)	RW_WR	$t_{PW80(W)}$	55	–	–	ns	
Pulse width (RD)	E_RD	$t_{PW80(R)}$	125	–	–	ns	
Data setup time Data hold time	DB0–DB7	t_{DS80} t_{DH80}	35 13	–	–	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	– 10	– –	125 90	ns ns	C_L = 100pF

(V_{DD} = 4.5V– 5.5V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	10 10	–	–	ns	
System cycle time	RS	t_{CY80}	150	–	–	ns	
Pulse width (WR)	RW_WR	$t_{PW80(W)}$	25	–	–	ns	
Pulse width (RD)	E_RD	$t_{PW80(R)}$	65	–	–	ns	
Data setup time Data hold time	DB0~DB7	t_{DS80} t_{DH80}	18 10	–	–	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	– 10	– –	65 45	ns ns	C_L = 100pF

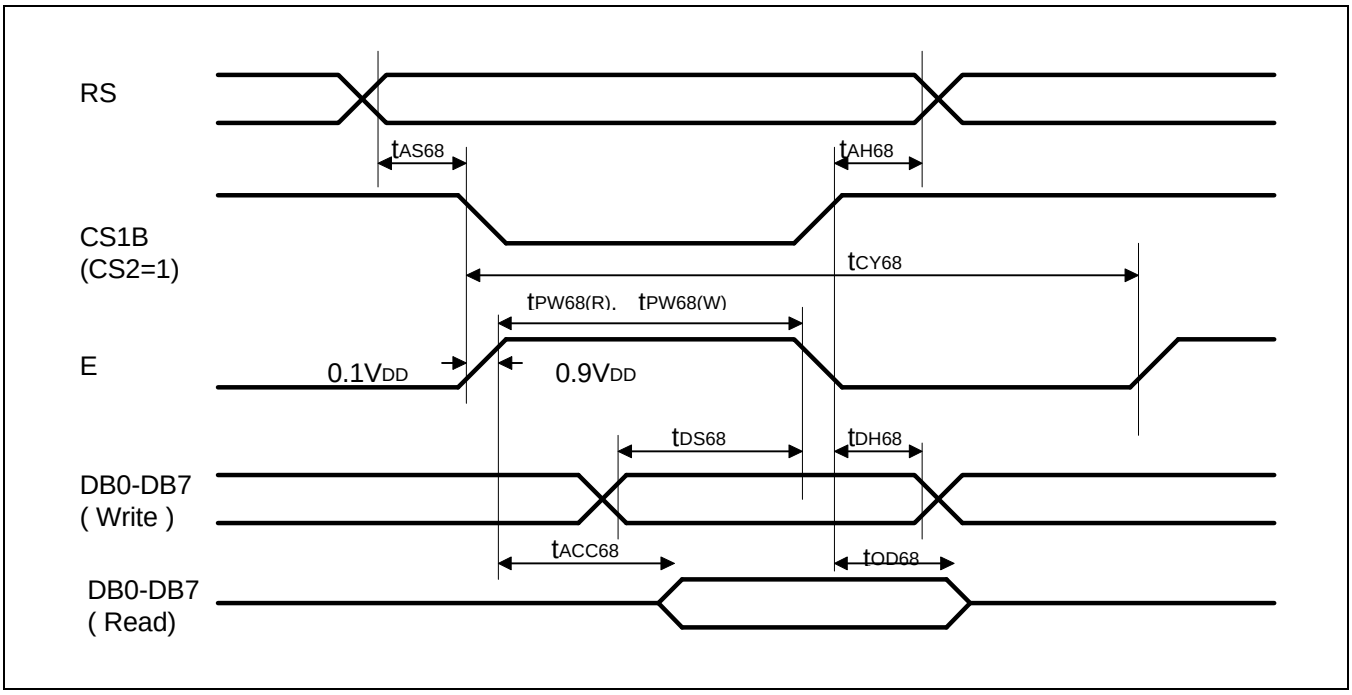


Figure 22. Read/Write Characteristics (6800-Series Microprocessor)

(V_{DD} = 2.4V– 3.3V, Ta = – 40 to + 85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	13 17	–	–	ns	
System cycle time		RS	t_{CY68}	400	–	–	ns	
Data setup time Data hold time		DB0–DB7	t_{DS68} t_{DH68}	35 13	–	–	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	– 10	– –	125 90	ns	C_L = 100pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	125 55	–	–	–	

(V_{DD} = 4.5V– 5.5V, Ta = – 40 to + 85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	10 10	–	–	ns	
System cycle time		RS	t_{CY68}	150	–	–	ns	
Data setup time Data hold time		DB0–DB7	t_{DS68} t_{DH68}	18 10	–	–	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	– 10	– –	65 45	ns ns	C_L = 100pF
Enable pulse width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	65 25	–	–	–	

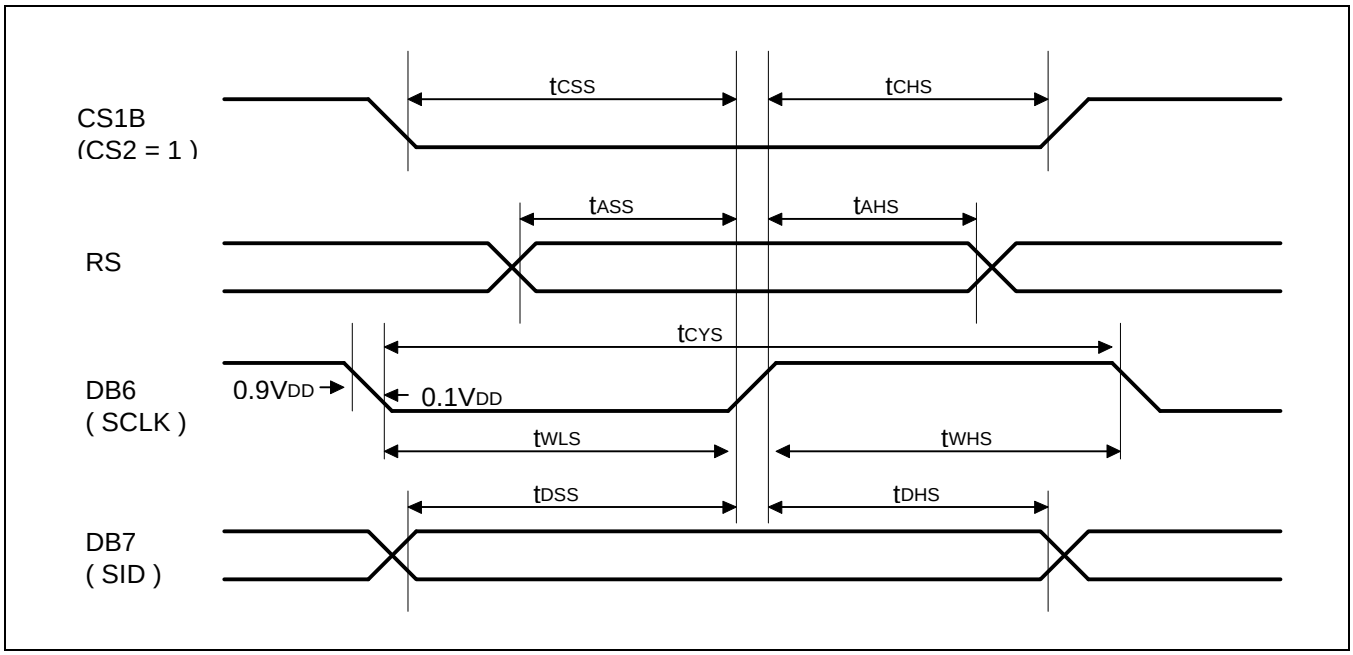


Figure 23. Serial Interface Characteristics

(V_{DD} = 2.4 V– 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	450 180 135	–	–	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	90 360	–	–	ns
Data setup time Data hold time	DB7(SID)	t_{DSS} t_{DHS}	90 90	–	–	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	55 180	–	–	ns

(V_{DD} = 4.5 V– 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	225 90 70	–	–	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	45 180	–	–	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	45 45	–	–	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	25 90	–	–	ns

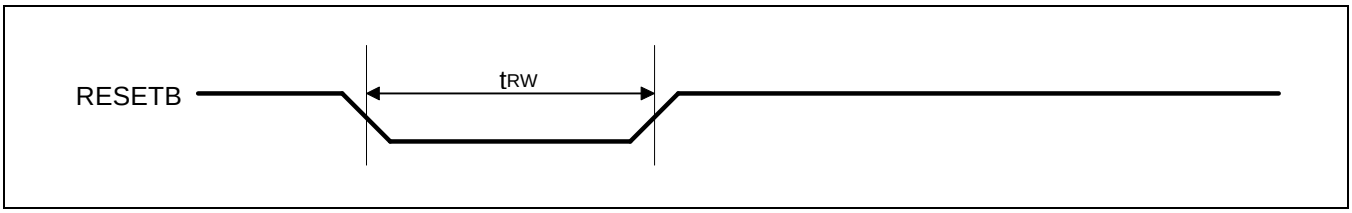


Figure 24. Serial Interface Characteristics

(V_{DD} = 2.4 V– 3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}	900	–	–	ns

(V_{DD} = 4.5 V–5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}	450	–	–	ns

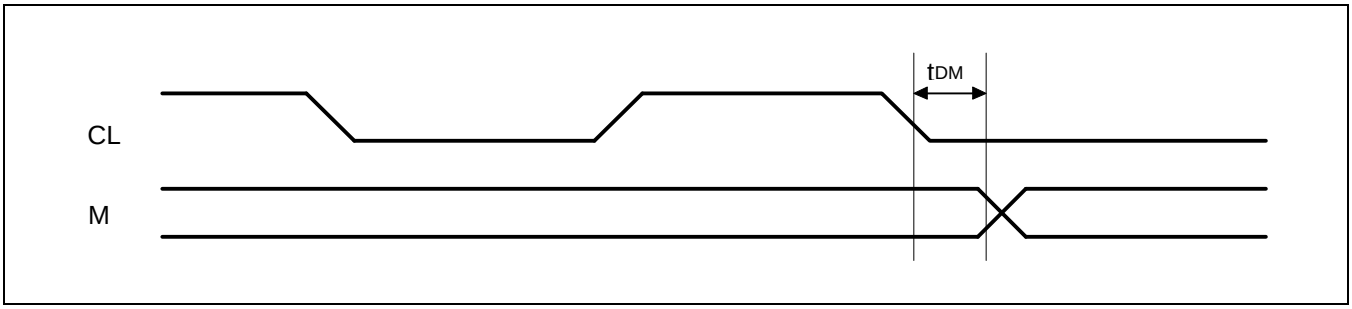


Figure 25. Display Control Output Timing

(V_{DD} = 2.4 V–3.3 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
M delay time	M	t_{DM}	–	13	70	ns

(V_{DD} = 4.5 V– 5.5 V, Ta = – 40 to + 85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit
M delay time	M	t_{DM}	–	10	35	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

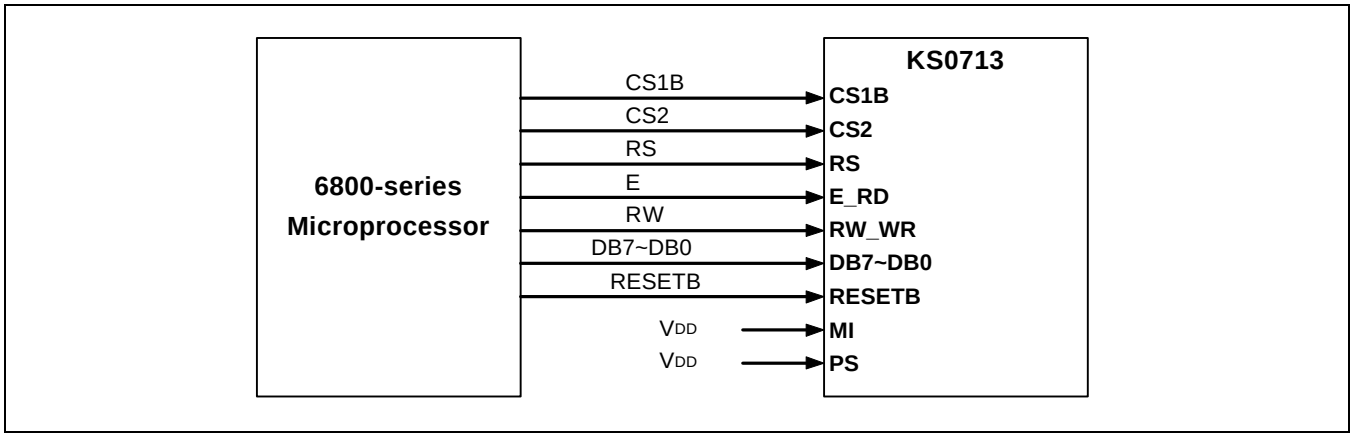


Figure 26. Interfacing with the 6800-Series (PS = "H", MI = "H")

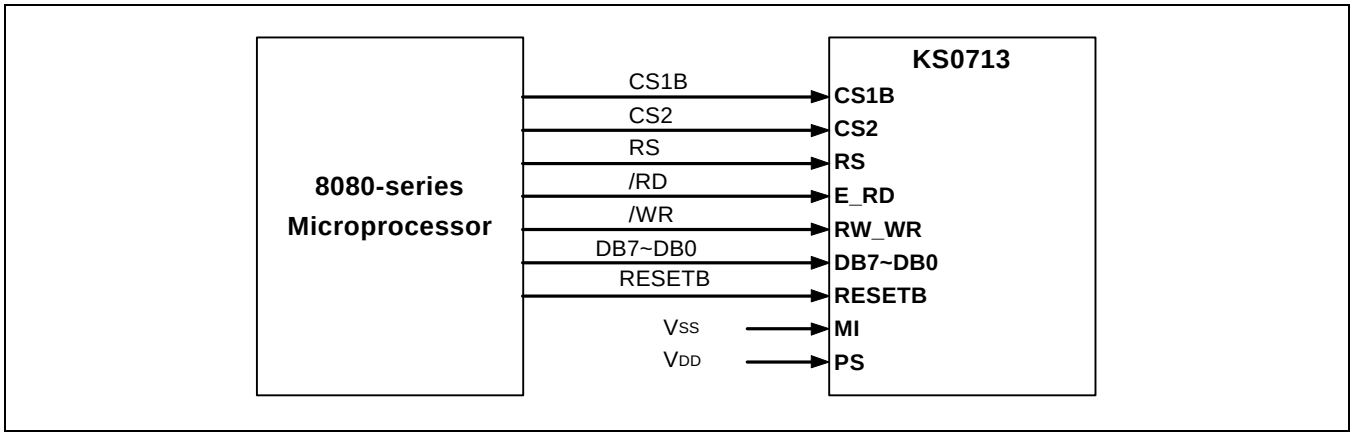


Figure 27. Interfacing with the 8080-Series (PS = "H", MI = "L")

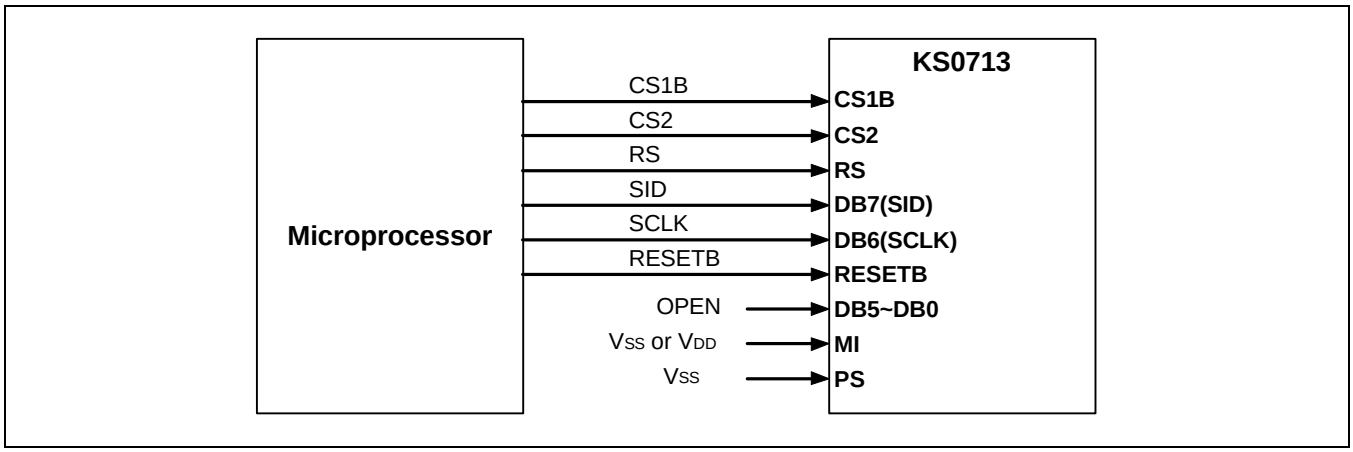


Figure 28. Serial Interface (PS = "L", MI = "H/L")

CONNECTIONS BETWEEN KS0713 AND LCD PANEL

Single-Chip Structure (1/65 Duty Configurations)

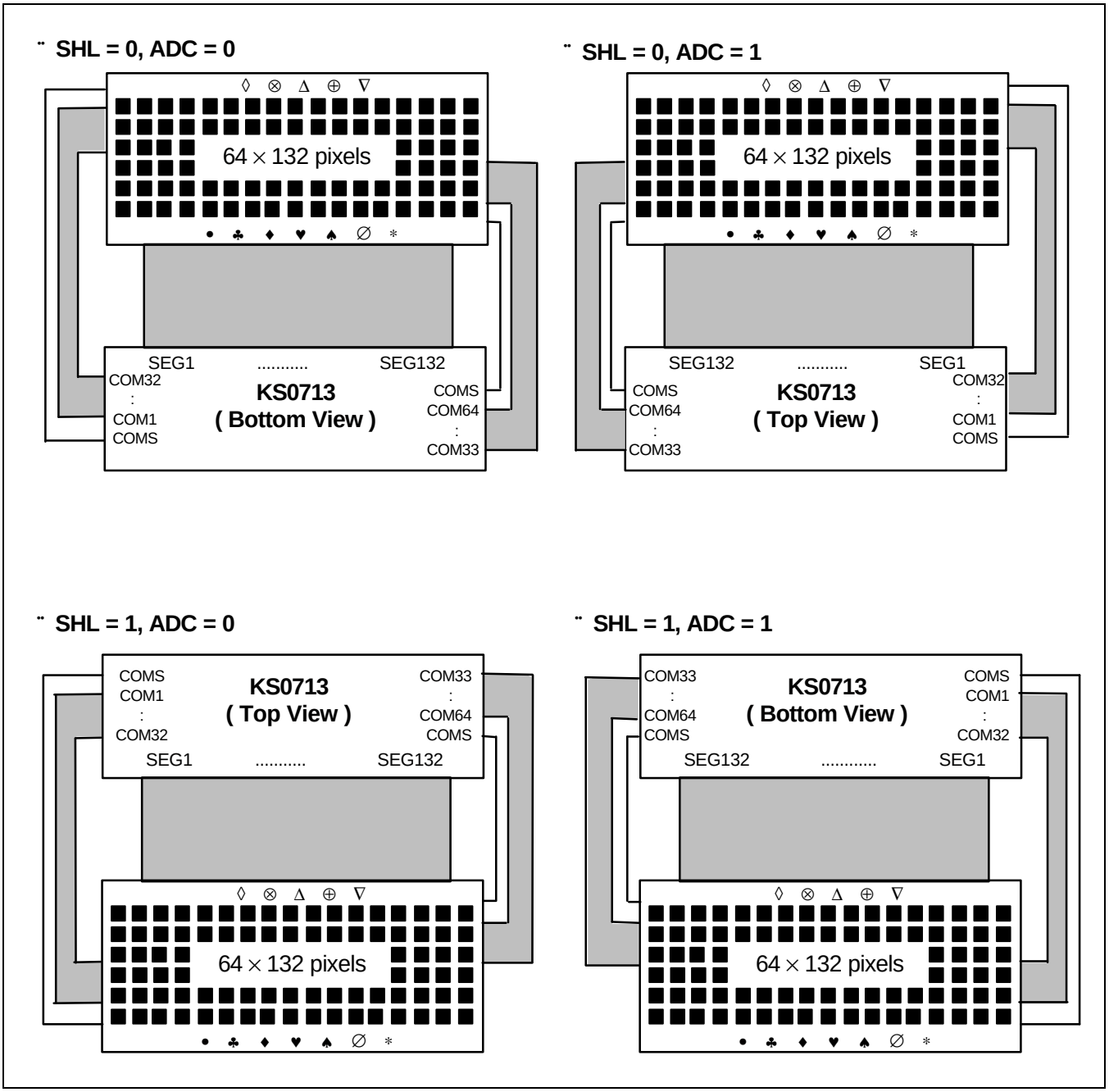


Figure 29. Single-Chip Structure (1/65 Duty Configurations)

Single-Chip Structure (1/49 Duty Configurations)

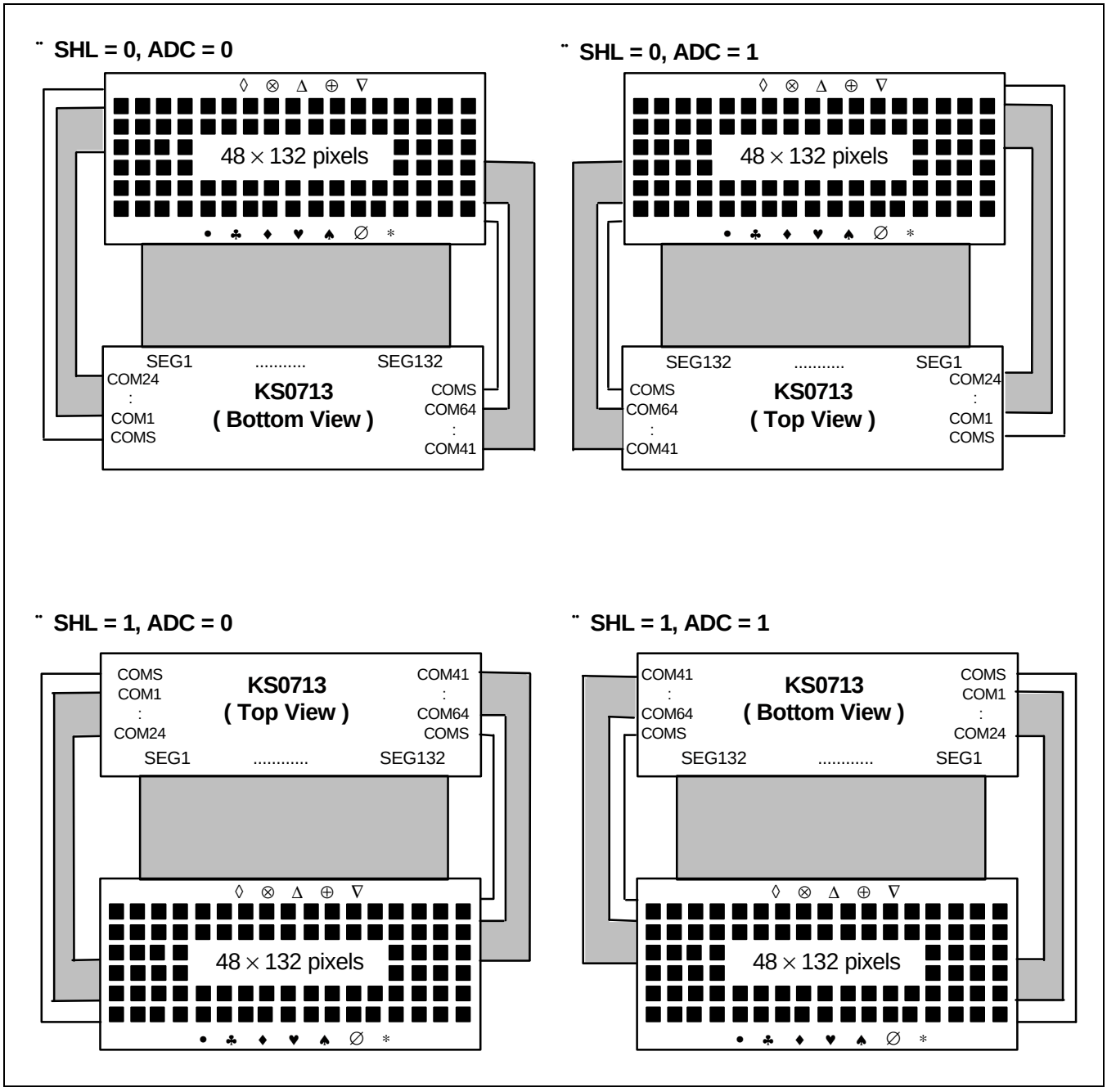


Figure 30. Single-Chip Structure (1/49 Duty Configurations)

Single-Chip Structure (1/33 Duty Configurations)

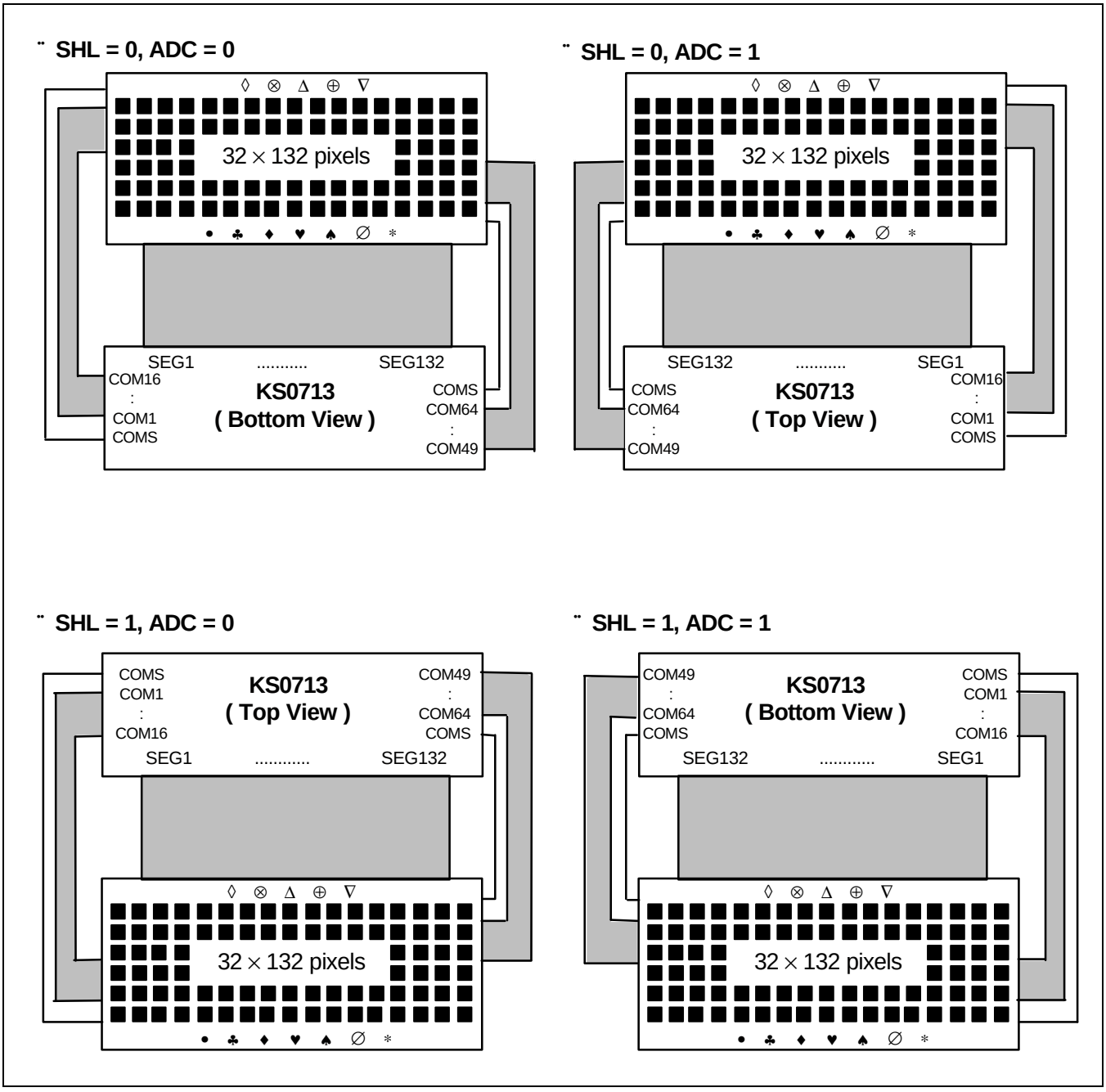


Figure 31. Single-Chip Structure (1/33 Duty Configurations)

Multi-Chip Structure (1/65 Duty Configurations)

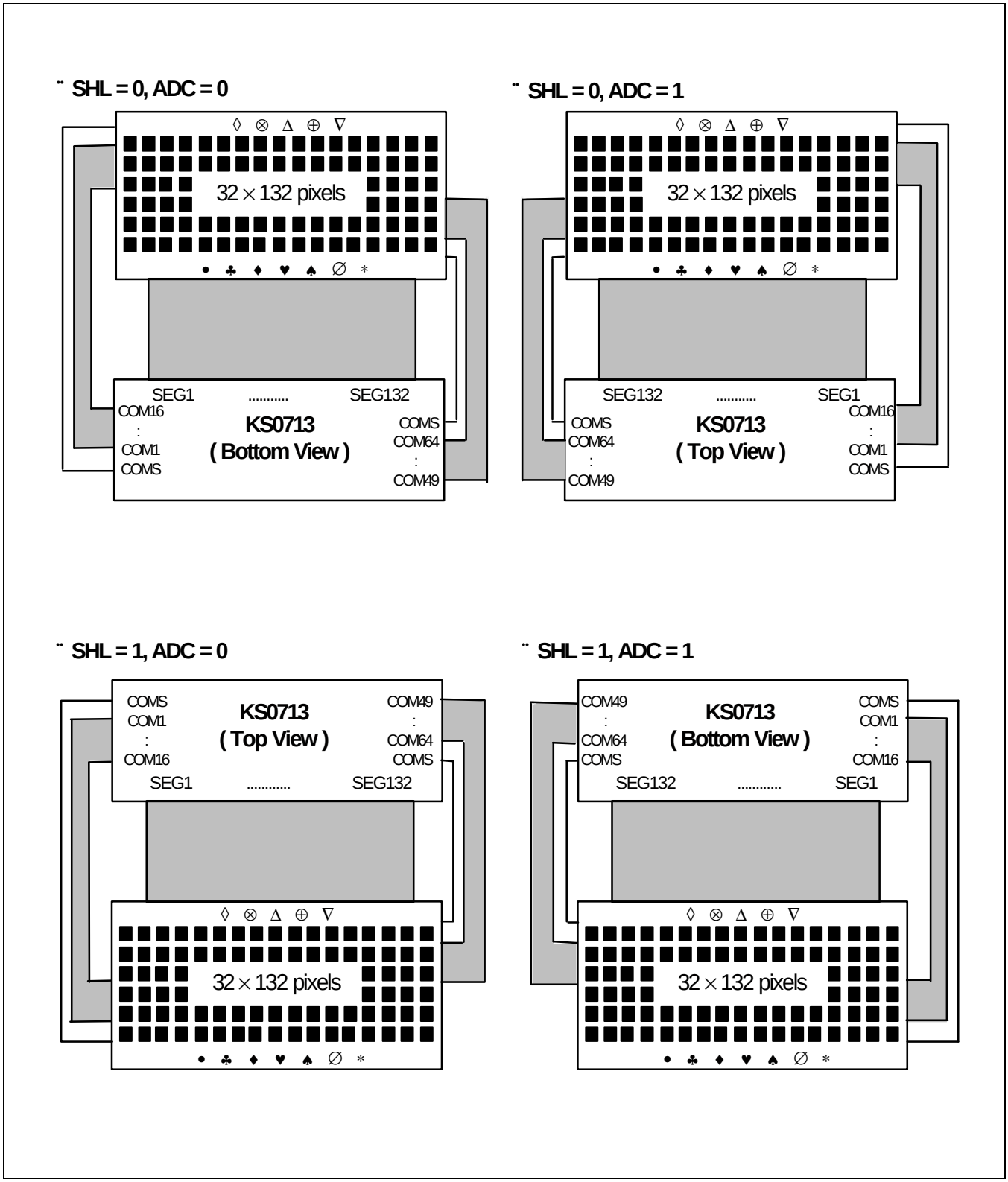


Figure 32. Multi-Chip Structure

KS0713 TCP PIN LAYOUT (SAMPLE)