INTRODUCTION

64 G/S 384CH. SOURCE DRIVER

The KS0664 is a 384-channel output, TFT LCD source driver for 64 gray scale displays.
Data input is a digital input consisting of 6 bits by 3 dots, while can realize a full-color display of 260,000 colors by output of 64 values γ-corrected.

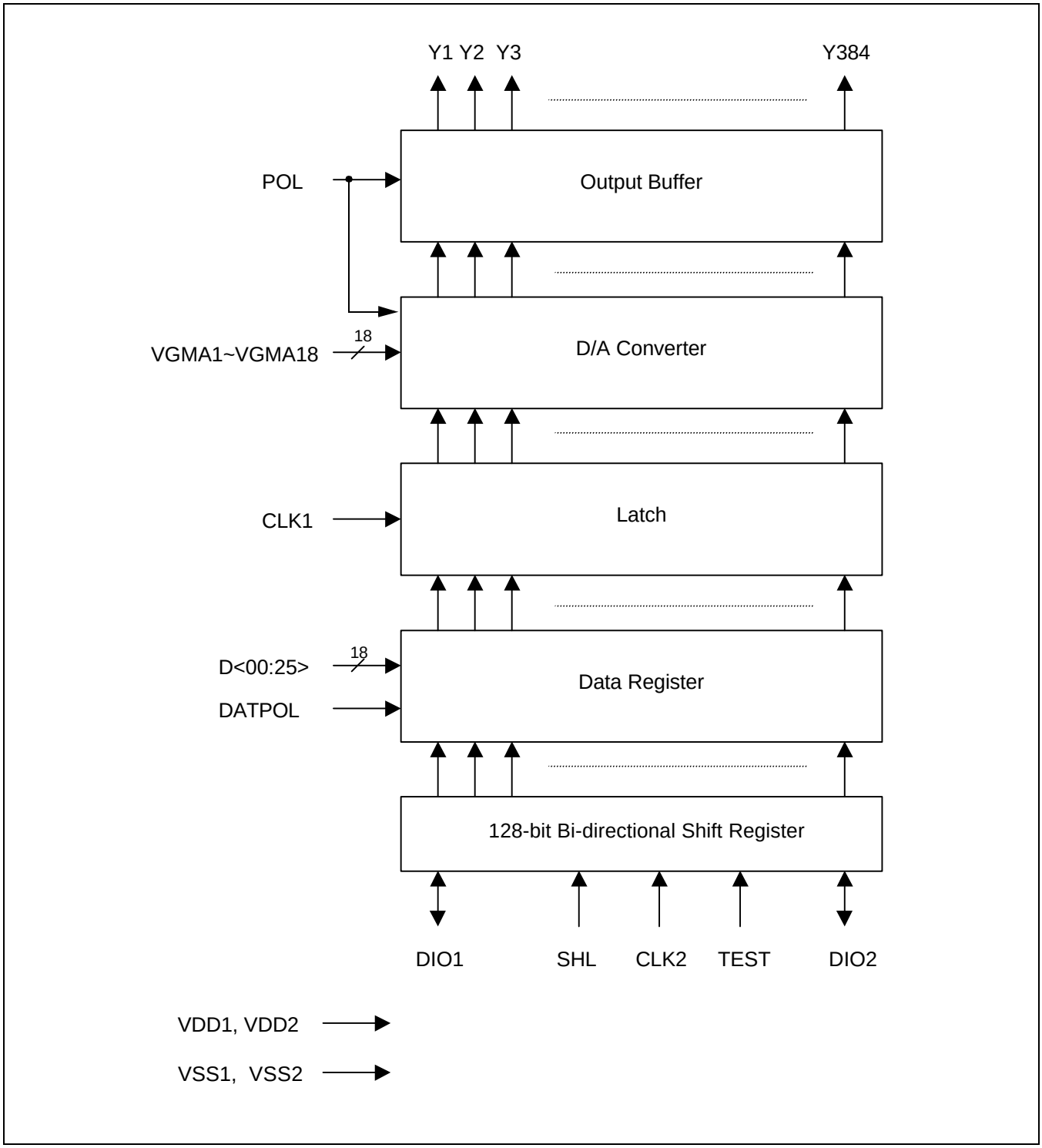
This device has an internal D/A (digital-to-analog) converter for each output and utilizes 18(9×2) external power supplies. Because the output dynamic range is as large as 6.0 to 12.6 Vp-p, it is unnecessary to operate level inversion of the LCDs common electrode. Besides, to be able to deal with dot-line inversion when mounted on a single-side, output gray scale voltages with different polarity can be output to the odd number output pins and the even number output pins.

The KS0664 can be adjusted to larger panel, and SHL (shift direction selection) pin makes use of the LCD panel connection convenient. Maximum operation clock frequency is 45 MHz at a 2.7 V logic operation and it can be applied to the TFT LCD panel of XGA/SXGA standards.

FEATURES

- ❑ TFT active matrix LCD source driver LSI.
- ❑ 64 outputs are possible through 18 (9 × 2) external power supply and D/A converter.
- ❑ Dot inversion display is possible.
- ❑ CMOS level input.
- ❑ 6 bits (G/S data) × 3dots (RGB) input: 1 port.
- ❑ Input data inversion function (DATPOL).
- ❑ Logic supply voltage: 2.7 to 3.6V.
- ❑ LCD drive supply voltage: 6.4 to 13.0V.
- ❑ Output dynamic range: 6.0 to 12.6Vp-p.
- ❑ Maximum operation clock frequency:
  fmax = 45MHz (internal data transmission rate at 2.7V operation)
- ❑ Output : 384 outputs.
- ❑ Slim TCP.

BLOCK DIAGRAM

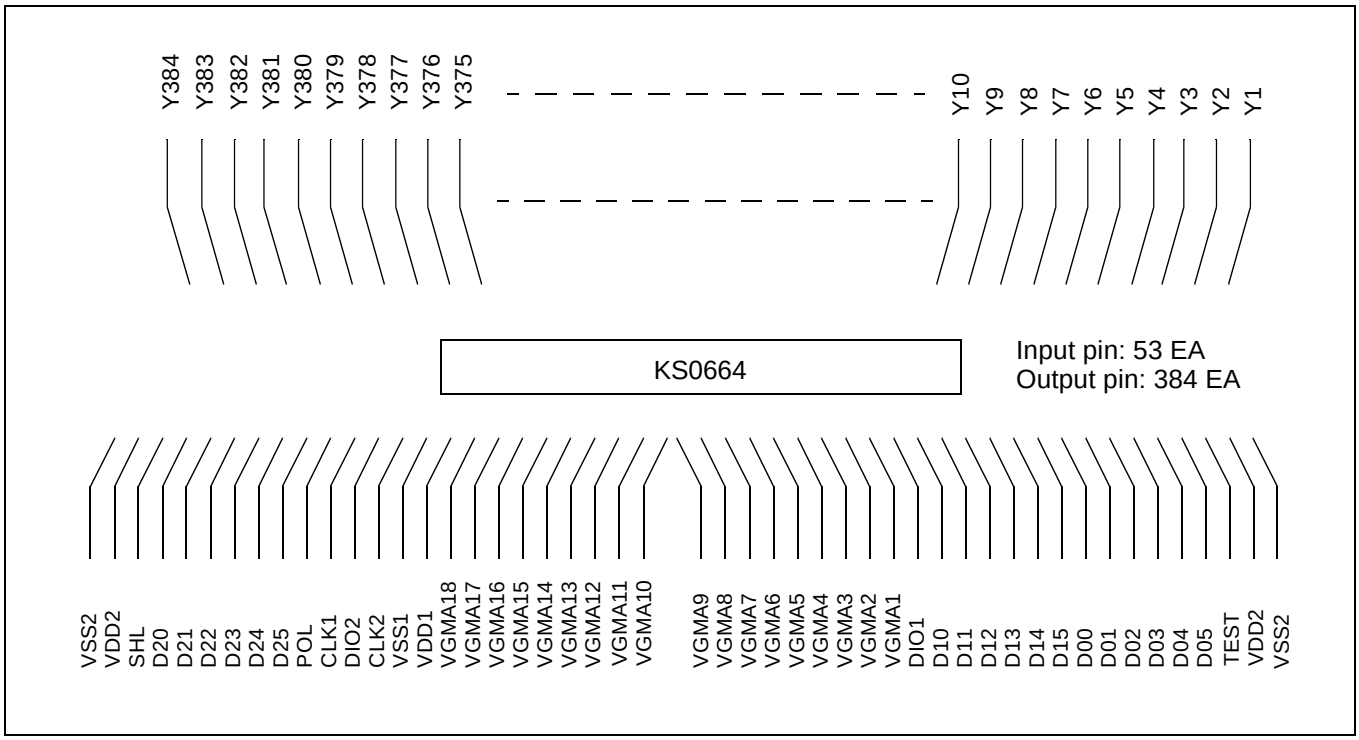


PIN DESCRIPTION

Pin Symbol	Pin Name	Description
V_{DD1}	Logic power supply	2.7 V to 3.6 V
V_{DD2}	Driver power supply	6.4 V to 13.0 V
V_{SS1}	Logic ground	Ground (0 V)
V_{SS2}	Driver ground	Ground (0 V)
Y1 to Y384	Driver Output	The D/A converted 64 G/S analog voltage is output
D0<0:5> D1<0:5> D2<0:5>	Display data input	The display data is input with a width of 18 bits, gray scale data (6 bits) × 3dots (R, G, B) DX0: LSB, DX5: MSB
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift register is as follows. SHL = H: DIO1 input (Y1→ Y384), DIO2 output SHL = L: DIO2 input (Y384 → Y1), DIO1 output
DIO1	Right shift start pulse input/output	SHL = H: DIO1 used as the start pulse input pin. (DIO2 is output) SHL = L: DIO1 used as the start pulse output pin. (DIO2 is input) The shift start pulse input triggers the latch of the bidirectional shift register, and the shift start pulse output transfers to the next chip as the next shift start pulse input. These start pulse in/out signal is controlled by the signal SHL.
DIO2	Left shift start pulse input/output	
CLK2	Shift clock input	Refer to shift clock input of the shift register. The display data is loaded to the data register at the rising edge of CLK2.
CLK1	Latch input	Latches the data register contents as rising edge and transfers it to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the Relationship between CLK1 start pulse (DIO1, DIO2) and blanking period of the switching characteristic waveform. (page 9)
VGMA1 to VGMA18	Gamma reference voltage	The gamma reference voltages, VGMA1 to 18, must be externally supported in order to operate the dot inversion. When a dot has a positive polarity, D/A converter refers to VGMA1 to 9 (high region) and when a dot has negative polarity, D/A converter refers to VGMA10 to 18 (low region). To ensure that the correct analog voltages appear at the DAC outputs, the external reference voltages, VGMA1 to 18, must stabilize before D/A conversion.
POL	Polarity inversion input	Signal POL determines the output terminals of the high or low region D/A converted signals. When POL = H, D/A converted analog voltage signals with VGMA1 to 9 (high region) transfer to the odd number output terminals, and these with VGMA10 to 18 (low region) transfer to the even number output terminals. When POL = L, high region signals transfer to the even number output terminals, and low region signals transfers to the odd number output terminals.

Pin Symbol	Pin Name	Description
DATPOL	Data inversion input	Signal DATPOL controls the digital MUX, which is connected to data latch. When DATPOL = H, the digital MUX provides the inverting digital data to data latch. When DATPOL = L, the digital MUX provides the non-inverting digital data to the data latch.
TEST	Test pin	TEST = L: Normal operation TEST = H: TEST MODE → OP-AMP cut-off This pin is internally pulled-down. < R_{PD} = 15kΩ >

TCP PIN CONFIGURATION



NOTES:

1. This figure does not specify the dimensions of the TCP package.
2. In actual panel application, the power should be supplied through all the V_{DD2} and V_{SS2} pins simultaneously.

ABSOLUTE MAXIMUM RATINGS

(V_{SS1} = V_{SS2} = 0 V)

Characteristic	Symbol	Rating	Unit
Digital supply voltage	V_{DD1}	–0.3 to +6.5	V
Analog supply voltage	V_{DD2}	–0.3 to +15.0	V
Input voltage	VGMA1 to VGMA18	–0.3 to V_{DD2}+0.3	V
	Other	–0.3 to V_{DD1}+0.3	
Output voltage	DIO1, DIO2	–0.3 to V_{DD1}+0.3	V
	Y1 to Y384	–0.3 to V_{DD2}+0.3	
Operation power dissipation	Pd	200	mW
Operation Temperature	Topr	–20 to +75	C
Storage Temperature	Tstg	–55 to +125	C

If LSIs are stressed beyond the above absolute maximum ratings, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the below recommended operating range is not implied.
Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE: Power on sequence : V_{DD1} → Input voltage → V_{DD2} → VGMA1 to VGMA18

RECOMMENDED OPERATION RANGE

(Ta = –20°C to +75°C, V_{SS1} = V_{SS2} = 0 V)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital supply voltage	V_{DD1}	–	2.7	3.3	3.6	V
Analog supply voltage	V_{DD2}	–	6.4	9.0	13.0	V
γ - corrected voltage	VGMA1 to VGMA9	–	$0.5V_{DD2}$	–	V_{DD2}-0.1	V
	VGMA10 to VGMA18	–	0.1	–	$0.5V_{DD2}$	V
Output voltage range	VYO	–	0.1	–	V_{DD2}-0.1	V
Max. clock frequency	*NOTE. fmax	–	–	–	45	MHz
Output Load capacitance	CL	–	–	–	150	pF

NOTE: DD1 = 2.7V

DC CHARACTERISTICS

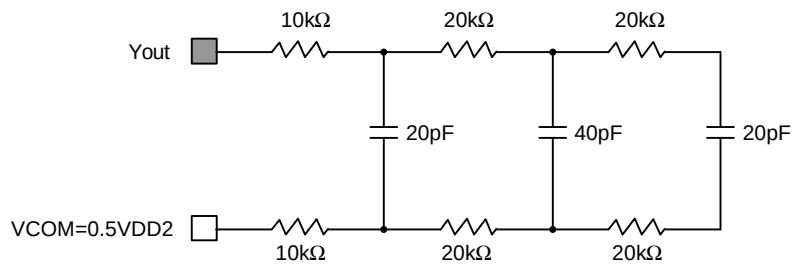
(Ta = –20 to +75°C, V_{DD1} = 2.7 to 3.6 V, V_{DD2} = 6.4 to 13.0 V, V_{SS1} = V_{SS2} = 0 V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, D00 to D25, DATPOL, CLK1, POL, Dio1 (Dio2)	$0.7V_{DD1}$	–	V_{DD1}	V
Low level input voltage	VIL		0	–	$0.3V_{DD1}$	
Input leak current	IL	D00 to D25, SHL, CLK2, DATPOL, POL, CLK1, DIO1(DIO2)	–1	–	1	µA
High level output voltage	VOH	DIO1 (DIO2), IO = –1.0mA	V_{DD1}-0.5	–	–	V
Low level output voltage	VOL	DIO1(DIO2), IO = +1.0mA	–	–	0.5	
Resistance between γ-corrected voltage	R0 to R63	*refer to page 17 resistance ladder circuit	–	*refer to page17	–	Ω
Driver output current	IVOH	V_{DD2} = 10.0V, Vx = 2.5V, VyO = 8.5V	–	–1.5	–0.5	mA
	IVOL	V_{DD2} = 10.0V, Vx = 7.5V, VyO = 1.5V	0.5	1.5	–	mA
Output voltage deviation	ΔVO	INPUT DATA: 00~3FH	–	±8	±15	mV
Output voltage range	VYO	INPUT DATA: 00~3FH	V_{SS2}+0.1	–	V_{DD2}-0.1	V
Logic part dynamic current consumption	IDD1	*Note1, No load. VDD1 = 3.0V	–	3.0	5.0	mA
Driver part dynamic current consumption	IDD2	V_{DD1} = 3.0V, V_{DD2} = 9.0 VGMA1= 8.5V,VGMA9 = 5.0V, VGMA10 = 4.0V, VGMA18 = 0.5V, *Note1, Note2, Note3	–	6.5	9.0	

(Vyo is the output voltage of analog output pins Y1 to Y384.)
(Vx is the applied voltage of analog output pins Y1 to Y384.)

NOTES:

1. CLK1 cycle = 20µs, fCLK2 = 33 MHz, data pattern = 1010 ····· (Checkerboard pattern), Ta = 25°C
2. The current consumption per driver when SVGA single-sided mounting (8units) are connected in cascade.
3. Yout load condition.



AC CHARACTERISTICS

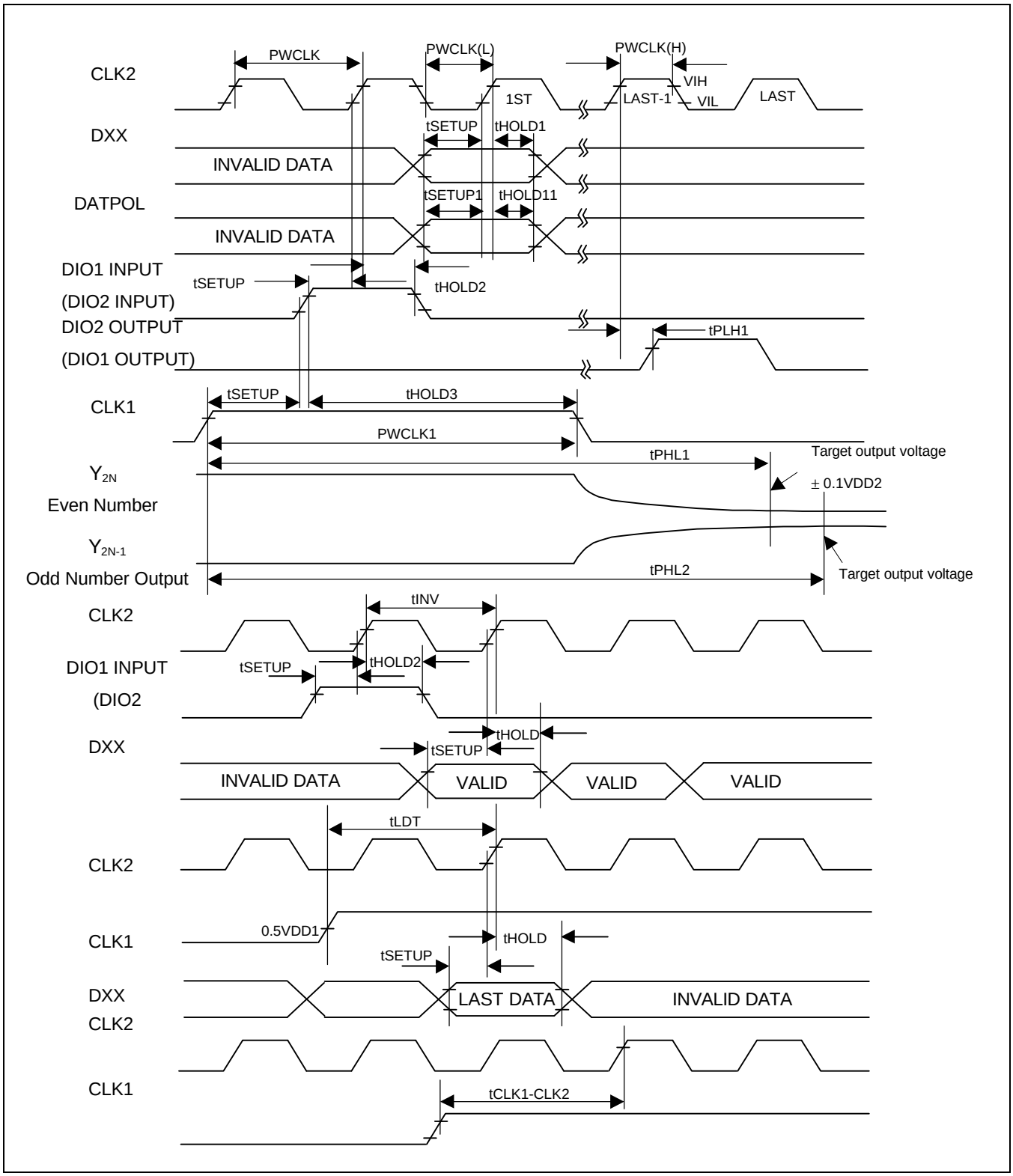
(Ta = –20 to +75°C, V_{DD1} = 2.7 to 3.6V, V_{DD2} = 6.4 to 13.0V, V_{SS1} = V_{SS2} = 0V)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	–	22	–	–	ns
Clock pulse low period	PWCLK(L)	–	6	–	–	
Clock pulse high period	PWCLK(H)	–	6	–	–	
Data setup time	tSETUP1	–	6	–	–	
Data hold time	tHOLD1	–	0	–	–	
Start pulse setup time	tSETUP2	–	6	–	–	
Start pulse hold time	tHOLD2	–	0	–	–	
DATPOL-CLK2 setup time	tSETUP4	–	6	–	–	
DATPOL-CLK2 hold time	tHOLD4	–	0	–	–	
Start pulse delay time	tPLH1	CL = 20pF	-	–	16	
CLK1 setup time	tSETUP3	–	1	–	-	CLK2 cycle
CLK1 high pulse width	PWCLK1	–	3	–	-	µs
Driver output delay time(1)	tPHL1	refer to Note3 (page6), Note4.	–	–	5	
Driver output delay time(2)	tPHL2	refer to Note3 (page6), Note5.	–	–	10	
Data invalid time	tINV	Note 6	1	–	–	CLK2 cycle
Last data time	tLDT	–	1	–	–	
CLK1-CLK2 time	tCLK1-CLK2	CLK1 ↑ → CLK2 ↑	6	–	–	ns
POL-CLK1 time	tPOL-CLK1	POL ↑ or ↓ → CLK1 ↑	-5	–	–	

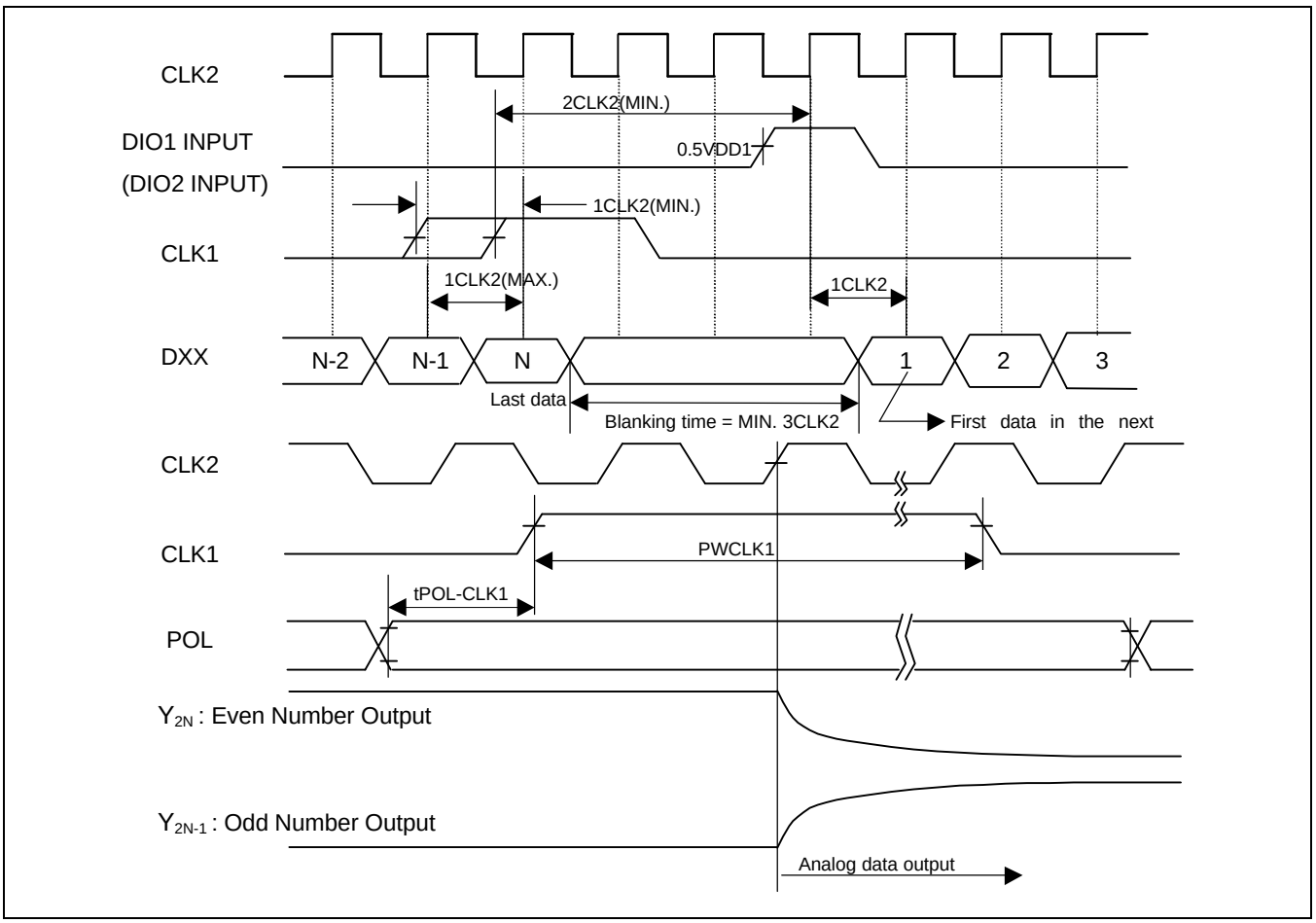
NOTES:

4. The value is specified when the drive voltage value reaches the target output voltage level of 90%
5. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
6. Set the rising edge of the first CLK2 after the rising edge of DIO1(or DIO2).

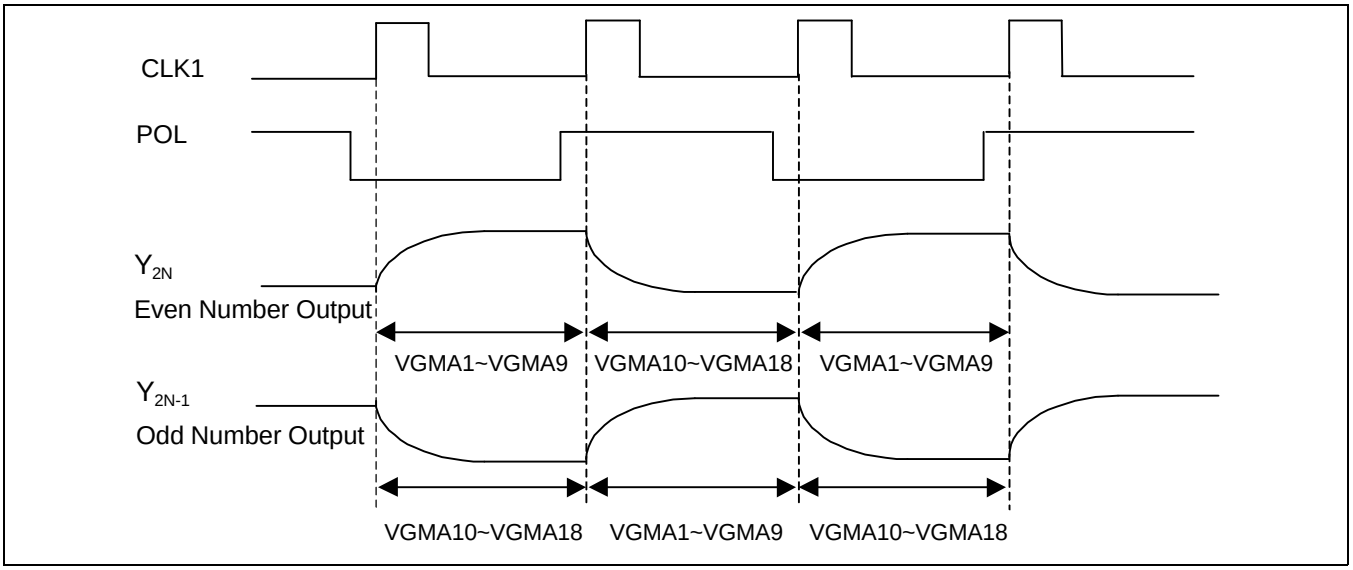
AC Waveform (VIH = 0.7V_{DD1}, VIL= 0.3V_{DD1})



Relationship between CLK1/start pulse (DIO1, DIO2) and blanking period



Relationship between CLK1, POL and output



DISPLAY DATA TRANSFER

DIO1 (or DIO2) = H is loaded into internal latch at the rising edge of CCLK2, which starts the data transfer operation, and after the falling edge of DIO1 (or DIO2), display data is valid at the rising edge of CLK2.
Once all the data of 384 channels is loaded into internal latch, it goes into standby state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1(or DIO2) input.
When DIO1 (or DIO2) is provided, new display data is valid at the next rising edge of CLK2 after the falling edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

- SHL = L
  Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.
- SHL = H
  Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

RELATIONSHIP #1 BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE

Outputs 64-level gray scale voltage generated by level 18 (9 × 2) of γ -corrected power supplies (VGMA1 to VGMA18) and 6-bit digital data.
Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins.
Among 9-by-2 γ -corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective 9 γ - corrected voltages of VGMA1 to VGMA9 and VGMA10 to VGMA18.
data format: 1PIXEL data (6 bits) × RGB (3 dots)
input width: 18 bits.

- Details on display data

DX5	DX4	DX3	DX2	DX1	DX0
Upper bits					Lower bits

- Relationship between shift direction and output data

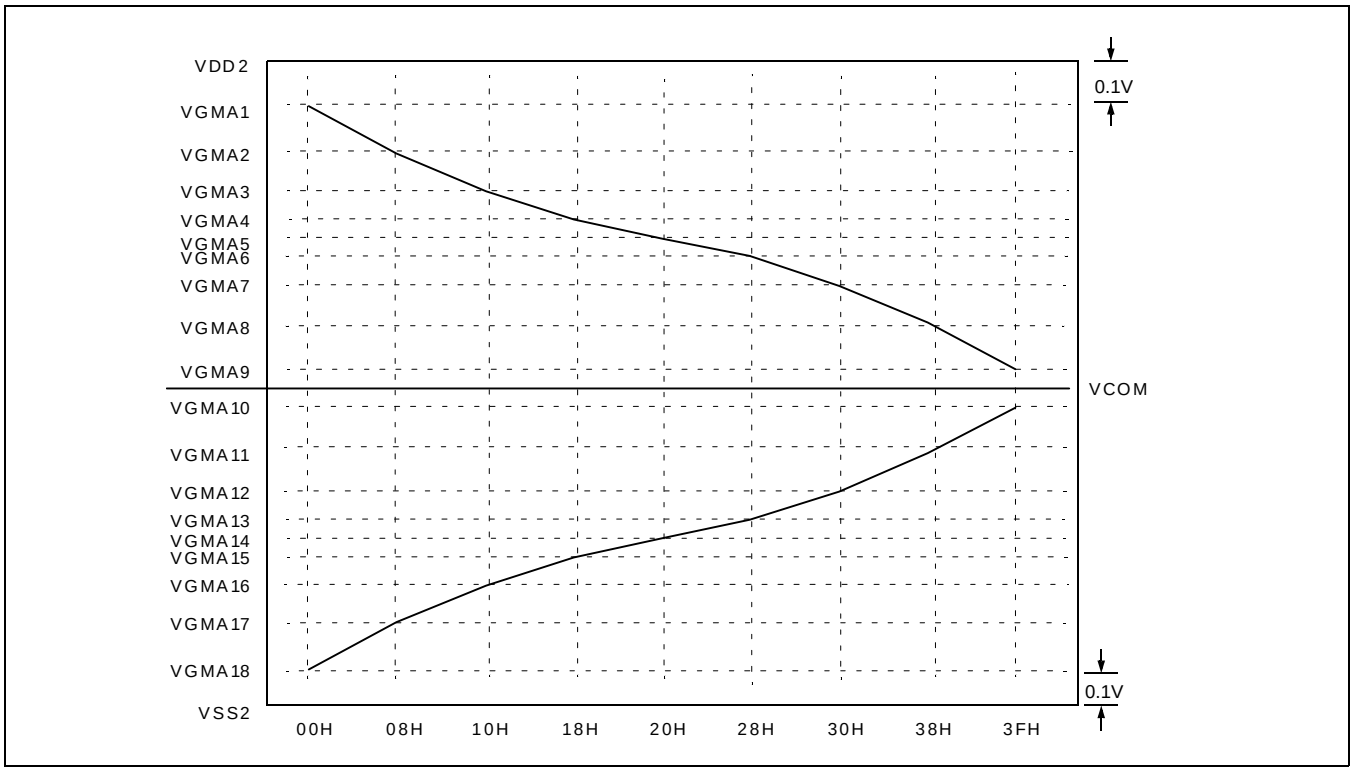
SHL = H (Right shift)

Output	Y1	Y2	Y3	-------	Y382	Y383	Y384
–	First			→	Last		
DATA	D00 to D05	D10 to D15	D20 to D25	-------	D00 to D05	D10 to D15	D20 to D25

SHL = L (Left shift)

Output	Y1	Y2	Y3	-------	Y382	Y383	Y384
–	Last			←	First		
DATA	D00 to D05	D10 to D15	D20 to D25	-------	D00 to D05	D10 to D15	D20 to D25

γ - Correction Characteristic Curve



RELATIONSHIP #2BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE (1)

VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8>VGMA9

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0	VGMA1
01H	0	0	0	0	0	1	V1	VGMA1+(VGMA2-VGMA1) × 1/8
02H	0	0	0	0	1	0	V2	VGMA1+(VGMA2-VGMA1) × 2/8
03H	0	0	0	0	1	1	V3	VGMA1+(VGMA2-VGMA1) × 3/8
04H	0	0	0	1	0	0	V4	VGMA1+(VGMA2-VGMA1) × 4/8
05H	0	0	0	1	0	1	V5	VGMA1+(VGMA2-VGMA1) × 5/8
06H	0	0	0	1	1	0	V6	VGMA1+(VGMA2-VGMA1) × 6/8
07H	0	0	0	1	1	1	V7	VGMA1+(VGMA2-VGMA1) × 7/8
08H	0	0	1	0	0	0	V8	VGMA2
09H	0	0	1	0	0	1	V9	VGMA2+(VGMA3-VGMA2) × 1/8
0AH	0	0	1	0	1	0	V10	VGMA2+(VGMA3-VGMA2) × 2/8
0BH	0	0	1	0	1	1	V11	VGMA2+(VGMA3-VGMA2) × 3/8
0CH	0	0	1	1	0	0	V12	VGMA2+(VGMA3-VGMA2) × 4/8
0DH	0	0	1	1	0	1	V13	VGMA2+(VGMA3-VGMA2) × 5/8
0EH	0	0	1	1	1	0	V14	VGMA2+(VGMA3-VGMA2) × 6/8
0FH	0	0	1	1	1	1	V15	VGMA2+(VGMA3-VGMA2) × 7/8
10H	0	1	0	0	0	0	V16	VGMA3
11H	0	1	0	0	0	1	V17	VGMA3+(VGMA4-VGMA3) × 1/8
12H	0	1	0	0	1	0	V18	VGMA3+(VGMA4-VGMA3) × 2/8
13H	0	1	0	0	1	1	V19	VGMA3+(VGMA4-VGMA3) × 3/8
14H	0	1	0	1	0	0	V20	VGMA3+(VGMA4-VGMA3) × 4/8
15H	0	1	0	1	0	1	V21	VGMA3+(VGMA4-VGMA3) × 5/8
16H	0	1	0	1	1	0	V22	VGMA3+(VGMA4-VGMA3) × 6/8
17H	0	1	0	1	1	1	V23	VGMA3+(VGMA4-VGMA3) × 7/8
18H	0	1	1	0	0	0	V24	VGMA4
19H	0	1	1	0	0	1	V25	VGMA4+(VGMA5-VGMA4) × 1/8
1AH	0	1	1	0	1	0	V26	VGMA4+(VGMA5-VGMA4) × 2/8
1BH	0	1	1	0	1	1	V27	VGMA4+(VGMA5-VGMA4) × 3/8
1CH	0	1	1	1	0	0	V28	VGMA4+(VGMA5-VGMA4) × 4/8
1DH	0	1	1	1	0	1	V29	VGMA4+(VGMA5-VGMA4) × 5/8
1EH	0	1	1	1	1	0	V30	VGMA4+(VGMA5-VGMA4) × 6/8
1FH	0	1	1	1	1	1	V31	VGMA4+(VGMA5-VGMA4) × 7/8

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20H	1	0	0	0	0	0	V32	VGMA5
21H	1	0	0	0	0	1	V33	VGMA5+(VGMA6-VGMA5) × 1/8
22H	1	0	0	0	1	0	V34	VGMA5+(VGMA6-VGMA5) × 2/8
23H	1	0	0	0	1	1	V35	VGMA5+(VGMA6-VGMA5) × 3/8
24H	1	0	0	1	0	0	V36	VGMA5+(VGMA6-VGMA5) × 4/8
25H	1	0	0	1	0	1	V37	VGMA5+(VGMA6-VGMA5) × 5/8
26H	1	0	0	1	1	0	V38	VGMA5+(VGMA6-VGMA5) × 6/8
27H	1	0	0	1	1	1	V39	VGMA5+(VGMA6-VGMA5) × 7/8
28H	1	0	1	0	0	0	V40	VGMA6
29H	1	0	1	0	0	1	V41	VGMA6+(VGMA7-VGMA6) × 1/8
2AH	1	0	1	0	1	0	V42	VGMA6+(VGMA7-VGMA6) × 2/8
2BH	1	0	1	0	1	1	V43	VGMA6+(VGMA7-VGMA6) × 3/8
2CH	1	0	1	1	0	0	V44	VGMA6+(VGMA7-VGMA6) × 4/8
2DH	1	0	1	1	0	1	V45	VGMA6+(VGMA7-VGMA6) × 5/8
2EH	1	0	1	1	1	0	V46	VGMA6+(VGMA7-VGMA6) × 6/8
2FH	1	0	1	1	1	1	V47	VGMA6+(VGMA7-VGMA6) × 7/8
30H	1	1	0	0	0	0	V48	VGMA7
31H	1	1	0	0	0	1	V49	VGMA7+(VGMA8-VGMA7) × 1/8
32H	1	1	0	0	1	0	V50	VGMA7+(VGMA8-VGMA7) × 2/8
33H	1	1	0	0	1	1	V51	VGMA7+(VGMA8-VGMA7) × 3/8
34H	1	1	0	1	0	0	V52	VGMA7+(VGMA8-VGMA7) × 4/8
35H	1	1	0	1	0	1	V53	VGMA7+(VGMA8-VGMA7) × 5/8
36H	1	1	0	1	1	0	V54	VGMA7+(VGMA8-VGMA7) × 6/8
37H	1	1	0	1	1	1	V55	VGMA7+(VGMA8-VGMA7) × 7/8
38H	1	1	1	0	0	0	V56	VGMA8
39H	1	1	1	0	0	1	V57	VGMA8+(VGMA9-VGMA8) × 1/8
3AH	1	1	1	0	1	0	V58	VGMA8+(VGMA9-VGMA8) × 2/8
3BH	1	1	1	0	1	1	V59	VGMA8+(VGMA9-VGMA8) × 3/8
3CH	1	1	1	1	0	0	V60	VGMA8+(VGMA9-VGMA8) × 4/8
3DH	1	1	1	1	0	1	V61	VGMA8+(VGMA9-VGMA8) × 5/8
3EH	1	1	1	1	1	0	V62	VGMA8+(VGMA9-VGMA8) × 6/8
3FH	1	1	1	1	1	1	V63	VGMA8+(VGMA9-VGMA8) × 7/8

RELATIONSHIP #2BETWEEN THE INPUT DATA AND OUTPUT VOLTAGE (2)

VGMA10>VGMA11>VGMA12>VGMA13>VGMA14>VGMA15>VGMA16>VGMA17>VGMA18

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
00H	0	0	0	0	0	0	V0	VGMA18
01H	0	0	0	0	0	1	V1	VGMA18+(VGMA17-VGMA18) × 1/8
02H	0	0	0	0	1	0	V2	VGMA18+(VGMA17-VGMA18) × 2/8
03H	0	0	0	0	1	1	V3	VGMA18+(VGMA17-VGMA18) × 3/8
04H	0	0	0	1	0	0	V4	VGMA18+(VGMA17-VGMA18) × 4/8
05H	0	0	0	1	0	1	V5	VGMA18+(VGMA17-VGMA18) × 5/8
06H	0	0	0	1	1	0	V6	VGMA18+(VGMA17-VGMA18) × 6/8
07H	0	0	0	1	1	1	V7	VGMA18+(VGMA17-VGMA18) × 7/8
08H	0	0	1	0	0	0	V8	VGMA17
09H	0	0	1	0	0	1	V9	VGMA17+(VGMA16-VGMA17) × 1/8
0AH	0	0	1	0	1	0	V10	VGMA17+(VGMA16-VGMA17) × 2/8
0BH	0	0	1	0	1	1	V11	VGMA17+(VGMA16-VGMA17) × 3/8
0CH	0	0	1	1	0	0	V12	VGMA17+(VGMA16-VGMA17) × 4/8
0DH	0	0	1	1	0	1	V13	VGMA17+(VGMA16-VGMA17) × 5/8
0EH	0	0	1	1	1	0	V14	VGMA17+(VGMA16-VGMA17) × 6/8
0FH	0	0	1	1	1	1	V15	VGMA17+(VGMA16-VGMA17) × 7/8
10H	0	1	0	0	0	0	V16	VGMA16
11H	0	1	0	0	0	1	V17	VGMA16+(VGMA15-VGMA16) × 1/8
12H	0	1	0	0	1	0	V18	VGMA16+(VGMA15-VGMA16) × 2/8
13H	0	1	0	0	1	1	V19	VGMA16+(VGMA15-VGMA16) × 3/8
14H	0	1	0	1	0	0	V20	VGMA16+(VGMA15-VGMA16) × 4/8
15H	0	1	0	1	0	1	V21	VGMA16+(VGMA15-VGMA16) × 5/8
16H	0	1	0	1	1	0	V22	VGMA16+(VGMA15-VGMA16) × 6/8
17H	0	1	0	1	1	1	V23	VGMA16+(VGMA15-VGMA16) × 7/8
18H	0	1	1	0	0	0	V24	VGMA15
19H	0	1	1	0	0	1	V25	VGMA15+(VGMA14-VGMA15) × 1/8
1AH	0	1	1	0	1	0	V26	VGMA15+(VGMA14-VGMA15) × 2/8
1BH	0	1	1	0	1	1	V27	VGMA15+(VGMA14-VGMA15) × 3/8
1CH	0	1	1	1	0	0	V28	VGMA15+(VGMA14-VGMA15) × 4/8
1DH	0	1	1	1	0	1	V29	VGMA15+(VGMA14-VGMA15) × 5/8
1EH	0	1	1	1	1	0	V30	VGMA15+(VGMA14-VGMA15) × 6/8
1FH	0	1	1	1	1	1	V31	VGMA15+(VGMA14-VGMA15) × 7/8

Input data	DX5	DX4	DX3	DX2	DX1	DX0	Output voltage	
20H	1	0	0	0	0	0	V32	VGMA14
21H	1	0	0	0	0	1	V33	VGMA14+(VGMA13-VGMA14) × 1/8
22H	1	0	0	0	1	0	V34	VGMA14+(VGMA13-VGMA14) × 2/8
23H	1	0	0	0	1	1	V35	VGMA14+(VGMA13-VGMA14) × 3/8
24H	1	0	0	1	0	0	V36	VGMA14+(VGMA13-VGMA14) × 4/8
25H	1	0	0	1	0	1	V37	VGMA14+(VGMA13-VGMA14) × 5/8
26H	1	0	0	1	1	0	V38	VGMA14+(VGMA13-VGMA14) × 6/8
27H	1	0	0	1	1	1	V39	VGMA14+(VGMA13-VGMA14) × 7/8
28H	1	0	1	0	0	0	V40	VGMA13
29H	1	0	1	0	0	1	V41	VGMA13+(VGMA12-VGMA13) × 1/8
2AH	1	0	1	0	1	0	V42	VGMA13+(VGMA12-VGMA13) × 2/8
2BH	1	0	1	0	1	1	V43	VGMA13+(VGMA12-VGMA13) × 3/8
2CH	1	0	1	1	0	0	V44	VGMA13+(VGMA12-VGMA13) × 4/8
2DH	1	0	1	1	0	1	V45	VGMA13+(VGMA12-VGMA13) × 5/8
2EH	1	0	1	1	1	0	V46	VGMA13+(VGMA12-VGMA13) × 6/8
2FH	1	0	1	1	1	1	V47	VGMA13+(VGMA12-VGMA13) × 7/8
30H	1	1	0	0	0	0	V48	VGMA12
31H	1	1	0	0	0	1	V49	VGMA12+(VGMA11-VGMA12) × 1/8
32H	1	1	0	0	1	0	V50	VGMA12+(VGMA11-VGMA12) × 2/8
33H	1	1	0	0	1	1	V51	VGMA12+(VGMA11-VGMA12) × 3/8
34H	1	1	0	1	0	0	V52	VGMA12+(VGMA11-VGMA12) × 4/8
35H	1	1	0	1	0	1	V53	VGMA12+(VGMA11-VGMA12) × 5/8
36H	1	1	0	1	1	0	V54	VGMA12+(VGMA11-VGMA12) × 6/8
37H	1	1	0	1	1	1	V55	VGMA12+(VGMA11-VGMA12) × 7/8
38H	1	1	1	0	0	0	V56	VGMA11
39H	1	1	1	0	0	1	V57	VGMA11+(VGMA10-VGMA11) × 1/8
3AH	1	1	1	0	1	0	V58	VGMA11+(VGMA10-VGMA11) × 2/8
3BH	1	1	1	0	1	1	V59	VGMA11+(VGMA10-VGMA11) × 3/8
3CH	1	1	1	1	0	0	V60	VGMA11+(VGMA10-VGMA11) × 4/8
3DH	1	1	1	1	0	1	V61	VGMA11+(VGMA10-VGMA11) × 5/8
3EH	1	1	1	1	1	0	V62	VGMA11+(VGMA10-VGMA11) × 6/8
3FH	1	1	1	1	1	1	V63	VGMA11+(VGMA10-VGMA11) × 7/8

g - Corrected Power Circuit and Relationship Input Data and Output Voltage.

* Ladder Resistance Value (R0 to R63, Unit: W)

Name	Value	Name	Value
R0	380	R32	191
R1	380	R33	191
R2	380	R34	191
R3	380	R35	191
R4	380	R36	191
R5	380	R37	191
R6	380	R38	191
R7	380	R39	191
R8	191	R40	191
R9	191	R41	191
R10	191	R42	191
R11	191	R43	191
R12	191	R44	191
R13	191	R45	191
R14	191	R46	191
R15	191	R47	191
R16	191	R48	191
R17	191	R49	191
R18	191	R50	191
R19	191	R51	191
R20	191	R52	191
R21	191	R53	191
R22	191	R54	191
R23	191	R55	191
R24	191	R56	380
R25	191	R57	380
R26	191	R58	380
R27	191	R59	380
R28	191	R60	380
R29	191	R61	380
R30	191	R62	380
R31	191	R63	380